REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Paragraph 1.3: Made corrections. Table I: Made corrections throughout to accurately reflect how the part is tested and to incorporate RHA limits. Figure 4: Made corrections. Editorial changes throughout. -sld	16-05-23	Charles F. Saffle

REV																				
SHEET																				
REV	A	A																		
SHEET	15	16																		

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
14-02-06

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

MICROCIRCUIT, CMOS, ANALOG TO DIGITAL CONVERTER, 14-BIT, 8 CHANNEL MULTIPLEXED, MONOLITHIC SILICON

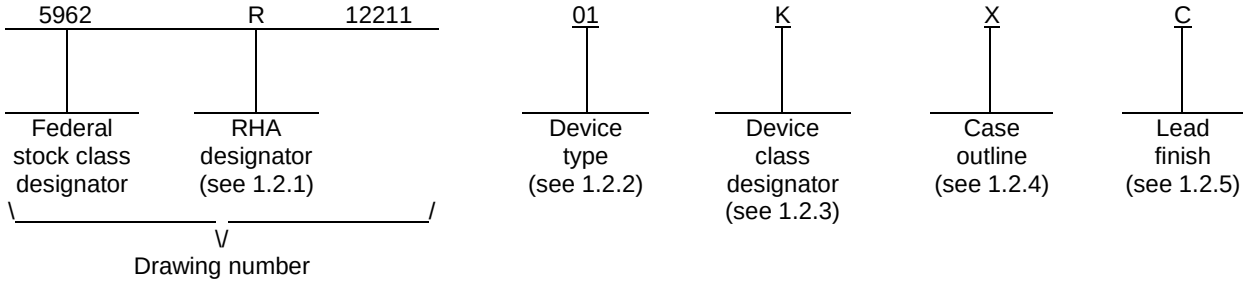
SIZE	CAGE CODE	
A	**67268**	**5962-12211**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices meet the MIL-PRF-38534 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHD5958	A/D converter, 14-bit, 8 channel multiplexed

1.2.3 Device class designator. This device class designator is a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	40	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltages	+7.0 V dc
Clock frequency	1.5 MHz
Input voltage (PREF, NREF)	V_{CC} + 0.4 V, GND - 0.4 V
Thermal resistance, junction-to-case (Θ_{JC})	+2.0° C/W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Power dissipation (P_D)	130 mW
Case operating temperature range (T_C)	-55°C to +125°C

1.4 Recommended operating conditions.

Analog power supply voltage (AV_{CC})	+5.0 V
Digital power supply voltage (DV_{CC})	+5.0 V
Digital output high reference level range (DRVP)	+3.3 V to +5.0 V
Digital output low reference level (DRVN)	0 V
High analog reference voltage (PREF)	+4.5 V
Low analog reference voltage (NREF)	+0.5 V

1.5 Radiation features. 2/

Maximum Total Ionizing Dose (TID) ..(dose rate = 50 - 300 rad(Si)/s):	
In accordance with MIL-STD-883, method 1019, condition A	100 krad(Si) 3/
Enhanced Low Dose Rate Sensitvity (ELDRS)	4/
Single Event Latchup (SEL)	> 100 MeV-cm^2/mg 5/
Neutron Displacement Damage (> 1 x 10^{14} neutrons/cm^2)	4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ See section 4.3.5 for the manufacturer's radiation hardness assurance analysis and testing.
3/ The device will be tested every wafer diffusion lot.
4/ Not tested, Immune by 100 percent CMOS technology.
5/ Single Event Latchup (SEL) immunity is accomplished by double, fully enclosing, guard rings in the CMOS design layout. The guard rings eliminate the parasitic pnpn structure that is responsible for latchup in CMOS circuits. This limit is guaranteed by design or process, but not tested.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify, or optimize the tests and inspections herein, however, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Radiation exposure circuits. The radiation exposure circuits shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions A_{VCC} = +5.0 V, D_{VCC} = +5.0 V, DRVP = +5.0 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital supply current sleep 1/	DI_{CCS}	$V_{EN} = D_{GND}$, $V_{OE} = D_{GND}$	1,2,3	01		1	mA
Digital supply current active 1/	DI_{CCA}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$	1,2,3	01		2	mA
Digital supply current quiescent 1/	DI_{CCQ}	$V_{EN} = D_{VCC}$, CLK = D_{GND}, $V_{OE} = D_{VCC}$	1,2,3	01		1	mA
Analog supply current sleep 1/	AI_{CCS}	$V_{EN} = D_{GND}$, $V_{OE} = D_{GND}$	1,2,3	01		4	mA
Analog supply current active 1/	AI_{CCA}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$	1,2,3	01		10	mA
Analog supply current 1/ quiescent	AI_{CCQ}	$V_{EN} = D_{VCC}$, CLK = D_{GND}, $V_{OE} = D_{VCC}$	1,2,3	01		10	mA
Digital output supply current 1/ sleep	I_{DRVPS}	$V_{EN} = D_{VCC}$, C_L = 50 pF, $V_{OE} = D_{GND}$	1,2,3	01		1	mA
Digital output supply current 1/ active	I_{DRVPA}	$V_{EN} = D_{VCC}$, C_L = 50 pF, $V_{OE} = D_{VCC}$	1,2,3	01		1	mA
Digital output supply current 1/ quiescent	I_{DRVPQ}	$V_{EN} = D_{VCC}$, C_L = 50 pF, CLK = D_{GND}, $V_{OE} = D_{VCC}$	1,2,3	01		0.10	mA
Full-scale input range 1/	V_{IN}		1,2,3	01	V_{NREF}	V_{PREF}	V
Input capacitance 2/	C_{IN}	T_C = +25°C	1	01		50	pF
Analog reference impedance 1/	Z_{REF}	PREF to NREF	1,2,3	01	2	6	kΩ
High analog reference voltage	V_{PREF}	DRVP = 5.0 V 1/	1,2,3	01	V_{NREF}	+5.0	V
		DRVP = 3.3 V 2/			V_{NREF}	+5.0	
Low analog reference voltage	V_{NREF}	DRVP = 5.0 V 1/	1,2,3	01	0	V_{PREF}	V
		DRVP = 3.3 V 2/			0	V_{PREF}	
Integral non-linearity 1/	INL	PREF-NREF = 4.0 V	4,5,6	01	-48	48	LSBs
Differential non-linearity 1/	DNL	PREF-NREF = 4.0 V	4,5,6	01	-8.2	8.2	LSBs
DC offset 1/	V_{OS}	PREF-NREF = 4.0 V	4,5,6	01	-1	1	%FSR
DC gain 1/	A_E	PREF-NREF = 4.0 V	4,5,6	01	-2	2	%FSR
Channel isolation 2/	ISO	T_C = +25°C	4	01	80		dB
Clock frequency 1/	f_C	PREF-NREF = 5.0 V	4,5,6	01		1	MHz
Maximum sampling rate 2/	f_{SAMPLE}	f_C = 1 MHz	4,5,6	01		50	kSPS
Digital high level input voltage EN_H, STCNV_H, OE_H, CLK (AD00 - AD02)	V_{IH}	DRVP = 5.0 V 1/	1,2,3	01	3.5		V
		DRVP = 3.3 V 2/			2.31		
Digital low level input voltage EN_H, STCNV_H, OE_H, CLK (AD00 - AD02)	V_{IL}	DRVP = 5.0 V 1/				1.5	
		DRVP = 3.3 V 2/				0.99	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions A_{VCC} = +5.0 V, D_{VCC} = +5.0 V, DRVP = +5.0 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital high level input current EN_H, STCNV_H, OE_H, CLK (AD00 - AD02) 1/ 3/	I_{IH}	DRVP = 5.0 V, V_{IH} = 5.0 V, All other digital inputs = D_{GND}	1	01	-5	5	nA
			2		-50	50	
Digital low level input current EN_H, STCNV_H, OE_H, CLK (AD00 - AD02) 1/ 3/	I_{IL}	DRVP = 5.0 V, V_{IL} = 0.0 V, All other digital inputs = D_{GND}	1	01	-5	5	nA
			2		-50	50	
High input leakage current (AIN00 - AIN15) 1/ 4/	$I_{INLK(HI)}$	Input under test = A_{VCC}, V_{EN} = D_{VCC}	1	01	-5	5	nA
			2		-50	50	
Low input leakage current (AIN00 - AIN15) 1/ 4/	$I_{INLK(LO)}$	Input under test = A_{GND}, V_{EN} = D_{VCC}	1	01	-5	5	nA
			2		-50	50	
Digital high level output voltage (B00 - B13)	V_{OH}	DRVP = 5.0 V, I_{OH} = -1.0 mA 2/	1,2,3	01	4.6		V
		DRVP = 5.0 V, I_{OH} = -4.0 mA 1/ 4/			4.2		
		DRVP = 3.3 V, I_{OH} = -1.0 mA 2/			3.0		
		DRVP = 3.3 V, I_{OH} = -4.0 mA 1/ 4/			2.7		
Digital low level output voltage (B00 - B13)	V_{OL}	DRVP = 5.0 V, I_{OL} = 1.0 mA 2/	1,2,3	01		0.4	V
		DRVP = 5.0 V, I_{OL} = 4.0 mA 1/ 4/	1,3			0.6	
			2			0.8	
		DRVP = 3.3 V, I_{OL} = 1.0 mA 2/	1,2,3			0.4	
		DRVP = 3.3 V, I_{OL} = 4.0 mA 1/ 4/	1,3			0.6	
			2			0.8	
Digital high level output current (B00 - B13) 1/ 4/	I_{OH}	DRVP = 5.0 V, V_{EN} ≥ V_{IH}	1,2,3	01		-4.0	mA
		DRVP = 3.3 V, V_{EN} ≥ V_{IH}				-4.0	
Digital low level output current (B00 - B13) 1/ 4/	I_{OL}	DRVP = 5.0 V, V_{EN} ≥ V_{IH}	1,2,3	01		4.0	mA
		DRVP = 3.3 V, V_{EN} ≥ V_{IH}				4.0	
High output leakage current (B00 - B13) 1/ 4/	$I_{OUTLK(HI)}$	V_{OE} = D_{GND}	1	01	-5	5	nA
			2		-50	50	
Low output leakage current (B00 - B13) 1/ 4/	$I_{OUTLK(LO)}$	V_{OE} = D_{GND}	1	01	-5	5	nA
			2		-50	50	

1/ This device has been tested to (100 krad(Si)) to Method 1019, condition A of MIL-STD-883 at +25°C for these parameters.
2/ Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.
3/ Subgroup 3 for these parameters is guaranteed, but not production tested.
4/ This test or test condition was used during Radiation Lot Acceptance Testing (RLAT), but not production tested.

Case outline X.

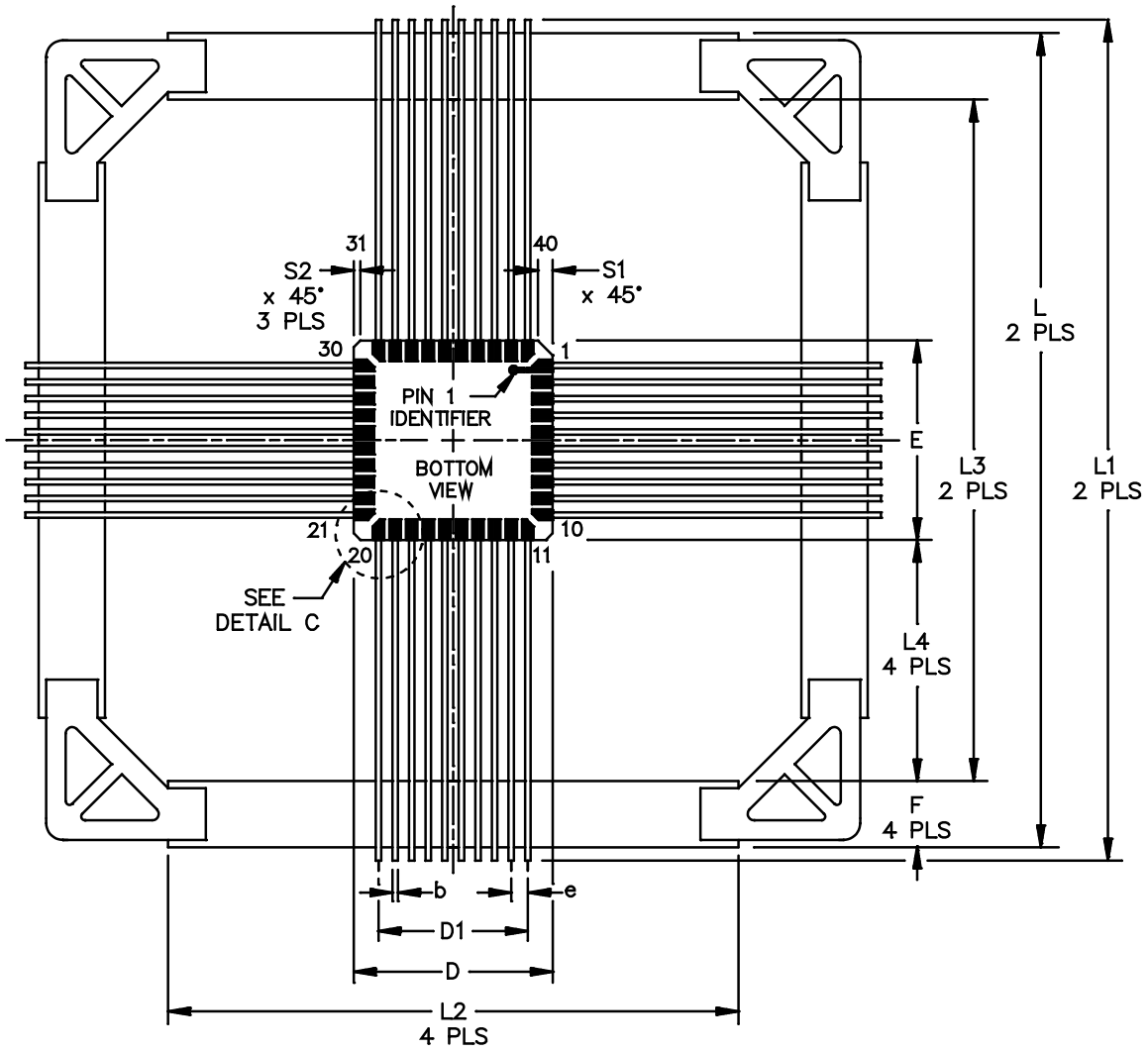
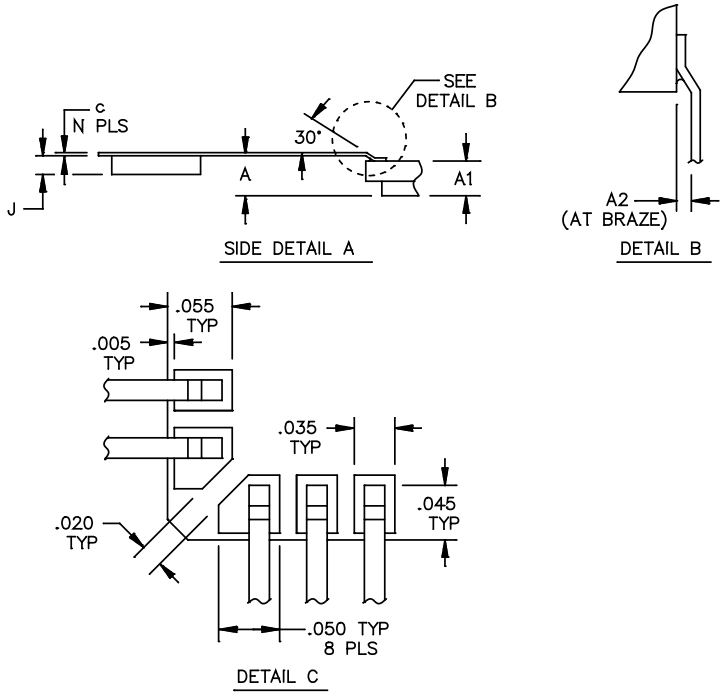


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12211
		REVISION LEVEL A	SHEET 7



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.120		3.05
A1		.111		2.82
A2	.005	.011	.13	.28
b	.0135	.0195	.343	.495
c	.004	.008	.10	.20
D/E	.590	.610	14.99	15.49
D1	.444	.456	11.28	11.58
e	.050 BSC		1.27 BSC	
F	.200 TYP		5.08 TYP	
J	.035 TYP		.89 TYP	
L	2.490	2.510	63.25	63.75
L1		2.580		65.53
L2	1.700	1.740	43.18	44.20
L3	2.090	2.110	53.09	53.60
L4	.750 TYP		19.05 TYP	
N	40		40	
S1	.030 TYP		.76 TYP	
S2	.015 TYP		.38 TYP	

NOTES:
1. Pin 1 is indicated by the ESD marking on top of the package and the extended lead on the bottom of the package.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. N equals 40, the total number of leads on the package.
4. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AV_{CC}	21	B10
2	DV_{CC}	22	B11
3	AD02	23	B12
4	AD01	24	B13
5	AD00	25	EOC_H
6	CASE GND	26	BUSY_L
7	STCNV_H	27	DRVN
8	EN_H	28	DRVP
9	OE_H	29	D_{GND}
10	CLK	30	A_{GND}
11	B00	31	PREF
12	B01	32	AIN07
13	B02	33	AIN06
14	B03	34	AIN05
15	B04	35	AIN04
16	B05	36	AIN03
17	B06	37	AIN02
18	B07	38	AIN01
19	B08	39	AIN00
20	B09	40	NREF

FIGURE 2. Terminal connections.

AD02	AD01	AD00	EN_H	"ON" Channel
X	X	X	L	None
L	L	L	H	AIN00
L	L	H	H	AIN01
L	H	L	H	AIN02
L	H	H	H	AIN03
H	L	L	H	AIN04
H	L	H	H	AIN05
H	H	L	H	AIN06
H	H	H	H	AIN07

FIGURE 3. Truth table.

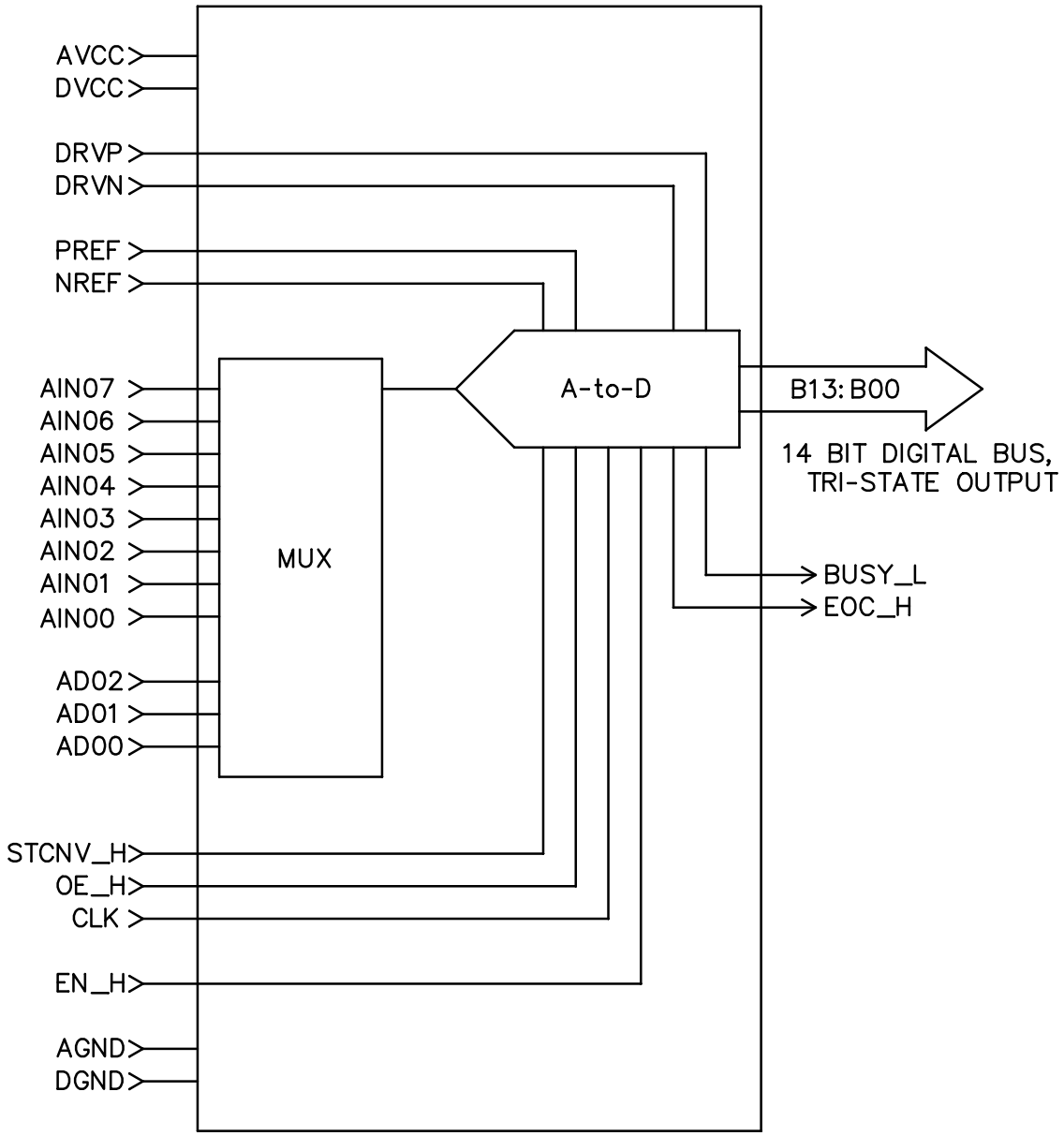


FIGURE 4. Block diagram.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*,2,3,4,5,6
Group A test requirements	1,2,3,4,5,6
Group C end-point electrical parameters	1,2,3,4,5,6
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	1

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5. Radiation hardness assurance (RHA). RHA qualification is required only for those devices with the RHA designator as specified herein. See table IIIA and table IIIB.

Table IIIA. Radiation Hardness Assurance Method Table.

RHA method employed	**Total Dose Testing RHA level "R" 100 krad(Si)**		**Worst Case Analysis Performed**				**End point electricals after total dose**	
	Element level	Hybrid device level	Includes temperature effects	Combines temperature and radiation effects	Combines total dose and displacement effects	End-of-life	Element level	Hybrid device level
	Tested at 100 krad(Si)	Tested at 100 krad(Si) (See 4.3.5.1.1)	No	No	No	No	T_C = +25°C	T_C = +25°C

Table IIIB. Hybrid level and element level test table.

	Radiation Test								
	Total Dose			**Heavy Ion**		**Proton**		**Neutron**	
	Low Dose Rate (LDR)	High Dose Rate (HDR)	ELDRS	SET (transient)	SEL (latch-up)	Low Energy	High Energy	SEE (upset)	Displacement Damage (DD)
CMOS IC	G	Tested 100 krad(Si)	G	Not Tested	G 100 MeV-cm^2/mg	Not Tested	Not Tested	Not Tested	G

NOTE:
G = Guaranteed by design or process.

4.3.5.1 Radiation Hardness Assurance (RHA) inspection. RHA qualification is required for those devices with the RHA designator as specified herein. End-point electrical parameters for radiation hardness assurance (RHA) devices shall be specified in table II. Radiation testing will be in accordance with the qualifying activity (DLA Land and Maritime -VQ) approved plan and with MIL-PRF-38534, Appendix G.

a. The hybrid device manufacturer shall establish procedures controlling component radiation testing, and shall establish radiation test plans used to implement component lot qualification during procurement. Test plans and test reports shall be filed and controlled in accordance with the manufacturer's configuration management system.

b. The hybrid device manufacturer shall designate a RHA program manager to oversee component lot qualification, and to monitor design changes for continued compliance to RHA requirements.

4.3.5.1.1 Hybrid level RHA qualification. Hybrid level and element level testing are the same for the devices on this Standard Microcircuit Drawing (SMD) since the active element is accessible to the device leads for test.

4.3.5.1.1.1 Qualification by similarity. The device on this (SMD) is considered similar for the purpose of RHA testing. Device type 5962R1220301KXC was RHA tested, therefore the device type on this SMD is qualified by similarity.

4.3.5.1.2 Element level qualification.

4.3.5.1.2.1 Total ionizing dose irradiation testing. A minimum of 5 biased and 5 unbiased devices of the active element used will be tested every wafer lot. This active element will be tested at HDR in accordance with condition A of method 1019 of MIL-STD-883 to 100 krad(Si) for the device parameters as specified in table I herein.

4.3.5.1.2.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed per paragraph 3.12.2 of MIL-STD-883, Test Method 1019 on all CMOS devices. The post-anneal end-point electrical parameter test data values shall not exceed the maximum irradiated dose level limits specified in table I herein at 25°C ±5°C.

4.3.5.2 RHA Lot Acceptance. Each wafer lot of the active element shall be evaluated for acceptance in accordance with MIL-PRF-38534 and herein.

4.3.5.2.1 Total Ionizing Dose (TID). See paragraph 4.3.5.1.2.1 and 4.3.5.1.2.1.1 herein.

4.3.5.2.2 Enhanced Element Evaluation. Enhanced Element Evaluation per Table IV herein including 45 devices subjected to Group C2, 1000 hours life testing, is required only for those devices with the RHA designator as specified herein.

Table IV. Enhanced Element Evaluation For Microcircuit Die.

Subgroup	Class K	Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity (accept number)	Reference Paragraph 1/
2	X	Element visual	2010		100 percent	C.3.3.2
		Assembled into package as specified in 1.2.4 herein.			100 percent	
1	X	Element electrical			100 percent	C.3.3.1
3	X	Internal visual	2017		45(0)	C.5.5
4	X	Temperature cycling	1010	C	45(0) 2/	C.3.3.3
	X	Constant acceleration	2001	3000g's, Y1 direction		C.5.6
	X	Burn-in	1015	160 hours minimum at +125°C		
	X	Interim electrical				C.3.3.4.3
	X	Burn-in	1015	160 hours minimum at +125°C		
	X	Post burn-in Final Electrical, Group A				C.5.10
	X	Steady-state life	1005	1000 hours minimum at +125°C		
	X	Final electrical				C.3.3.4.3
5	X	Wire bond evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018		See method 2018 of MIL-STD-883	C.3.3.6

1/ See MIL-PRF-38534.
2/ Die shall be traceable to the wafer and wafer lot. The sample size shall consist of a minimum of 3 die from each wafer and a minimum of 45 die from each wafer lot.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors, listed in MIL-HDBK-103 and QML-38534, have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-05-23

Approved sources of supply for SMD 5962-12211 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1221101KXC 5962R1221101KXC	88379 88379	RHD5958-201-1S RHD5958-901-1S

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
88379	Aeroflex Plainview Incorporated, (Aeroflex Microelectronic Solutions) 35 South Service Road Plainview, NY 11803-4193