| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add peak-to-peak jitter and random jitter test under Table IA. -jt | 14-03-21 | C.Saffle |
| B | Update paragraphs to MIL- 535 require PRF-38ments. - drw | 19-12-16 | James R. Eschmeyer |
| C | Make correction to the thermal resistance, junction-to-ambient and thermal resistance, junction-to-case values in 1.3. Add radiation hardened requirements. -rrp | 21-02-04 | James R. Eschmeyer |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | C | C | C | C | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

PMIC N/A

PREPARED BY
Jeffery Tunstall

CHECKED BY
Rajesh Pithadia

APPROVED BY
Charles Saffle

DRAWING APPROVAL DATE
12-07-30

REVISION LEVEL
C

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

MICROCIRCUIT, DIGITAL-LINEAR, 2x2 LVDS CROSSPOINT SWITCH, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-11242** |

SHEET 1 OF 18

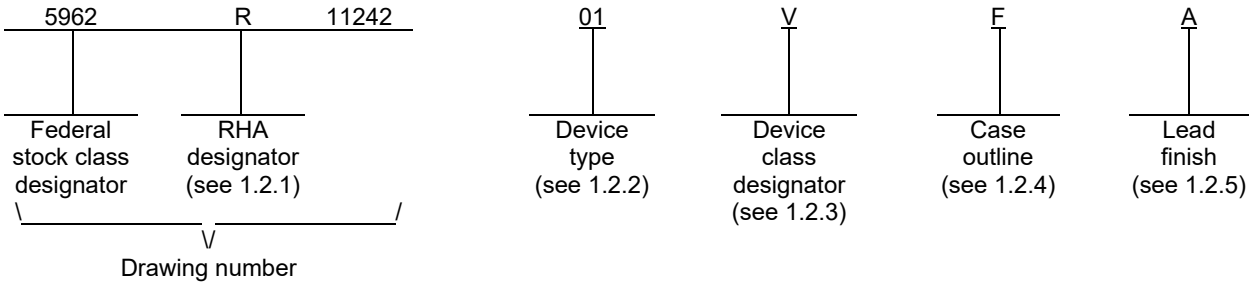
DSCC FORM 2233
APR 97

5962-E173-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | SN55LVCP22-SP | 2x2 LVDS crosspoint switch |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| F | GDFP2-F16 | 16 | Flat pack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | -0.5 V to 4 V 2/ |
| CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1) | -0.5 V to 4 V |
| LVDS receiver input voltage (IN+, IN-) | -0.7 V to 4.3 V |
| LVDS driver output voltage (OUT+, OUT-) | -0.5 V to 4.0 V |
| LVDS output short circuit current | Continuous |
| Storage temperature range | -65°C to 125°C |
| Junction temperature | +150°C |
| Power dissipation ($P_D$) | 313 mW 3/ |
| Thermal resistance, junction-to-ambient ($\theta_{JA}$) | 118.1°C/W |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | 51.2°C/W |
| Maximum lead temperature (soldering 10 seconds) | 300°C |
| Electrostatic discharge (ESD) classification: | |
| Human body model (HBM) | 5000 V |
| Charged-device mode (CDM) | 500V |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 3 V to 3.6 V |
| Receiver input voltage | 0 V to 4 V |
| Operating case Temperature, range ($T_C$) | -55°C to +125°C |
| Magnitude of differential input voltage $\lvert V_{ID} \rvert$ | 0.1 V to 3V |

1.5 Radiation features.

| | |
|---|---|
| Maximum total dose available (high dose rate = 50-300 rad(Si)/s) | 100 krad(Si) 4/ |
| Heavy ion Single event phenomenon (SEP) test: | |
| No SEL occurs at effective LET (see 4.4.4) | ≤ 75 MeV·cm$^2$/mg 5/ |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.

3/ Test conditions: $V_{CC}$ = 3.6 V, $T_A$=125°C, 1Gbps.

4/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1. Post irradiation electrical parametric limits falls within the spec limits during electrical measurement. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si). This part has been characterized and tested at low dose rate condition D, for details please contact manufacturer.

5/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Gold (Au) ion beam was used at an angles of incidence of 44° at flux of $10^5$ ions/cm$^2$·s, fluence level of $10^7$ ions/cm$^2$ and a temperature of 125°C. After run, no single event latch-up (SEL) was observed at an effective LET of 75 MeV·cm$^2$/mg. For more information on SEE/SEP test please contact device manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Function table. The function table shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_C \le +125°C$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| CMOS/TTL DC SPECIFICATION (EN0, EN1, SEL0, SEL1) | | | | | | | |
| High-level input voltage | $V_{IH}$ | | 1, 2, 3 | 01 | 2 | $V_{CC}$ | V |
| Low-level input voltage | $V_{IL}$ | | 1, 2, 3 | 01 | GND | 0.8 | V |
| High-level input current | $I_{IH}$ | $V_{IN}$ = 3.6 V or 2.0 V,<br>$V_{CC}$ = 3.6 V | 1, 2, 3 | 01 | | ±25 | µA |
| Low-level input current | $I_{IL}$ | $V_{IN}$ = 0.0 V or 0.8 V,<br>$V_{CC}$ = 3.6 V | 1, 2, 3 | 01 | | ±15 | µA |
| Input clamp voltage | $V_{CL}$ | $I_{CL}$ = -18mA | 1, 2, 3 | 01 | | -1.5 | V |
| LVDS OUTPUT SPECIFICATION (OUT0, OUT1) | | | | | | | |
| Differential output voltage | $\lvert V_{OD} \rvert$ | $R_L$ = 75Ω, See figure 3 | 1, 2, 3 | 01 | 255 | 475 | mV |
| | | $R_L$ = 75Ω, $V_{CC}$ = 3.3 V,<br>$T_A$ = 25°C, See figure 3 | 1 | 01 | 285 | 440 | |
| Change in differential output voltage magnitude between states | $\Delta\lvert V_{OD} \rvert$ | $V_{ID}$ = ± 100mV, See figure 3 | 1, 2, 3 | 01 | -25 | 25 | mV |
| Steady-state offset voltage | $V_{OS}$ | See Figure 4 | 1, 2, 3 | 01 | 1 | 1.45 | V |
| Change in steady-state offset voltage between logic states | $\Delta V_{OS}$ | See Figure 4 | 1, 2, 3 | 01 | -25 | 25 | mV |
| High-impedance output current | $I_{OZ}$ | $V_{OUT}$ = GND or $V_{CC}$ | 1, 2, 3 | 01 | | ±15 | µA |
| Power-off leakage current | $I_{OFF}$ | $V_{CC}$ = 0 V, 1.5 V;<br>$V_{OUT}$ = 3.6 V or GND | 1, 2, 3 | 01 | | ±15 | µA |
| Output short-circuit current | $I_{OS}$ | $V_{OUT}$ + or $V_{OUT}$- = 0 V | 1, 2, 3 | 01 | | -8 | mA |
| Both outputs short-circuit current | $I_{OSB}$ | $V_{OUT}$ + and $V_{OUT}$- = 0 V | 1, 2, 3 | 01 | -8 | 8 | mA |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| LVDS RECIEVER DC SPECIFICATION (IN0, IN1) | | | | | | | |
| Positive-going differential input voltage threshold | $V_{TH}$ | See table IC | 1, 2, 3 | 01 | | 100 | mV |
| Negative-going differential input voltage threshold | $V_{TL}$ | See table IC | 1, 2, 3 | 01 | -100 | | mV |
| Differential input voltage hysteresis | $V_{ID}$ (HYS) | | 1, 2, 3 | | | 150 | mV |
| Common-mode voltage range | $V_{CMR}$ | $V_{ID}$ = 100mV, $V_{CC}$ = 3.0 V to 3.6 V | 1,2,3 | 01 | .05 | 3.95 | V |
| Input current | $I_{IN}$ | $V_{IN}$ = 4 V, $V_{CC}$ = 3.6 V or 0.0 V | 1, 2, 3 | 01 | | ±18 | µA |
| | | $V_{IN}$ = 0 V, $V_{CC}$ = 3.6 V or 0.0 V | 1, 2, 3 | 01 | | ±18 | |
| SUPPLY CURRENT | | | | | | | |
| Quiescent supply current | $I_{CCQ}$ | $R_L$ = 75Ω, ENO = EN1 = High | 1, 2, 3 | 01 | | 87 | mA |
| Total supply current | $I_{CCD}$ | $R_L$ = 75Ω, $C_L$ = 5 pF, 500 MHz(1000 Mbps), EN0 = EN1 = High | 1, 2, 3 | 01 | | 87 | mA |
| Three state supply current | $I_{CCZ}$ | EN0 = EN1 = Low | 1, 2, 3 | 01 | | 35 | mA |
| Functional test | | See 4.4.1b | 7,8 | 01 | | | |
| SWITCHING CHARACTERISTICS | | | | | | | |
| Input to SEL setup time | $t_{SET}$ | See figure 5 | 9, 10, 11 | | 2.2 | | ns |
| Input to SEL hold time | $t_{HOLD}$ | See figure 5 | 9, 10, 11 | 01 | 2.2 | | ns |
| SEL to switched output | $t_{SWITCH}$ | See figure 5 | 9, 10, 11 | 01 | | 2.6 | ns |
| Disable time, high-level-to-high-impedance | $t_{PHZ}$ | See figure 6 | 9, 10, 11 | 01 | | 4 | ns |
| Disable time, low-level-to-high-impedance | $t_{PLZ}$ | See figure 6 | 9, 10, 11 | 01 | | 4 | ns |
| Enable time, high-impedance-to-high-level output | $t_{PZH}$ | See Figure 6 | 9, 10, 11 | 01 | | 4 | ns |
| Enable time, high-impedance-to-low-level output | $t_{PZL}$ | See Figure 6 | 9, 10, 11 | 01 | | 8 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| SWITCHING CHARACTERISTICS – continued. | | | | | | | |
| Differential output signal rise time (20%-80%) 2/ | $t_{LHT}$ | $C_L$ = 5 pF, see Figure 7 | 9, 10, 11 | 01 | | 620 | ps |
| Differential output signal fall time (20%-80%) 2/ | $t_{HLT}$ | $C_L$ = 5 pF, See Figure 7 | 9, 10, 11 | 01 | | 620 | ps |
| Propagation delay time, low-to-high level output 2/ | $t_{PLHD}$ | | 9, 10, 11 | 01 | 200 | 2350 | ps |
| Propagation delay time, high-to-low-level output 2/ | $t_{PHLD}$ | | 9, 10, 11 | 01 | 200 | 2350 | ps |
| Pulse skew ($\lvert t_{PLHD}-t_{PHLD} \rvert$) 3/, 4/ | $t_{skew}$ | $C_L$ = 5 pF, See Figure 7 | 9, 10, 11 | 01 | | 160 | ps |
| Added peak-to-peak jitter | $t_{JIT}$ | $V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 50 MHz, $C_L$ = 5pF | 9, 10, 11 | 01 | | 22.2 | ps |
| | | $V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 240 MHz, $C_L$ = 5pF | 9, 10, 11 | 01 | | 24.5 | |
| | | $V_{ID}$ = 200 mV, 50% duty cycle $V_{CM}$ = 1.2 V, 500 MHz, $C_L$ = 5 pF | 9, 10, 11 | 01 | | 35.7 | |
| | | $V_{ID}$ = 200 mV, PRBS = $2^{15}$-1 data pattern, $V_{CM}$ = 1.2 V, 240 Mbps, CL = 5 pF | 9, 10, 11 | 01 | | 204 | |
| | | $V_{ID}$ = 200 mV, PRBS = $2^{15}$-1 data pattern, $V_{CM}$ = 1.2 V, 1000 Mbps, $C_L$ = 5 pF | 9, 10, 11 | 01 | | 282 | |
| Added random jitter (rms) | $t_{JMS}$ | $V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 50 MHz, $C_L$ = 5 pF | 9, 10, 11 | 01 | | 1.5 | $PS_{RMS}$ |
| | | $V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 240 MHz, $C_L$ = 5 pF | 9, 10, 11 | 01 | | 1.53 | |
| | | $V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 500 MHz, $C_L$ = 5 pF | 9, 10, 11 | 01 | | 1.79 | |
| Maximum operating frequency 3/, 5/ | $f_{MAX}$ | | 4, 5, 6 | 01 | 1 | | GHz |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C (see 1.5 herein).

2/ Input: $V_{IC}$ = 1.2 V, $V_{ID}$ = 200 mV, 50% duty cycle, 1 MHz, $t_r/t_f$ = 500 ps.

3/ Pulse skew and $f_{MAX}$ parameters are guaranteed by characterization, but not production tested.

4/ $t_{skew}$ is the magnitude of the time difference between the $t_{PLHD}$ and $t_{PHLD}$ of any output of a single device.

5/ Signal generator conditions: 50% duty cycle, $t_r$ or $t_f \leq$ 100 ps (10% to 90%), transmitter output criteria: Duty cycle = 45% to 55% $V_{OD} \geq$ 300 mV.

TABLE IB. SEP test limits. 1/ 2/ 3/

| Device type | SEP | Temperature | Bias $V_{DD=}$ 3.45V<br>No SEL and SEFI were observed at effective LET |
|---|---|---|---|
| 01 | No SEL | 125°C | LET ≤ 75 MeV/(mg/cm$^2$) |

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Gold (Au) ion beam was used at an angles of incidence of 44° at flux of $10^5$ ions/cm$^2$·s, fluence level of $10^7$ ions/cm$^2$ and a temperature of 125°C. After run, no single event latch-up (SEL) and Single event functional interrupt (SEFI) were observed at an effective LET of 75 MeV·cm$^2$/mg. For more information on SEE/SEP test please contact device manufacturer.

Table IC. Reciever Input voltage threshold test.

| Applied Voltages | | Resulting differential Input Voltage | Resulting Common-Mode input Voltage | Output 1/ |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ | |
| 1.25 V | 1.15 V | 100mV | 1.2 V | H |
| 1.15 V | 1.25 | -100mV | 1.2 V | L |
| 4.0 V | 3.9 V | 100 mV | 3.95 V | H |
| 3.9 V | 4.0 V | -100 mV | 3.95 V | L |
| 0.1 V | 0.0 V | 100 mV | 0.05 V | H |
| 0.0 V | 0.1 V | -100 mV | 0.05 | L |
| 1.7 V | 0.7 V | 1000 mV | 1.2 V | H |
| 0.7 V | 1.7 V | -1000 mV | 1.2 V | L |
| 4.0 V | 3.0 V | 1000 mV | 3.5 V | H |
| 3.0 V | 4.0 V | -1000 mV | 3.5 V | L |
| 1.0 V | 0.0 V | 1000 mV | 0.5 V | H |
| 0.0 V | 1.0 V | -1000 mV | 0.5 V | L |

1/ H = High level, L = low level.

| Device type | 01 |
|---|---|
| Case outline | F |
| Terminal number | Terminal symbol |
| 1 | SEL1 |
| 2 | SEL0 |
| 3 | IN0+ |
| 4 | IN0- |
| 5 | Vcc |
| 6 | IN1+ |
| 7 | IN1- |
| 8 | NC |
| 9 | NC |
| 10 | OUT1- |
| 11 | OUT1+ |
| 12 | GND |
| 13 | OUT0- |
| 14 | OUT0+ |
| 15 | EN1 |
| 16 | EN0 |

NC = No internal connection

FIGURE 1. Terminal connections.

| SEL0 | SEL1 | OUT0 | OUT1 | Mode |
|---|---|---|---|---|
| 0 | 0 | IN0 | IN0 | 1:2 splitter |
| 0 | 1 | IN0 | IN1 | Repeater |
| 1 | 0 | IN1 | IN0 | Switch |
| 1 | 1 | IN1 | IN1 | 1:2 splitter |

FIGURE 2. Function table.

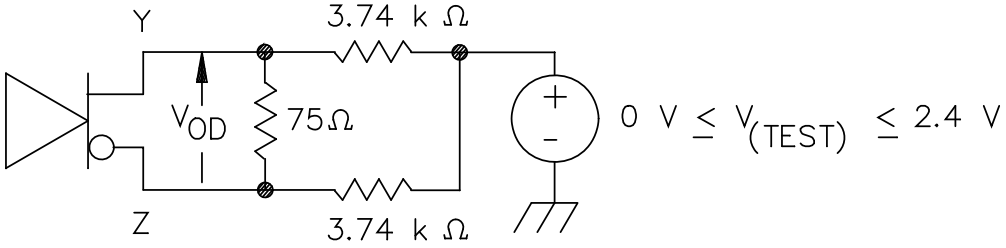
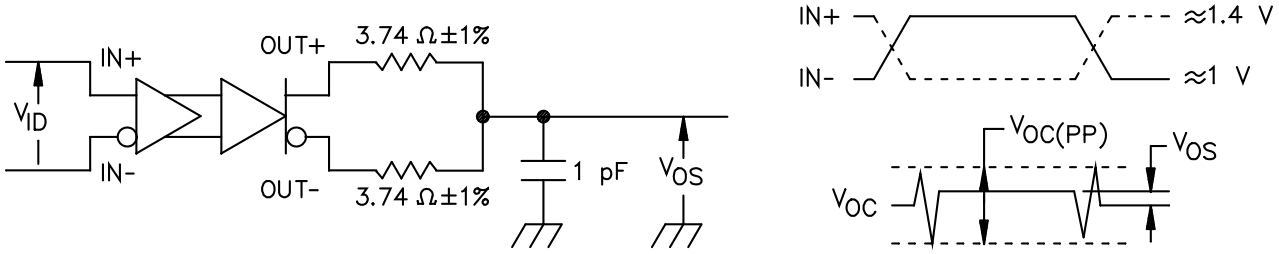



Figure 3. Differential output voltage ($V_{OD}$) test circuit.




Note: All input pulses are supplied by a generator having the following characteristics $t_r$ or $t_f$ ≤ 1 ns, Pulse-repetition rate (PRR) = 0.5 Mbps, pulse width = 500 ± 10 ns; $R_L$ = 100Ω; $C_L$ includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 db bandwidth of at least 300 MHz.

Figure 4. Test circuit and definition for the driver common-mode output voltage.

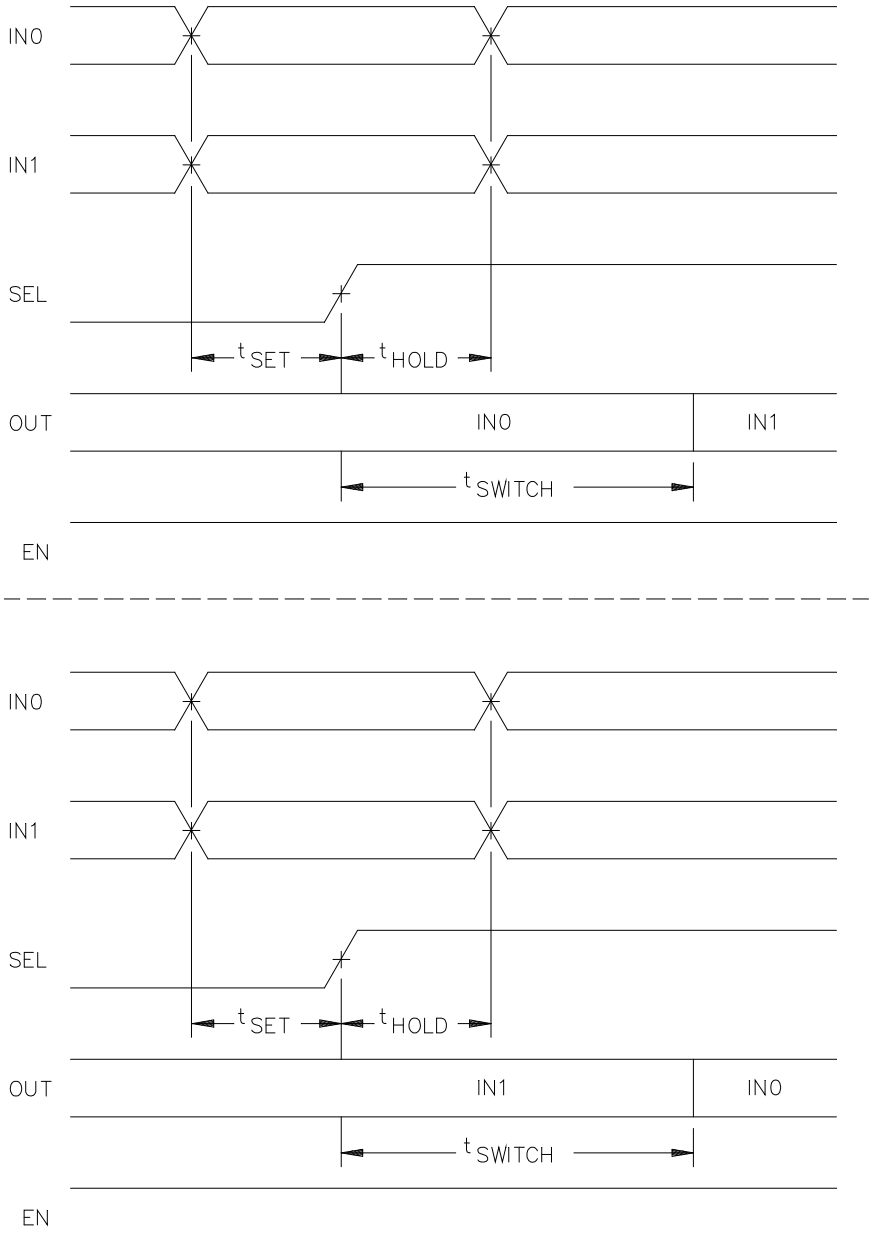



FIGURE 5. Input to select for both rising and falling edge setup and hold times.

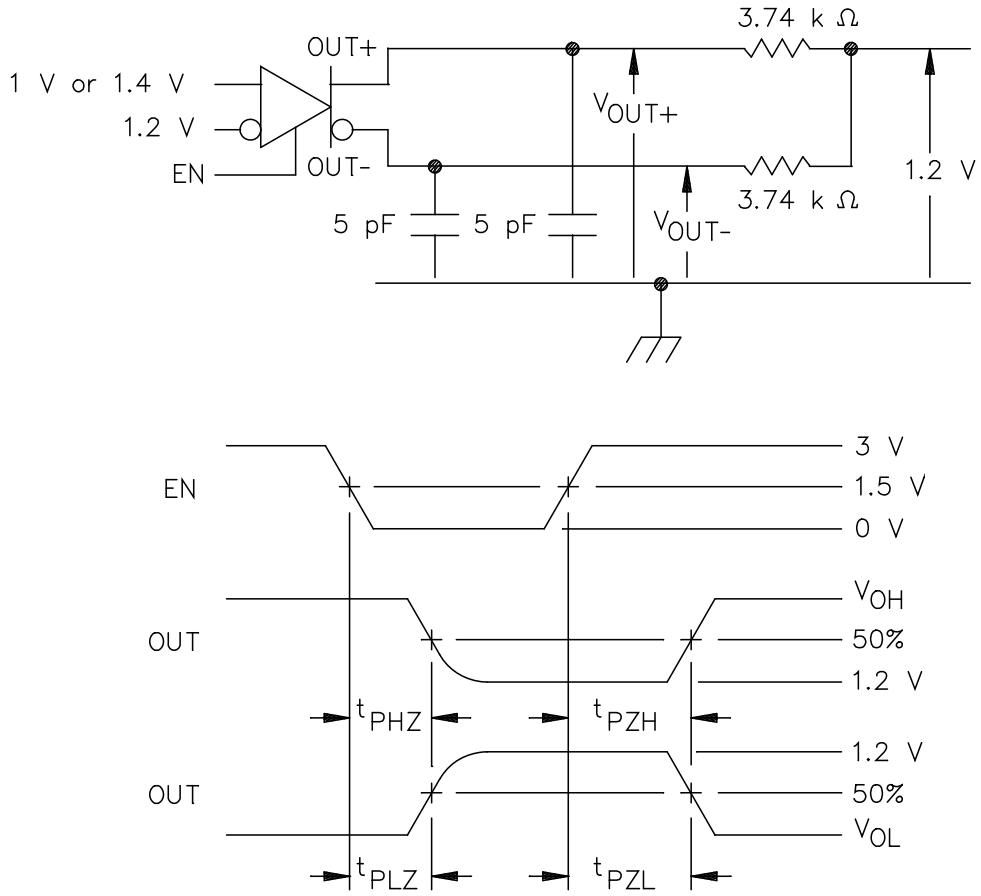



FIGURE 6. Enable and disable test circuit and waveforms.

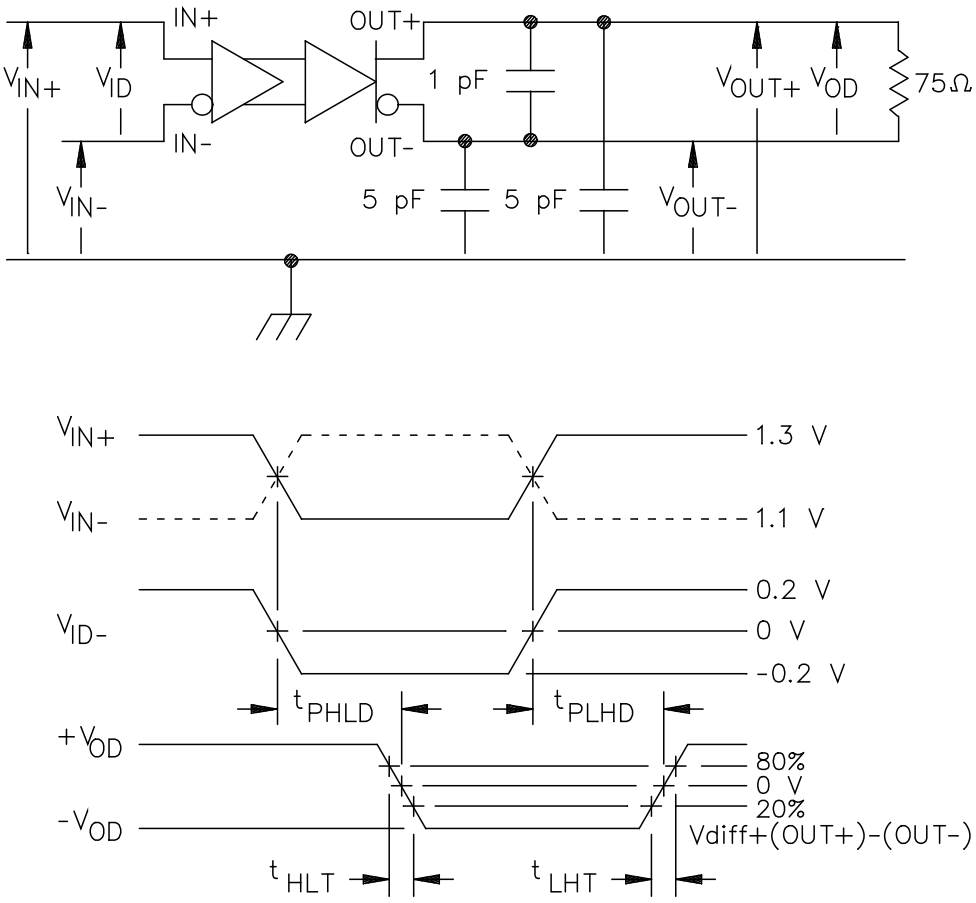



Figure 7. Timing test circuit and waveforms.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the function table.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ $10^7$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/cm$^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be $T_J$=125°C for SEL test.

f. For SEL test limits, see table IB herein.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1, 7, 9 | 1, 7, 9 |
| Final electrical parameters (see 4.2) | 1, 2, 3, 7, 8, 9, 10, 11 1/ | 1, 2, 3, 7, 8, 9, 10, 11 1/, 2/ |
| Group A test requirements (see 4.4) | 1, 2, 3, 7, 8, 9, 10, 11 | 1, 2, 3, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 2/ |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 |
| Group E end-point electrical parameters (see 4.4) | --- | 1, 2, 3 |

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified and the delta limits shall be computed with reference to the zero hour electrical parameters.

Table IIB. Burn-in and operating life test delta parameters. (+25°C) 1/

| Parameters 1/ | Delta Limits |
|---|---|
| Total quiescent supply current, $I_{CCQ}$ | -/+ 1.5 mA |
| Three state supply current, $I_{CCZ}$ | -/+ 0.5 mA |
| High-level input current, $I_{IH}$ | -/+ 300 nA |
| Low-level input current, $I_{IL}$ | -/+ 200 nA |
| Steady-state offset voltage, $V_{OS}$ | -/+ 50 mV |

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-02-04

Approved sources of supply for SMD 5962-11242 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-1124201QFA | 01295 | SN55LVCP22W |
| 5962-1124201VFA | 01295 | SN55LVCP22W-SP |
| 5962R1124201VFA | 01295 | SN55LVCP22AW-SP-RHA |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>PO Box 660199<br>Dallas, TX 75243 |