REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20														
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Greg Cecil

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
15-05-20

REVISION LEVEL

MICROCIRCUIT, HYBRID, CMOS, LINEAR, ANALOG MULTIPLEXER, 64 CHANNEL, +3.3 TO +5 VOLT

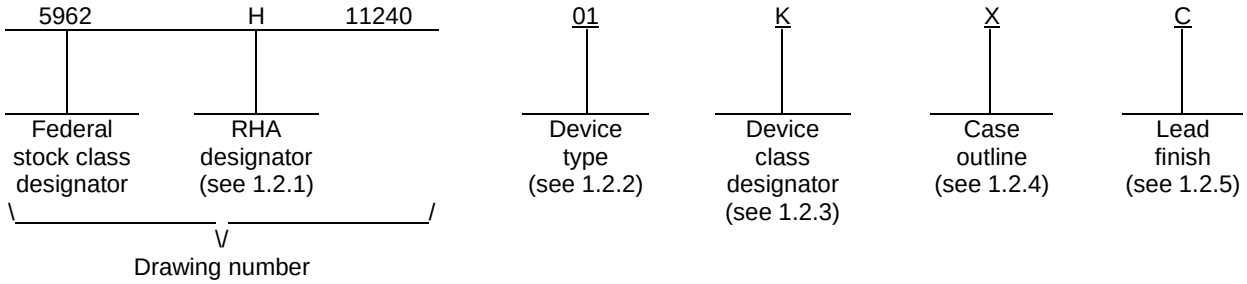
SIZE	CAGE CODE	
A	**67268**	**5962-11240**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHD8540	64 channel analog multiplexer, 32 channels voltage, 32 channels voltage and current
02	RHD8541	64 channel analog multiplexer

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	96	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+7.0 V dc
Digital input overvoltage range (V_{EN} ,$V_{A)}$	(< V_{CC} + .4)V, (> GND - .4)V
Analog input overvoltage range	(< V_{CC} + .4)V, (> GND - .4)V
Power dissipation (P_D):	
Device type 01	33.6 mW
Device type 02	22.4 mW
Thermal resistance junction-to-case (θ_{JC})	10°C/W
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+3.0 V to +5.5 V dc
Maximum logic low level input voltage	.3 V_{CC}
Minimum logic high level input voltage	.7 V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features. 2/

Maximum Total Ionizing Dose (TID) ..(dose rate = 50 - 300 rad(Si)/s):	
In accordance with MIL-STD-883, method 1019, condition A.	1 Mrad(Si)
Enhanced Low Dose Rate Sensitivity (ELDRS)	3/
Single Event Latchup (SEL)	> 100 MeV-cm^2/mg 4/
Neutron Displacement Damage (> 1 x 10^{14} neutrons/cm^2)	3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ See section 4.3.5 for the manufacturer's radiation hardness assurance analysis and testing.
3/ Not tested, Immune by 100 percent CMOS technology.
4/ Single Event Latchup (SEL) immunity is accomplished by double, fully enclosing, guard rings in the CMOS design layout. The guard rings eliminate the parasitic pnpn structure that is responsible for latchup in CMOS circuits. This limit is guaranteed by design or process, but not tested.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Switching test waveform(s). The switching test waveform(s) shall be as specified on figure 4.

3.2.5 Block diagram. The block diagram(s) shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = +5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply currents 1/	$+I_{CC}$	V_{EN} = .3 V_{CC}	1,2,3	01		4.8	mA
				02		3.2	
	$+I_{SBY}$	V_{EN} = .7 V_{CC}	1,2,3	01		1.2	mA
				02		800	µA
Address input 1/ currents	I_{AL} (A0-A3)	V_A = .3 V_{CC}	1	01	-20	20	nA
			2		-200	200	
			1	02	-10	10	nA
			2		-100	100	
	I_{AL} (B0-B3)		1	01,02	-10	10	nA
			2		-100	100	
	I_{AH} (A0-A3)	V_A = .7 V_{CC}	1	01	-20	20	nA
			2		-200	200	
			1	02	-10	10	nA
			2		-100	100	
	I_{AH} (B0-B3)		1	01,02	-10	10	nA
			2		-100	100	
Enable input 1/ currents ($\overline{EN}$)	I_{ENL} $\overline{EN}$(0-15) $\overline{EN}$(16-31)	V_A = .3 V_{CC}	1	01,02	-5	5	nA
			2		-50	50	
	I_{ENL} $\overline{EN}$(32-47) $\overline{EN}$(48-63)		1	01	-10	10	nA
			2		-100	100	
			1	02	-5	5	nA
			2		-50	50	
	I_{ENH} $\overline{EN}$(0-15) $\overline{EN}$(16-31)	V_A = .7 V_{CC}	1	01,02	-5	5	nA
			2		-50	50	
	I_{ENH} $\overline{EN}$(32-47) $\overline{EN}$(48-63)		1	01	-10	10	nA
			2		-100	100	
			1	02	-5	5	nA
			2		-50	50	
Input leakage current (CH0-CH15) 1/	I_{INLK5}	V_{IN} = +5 V, V_{EN} = .7 V_{CC}, output and all unused MUX inputs under test = 0 V	1	01,02	-5	5	nA
			2		-50	50	
	I_{INLK0}	V_{IN} = 0 V, V_{EN} = .7 V_{CC}, output and all unused MUX inputs under test = +5 V	1	01,02	-5	5	nA
			2		-50	50	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = +5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output leakge current (V_{OUT}) 1/	I_{OUTLK}	V_{OUT} = +5 V, V_{EN} = .7 V_{CC}, All inputs grounded except channel being tested	1	01,02	-5	5	nA
			2		-50	50	
Switch ON 1/ resistance	R_{DSON}	V_{IN} = 0 V, V_{EN} = .3 V_{CC}, I_{OUT} = +1 mA	1	01,02		750	Ω
			2			1000	
			3			500	
		V_{IN} = +2.5 V, V_{EN} = .3 V_{CC}, I_{OUT} = -0.6 mA	1			750	
			2			1000	
			3			500	
		V_{IN} = +5 V, V_{EN} = .3 V_{CC}, I_{OUT} = -1 mA	1			750	
			2			1000	
			3			500	
Address to output delay	t_AHL	R_L = 10 kΩ, C_L = 50 pF, See figure 4	9,11	01,02	10	150	ns
			10		10	200	
	t_ALH	R_L = 10 kΩ, C_L = 50 pF, See figure 4	9,11	01,02	10	150	ns
			10		10	200	
Enable to output delay	$t_{ON}EN$	R_L = 1 kΩ, C_L = 50 pF, See figure 4	9,11	01,02	10	150	ns
			10		10	200	
	$t_{OFF}EN$	R_L = 1 kΩ, C_L = 50 pF, See figure 4	9,10,11	01,02	10	200	ns

1/ These devices have been tested to (1 Mrad(Si)) to Method 1019, condition A of MIL-STD-883 at +25°C for these parameters to assure the requirements of RHA designator level "H" (1Mrad(Si)) are met.

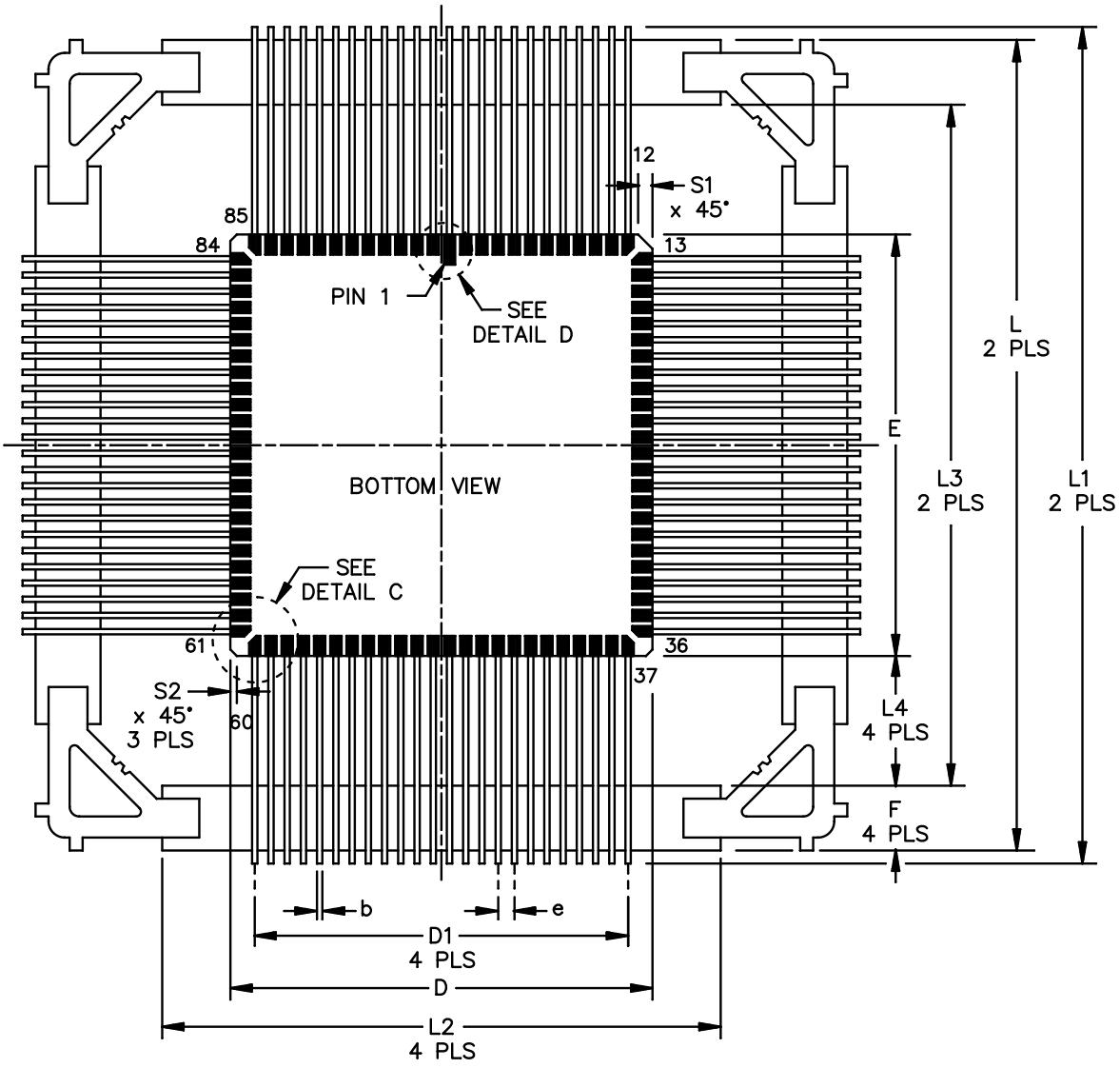


FIGURE 1. Case outline.

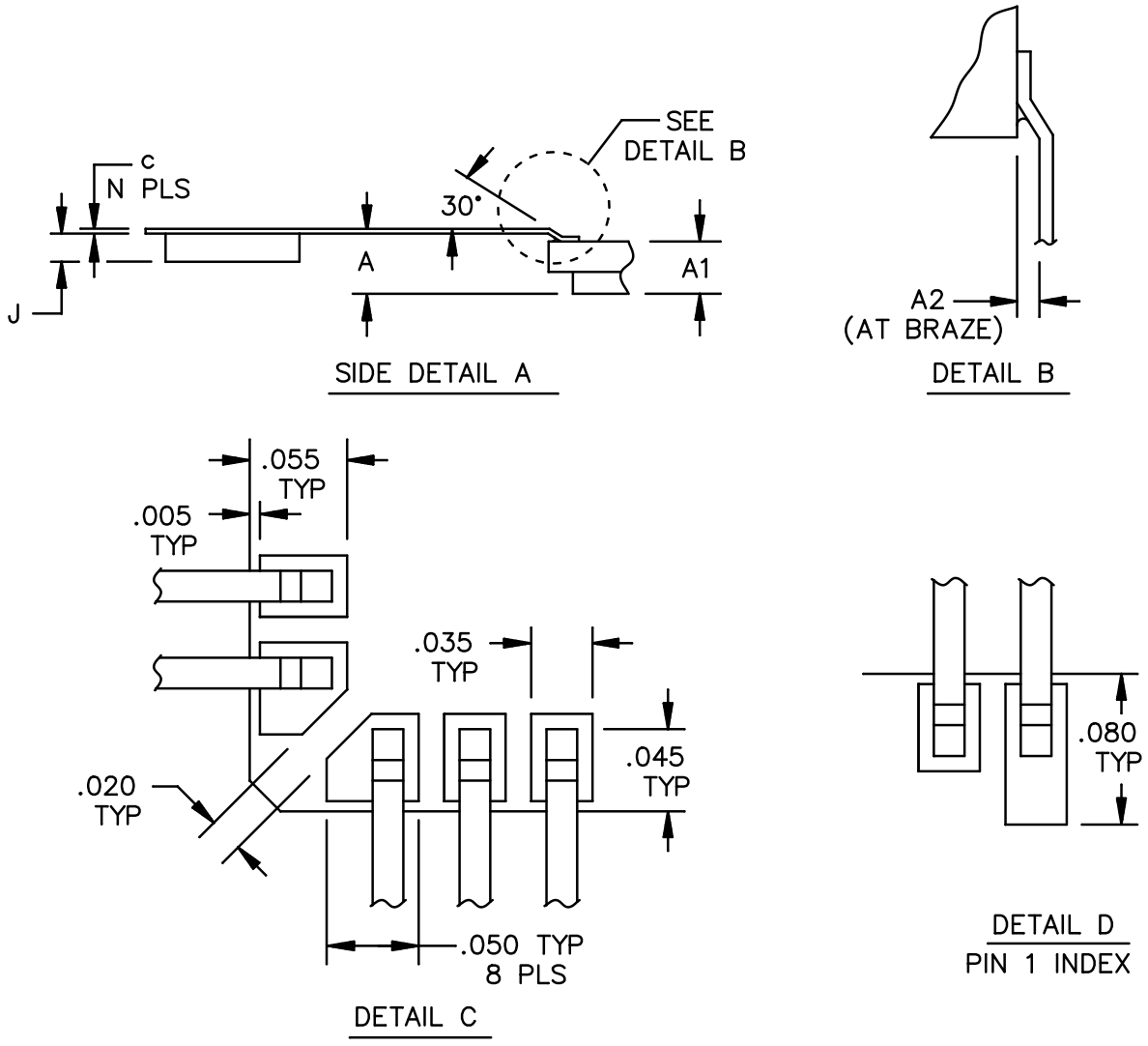


FIGURE 1. Case outline(s) - Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
A1		.180		4.57
A2	.005	.011	0.13	0.28
b	.0135	.0195	0.34	0.50
c	.005	.008	0.13	0.20
D/E	1.287	1.313	32.69	33.35
D1	1.145	1.155	29.08	29.34
e	.050 BSC		1.27 BSC	
F	.200 TYP		5.08 TYP	
J	.035 TYP		0.89 TYP	
L	2.490	2.510	63.25	63.75
L1		2.580		65.53
L2	1.700	1.740	43.18	44.20
L3	2.090	2.110	53.09	53.59
L4	.400 TYP		10.16 TYP	
N	96		96	
S1	.030 TYP		0.76 TYP	
S2	.015 TYP		0.38 TYP	

NOTES:
1. Pin 1 is indicated by an ESD triangle on top of the package and by an index on the bottom of the package.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. N equals 96, the total number of leads on the package.
4. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	OUTPUT I(48-63)
4	B3	36	CH28	68	OUTPUT V(48-63)
5	$\overline{EN}$(0-15)	37	CH13	69	OUTPUT I(32-47)
6	$\overline{EN}$(16-31)	38	CH29	70	OUTPUT V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	V_{CC}	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	NC	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	NC	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	Case GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	OUTPUT V(0-15)	57	CH57	89	GND
26	OUTPUT V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$(48-63)
28	CH24	60	CH54	92	$\overline{EN}$(32-47)
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

NOTE: NC is a no connect pin. NC pins should be grounded to eliminate or minimize electrostatic discharge (ESD) or static buildup.

FIGURE 2. Terminal connections.

Device type	02				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	NC
4	B3	36	CH28	68	OUTPUT V(48-63)
5	$\overline{EN}$(0-15)	37	CH13	69	NC
6	$\overline{EN}$(16-31)	38	CH29	70	OUTPUT V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	V_{CC}	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	NC	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	NC	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	Case GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	OUTPUT V(0-15)	57	CH57	89	GND
26	OUTPUT V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$(48-63)
28	CH24	60	CH54	92	$\overline{EN}$(32-47)
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

NOTE: NC is a no connect pin. NC pins should be grounded to eliminate or minimize electrostatic discharge (ESD) or static buildup.

FIGURE 2. Terminal connections - Continued.

Truth table (CH0-CH15) and (CH16-CH31)							
B3	B2	B1	B0	$\overline{EN}$(0-15)	"ON" Channel 1/	$\overline{EN}$(16-31)	"ON" Channel 2/
X	X	X	X	H	None	H	None
L	L	L	L	L	CH0	L	CH16
L	L	L	H	L	CH1	L	CH17
L	L	H	L	L	CH2	L	CH18
L	L	H	H	L	CH3	L	CH19
L	H	L	L	L	CH4	L	CH20
L	H	L	H	L	CH5	L	CH21
L	H	H	L	L	CH6	L	CH22
L	H	H	H	L	CH7	L	CH23
H	L	L	L	L	CH8	L	CH24
H	L	L	H	L	CH9	L	CH25
H	L	H	L	L	CH10	L	CH26
H	L	H	H	L	CH11	L	CH27
H	H	L	L	L	CH12	L	CH28
H	H	L	H	L	CH13	L	CH29
H	H	H	L	L	CH14	L	CH30
H	H	H	H	L	CH15	L	CH31

1/ Between (CH0-CH15) and OUTPUT(0-15).
2/ Between (CH16-CH31) and OUTPUT(16-31).

Truth table (CH32-CH47) and (CH48-CH63)							
A3	A2	A1	A0	$\overline{EN}$(32-47)	"ON" Channel 1/	$\overline{EN}$(48-63)	"ON" Channel 2/
X	X	X	X	H	None	H	None
L	L	L	L	L	CH32	L	CH48
L	L	L	H	L	CH33	L	CH49
L	L	H	L	L	CH34	L	CH50
L	L	H	H	L	CH35	L	CH51
L	H	L	L	L	CH36	L	CH52
L	H	L	H	L	CH37	L	CH53
L	H	H	L	L	CH38	L	CH54
L	H	H	H	L	CH39	L	CH55
H	L	L	L	L	CH40	L	CH56
H	L	L	H	L	CH41	L	CH57
H	L	H	L	L	CH42	L	CH58
H	L	H	H	L	CH43	L	CH59
H	H	L	L	L	CH44	L	CH60
H	H	L	H	L	CH45	L	CH61
H	H	H	L	L	CH46	L	CH62
H	H	H	H	L	CH47	L	CH63

1/ Between (CH32-CH47) and OUTPUT(32-47) and CURRENT(32-47).
2/ Between (CH48-CH63) and OUTPUT(48-63) and CURRENT(48-63).

FIGURE 3. Truth table(s). (Device type 01)

Truth table (CH0-CH15) and (CH16-CH31)							
B3	B2	B1	B0	$\overline{EN}$(0-15)	"ON" Channel 1/	$\overline{EN}$(16-31)	"ON" Channel 2/
X	X	X	X	H	None	H	None
L	L	L	L	L	CH0	L	CH16
L	L	L	H	L	CH1	L	CH17
L	L	H	L	L	CH2	L	CH18
L	L	H	H	L	CH3	L	CH19
L	H	L	L	L	CH4	L	CH20
L	H	L	H	L	CH5	L	CH21
L	H	H	L	L	CH6	L	CH22
L	H	H	H	L	CH7	L	CH23
H	L	L	L	L	CH8	L	CH24
H	L	L	H	L	CH9	L	CH25
H	L	H	L	L	CH10	L	CH26
H	L	H	H	L	CH11	L	CH27
H	H	L	L	L	CH12	L	CH28
H	H	L	H	L	CH13	L	CH29
H	H	H	L	L	CH14	L	CH30
H	H	H	H	L	CH15	L	CH31

1/ Between (CH0-CH15) and OUTPUT(0-15).
2/ Between (CH16-CH31) and OUTPUT(16-31).

Truth table (CH32-CH47) and (CH48-CH63)							
A3	A2	A1	A0	$\overline{EN}$(32-47)	"ON" Channel 1/	$\overline{EN}$(48-63)	"ON" Channel 2/
X	X	X	X	H	None	H	None
L	L	L	L	L	CH32	L	CH48
L	L	L	H	L	CH33	L	CH49
L	L	H	L	L	CH34	L	CH50
L	L	H	H	L	CH35	L	CH51
L	H	L	L	L	CH36	L	CH52
L	H	L	H	L	CH37	L	CH53
L	H	H	L	L	CH38	L	CH54
L	H	H	H	L	CH39	L	CH55
H	L	L	L	L	CH40	L	CH56
H	L	L	H	L	CH41	L	CH57
H	L	H	L	L	CH42	L	CH58
H	L	H	H	L	CH43	L	CH59
H	H	L	L	L	CH44	L	CH60
H	H	L	H	L	CH45	L	CH61
H	H	H	L	L	CH46	L	CH62
H	H	H	H	L	CH47	L	CH63

1/ Between (CH32-CH47) and OUTPUT(32-47).
2/ Between (CH48-CH63) and OUTPUT(48-63).

FIGURE 3. Truth table(s). (Device type 02)

DEVICE TYPE 01 AND 02

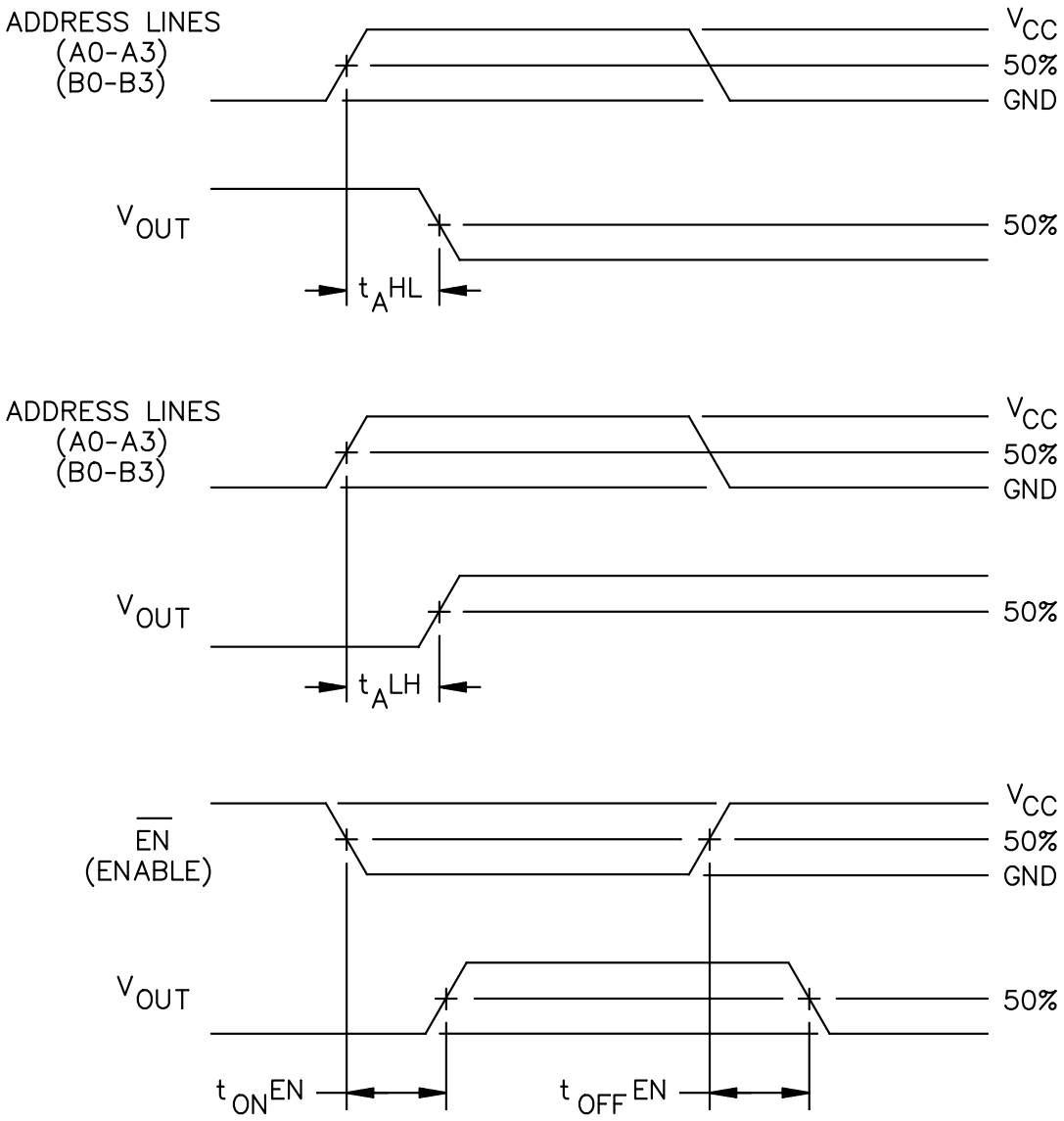


FIGURE 4. Switching test waveform(s).

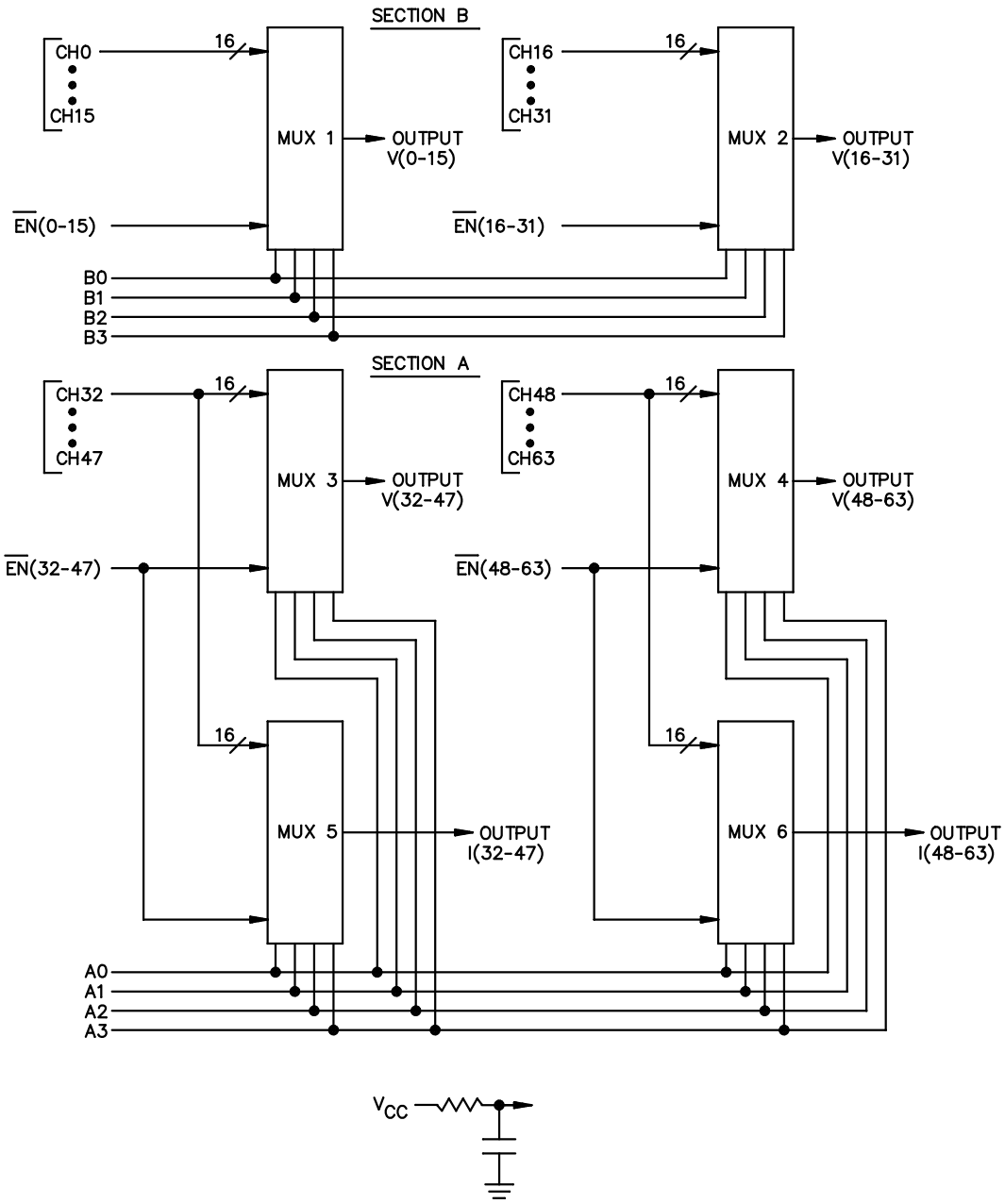


FIGURE 5. Block diagram. (Device Type 01)

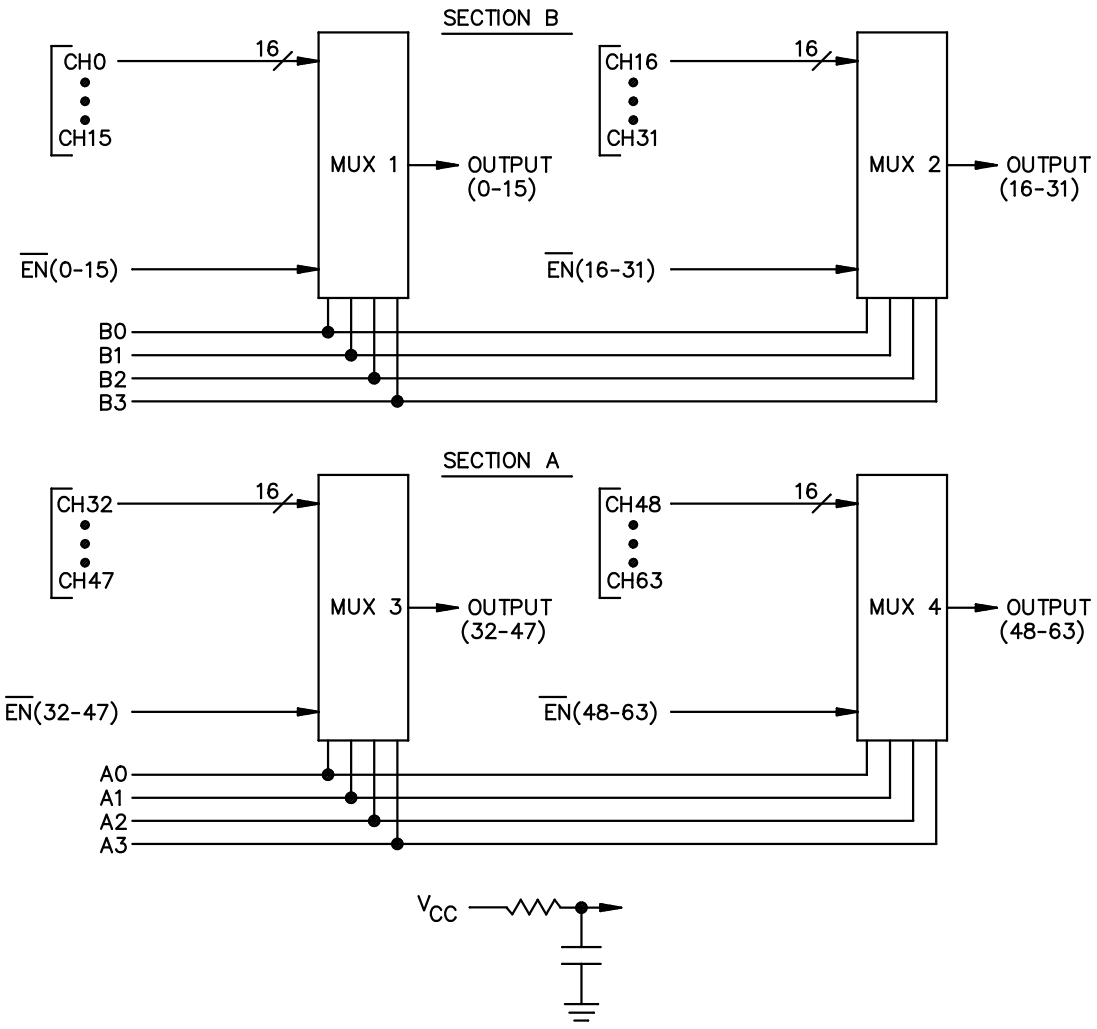


FIGURE 5. Block diagram - Continued. (Device Type 02)

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,9
Final electrical parameters	1*,2,3,9,10,11
Group A test requirements	1,2,3,9,10,11
Group C end-point electrical parameters	1,2,3,9,10,11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	1

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5. Radiation hardness assurance (RHA). RHA qualification is required only for those devices with the RHA designator as specified herein. See table IIIA and table IIIB.

Table IIIA. Radiation Hardness Assurance Method Table.

RHA method employed	**Total Dose Testing RHA level "H" (1 Mrad)**		**Worst Case Analysis Performed**				**End point electricals after total dose**	
	Element level	Hybrid device level	Includes temperature effects	Combines temperature and radiation effects	Combines total dose and displacement effects	End-of-life	Element level	Hybrid device level
	Tested at (1 Mrad)	Tested at (1 Mrad) (See 4.3.5.1.1)	No	No	No	No	T_C = +25°C	T_C = +25°C

Table IIIB. Hybrid level and element level test table.

	Radiation Test								
	Total Dose			**Heavy Ion**		**Proton**		**Neutron**	
	Low Dose Rate (LDR)	High Dose Rate (HDR)	ELDRS	SET (transient)	SEL (latch-up)	Low Energy	High Energy	SEE (upset)	Displacement Damage (DD)
CMOS IC	G	Tested (1 Mrad) (See 4.3.5.1.1)	G	Not Tested	G 100 MeV-cm^2/mg	Not Tested	Not Tested	Not Tested	G

NOTE:
G = Guaranteed by design or process

4.3.5.1 Radiation Hardness Assurance (RHA) inspection. RHA qualification is required for those devices with the RHA designator as specified herein. End-point electrical parameters for radiation hardness assurance (RHA) devices shall be specified in table II. Radiation testing will be in accordance with the qualifying activity (DLA Land and Maritime -VQ) approved plan and with MIL-PRF-38534, Appendix G.

a. The hybrid device manufacturer shall establish procedures controlling component radiation testing, and shall establish radiation test plans used to implement component lot qualification during procurement. Test plans and test reports shall be filed and controlled in accordance with the manufacturer's configuration management system.

b. The hybrid device manufacturer shall designate a RHA program manager to oversee component lot qualification, and to monitor design changes for continued compliance to RHA requirements.

4.3.5.1.1 Hybrid level RHA qualification. Hybrid level and element level testing are the same for the devices on this Standard Microcircuit Drawing (SMD) since the active element is accessible to the device leads for test.

4.3.5.1.1.1 Qualification by similarity. The devices on this SMD contain multiple of a common active element (that are accessible to the package leads for test), therefore the device types on this SMD are considered similar for the purpose of RHA qualification. The part number 5962H1024301KXC was RHA tested, therefore the device types 01 and 02 on this SMD are considered qualified by similarity. The package used for (5962H1024301KXC) is the same package construction and material as this drawing except for size and pin count. Internal Gas Analysis data demonstrates that the hydrogen level between the two packages is negligible.

4.3.5.1.2 Element level qualification.

4.3.5.1.2.1 Total ionizing dose irradiation testing. A minimum of 5 biased devices of the active element used will be tested every wafer lot. These active elements will be tested at HDR in accordance with condition A of method 1019 of MIL-STD-883 to 1 Mrad(Si) for the device parameters as specified in table I herein.

4.3.5.1.2.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.3.5.2. Total Ionizing Dose (TID). See paragraph 4.3.5.1.2.1 and 4.3.5.1.2.1.1 herein.

4.3.5.2.1 Radiation Lot Acceptance Testing (RLAT). Every wafer diffusion lot of integrated circuits used in this hybrid microcircuit device will be Radiation Lot Acceptance Testing (RLAT) tested at HDR in accordance with condition A (dose rate of 50 - 300 rad(Si)/s) of method 1019 of MIL-STD-883. A minimum of 5 samples under worst case biased conditions will be tested. 0.9000/90% statistics are applied to the device parameters as specified in table I herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-05-20

Approved sources of supply for SMD 5962-11240 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE	Vendor similar PIN 2/
5962-1124001KXC 5962H1124001KXC	88379 88379	RHD8540-201-1S RHD8540-901-1S
5962-1124002KXC 5962H1124002KXC	88379 88379	RHD8541-201-1S RHD8541-901-1S

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
88379	Aeroflex Plainview Incorporated, (Aeroflex Microelectronic Solutions) 35 South Service Road Plainview, NY 11803