

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02 and paragraph 4.4.4.1. Add new footnote 2/ to Table I. Under Table I, make two changes to footnote 9/; delete "COMM" and replace with "0 V"; delete "1 μA" and replace with "5 μA". - ro	13-12-04	C. SAFFLE
B	Add Single event phenomenon (SEP) requirements along with paragraphs 2.2, 4.4.4.2, and Table IB. Make change to ENBL limit from 1.25 V rms to V _S under paragraph 1.3. Make correction to pins 8 and 9 terminal symbols under figure 1. - ro	15-06-03	C. SAFFLE
C	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	20-07-14	J. ESCHMEYER



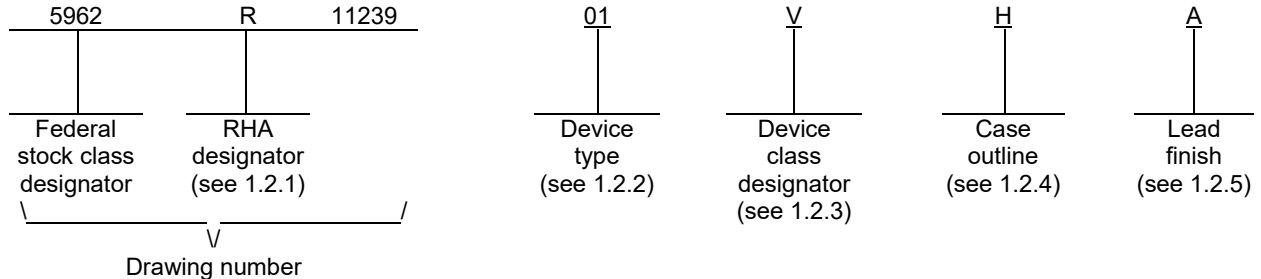
REV																				
SHEET																				
REV	C	C	C	C	C															
SHEET	15	16	17	18	19															
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Dan Wonnell	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Rajesh Pithadia																		
	APPROVED BY Charles F. Saffle	<p align="center">MICROCIRCUIT, LINEAR, POWER DETECTOR, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 13-02-06																		
	REVISION LEVEL C		<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-11239</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-11239													
SIZE A	CAGE CODE 67268	5962-11239																	
		SHEET 1 OF 19																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	ADL5501	Power detector, 50 MHz to 6 GHz
02	ADL5501	Power detector, 50 MHz to 6 GHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
H	GDFP1-F10	10	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 2

1.3 Absolute maximum ratings. 1/

Supply voltage (Vs)	5.5 V
VRMS	0 V - Vs
RFIN	1.25 V rms
ENBL	Vs
Equivalent power, re: 50 Ω	15 dBm
Power dissipation	80 mW
Junction temperature	+140°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-ambient (θJA)	167°C/W 2/
Thermal resistance, junction-to-case (θJC)	146°C/W 2/

1.4 Recommended operating conditions.

Supply voltage range, (Vs)	3.3 V to 5.0 V
Ambient operating temperature range	-55°C to +125°C

1.4.1 Operating performance characteristics. 3/

Input resistance:	
f = 50 MHz	87 Ω
f = 100 MHz	78 Ω
f = 900 MHz	52 Ω
f = 4000 MHz	41 Ω
f = 6000 MHz	86 Ω
Input capacitance:	
f = 50 MHz	6.9 pF
f = 100 MHz	4.2 pF
f = 900 MHz	0.9 pF
f = 4000 MHz	0.1 pF
f = 6000 MHz	0.1 pF
Temperature sensitivity +25°C ≤ TA ≤ +125°C:	
f = 50 MHz	0.0039 dB/°C
f = 100 MHz	0.0028 dB/°C
f = 900 MHz	0.0019 dB/°C
f = 4000 MHz	0.0019 dB/°C
f = 6000 MHz	0.0017 dB/°C
Temperature sensitivity -55°C ≤ TA ≤ +25°C:	
f = 50 MHz	-0.0037 dB/°C
f = 100 MHz	-0.0018 dB/°C
f = 900 MHz	-0.0002 dB/°C
f = 4000 MHz	-0.0043 dB/°C
f = 6000 MHz	-0.0008 dB/°C

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Measurement taken under absolute worst case condition of still air and represents data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package θJC thermal numbers with smaller die size.
- 3/ TA ≤ +25°C, Vs = 5.0 V and 3.3 V, ENBL = Vs, CFLTR = 1nF, COUT = open, unless otherwise specified.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 3

1.4.1 Operating performance characteristics - continued. 3/

Dynamic range (CW input):

f = 50 MHz:

±2.00 dB error, V _S = 3.3 V	32 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 5 V	35 dB	<u>4/</u> , <u>5/</u>

f = 100 MHz:

±0.25 dB error, (delta from +25°C, V _S = 5 V)	28 dB	<u>6/</u> , <u>5/</u>
±0.25 dB error, V _S = 3.3 V	19 dB	<u>4/</u> , <u>5/</u>
±0.25 dB error, V _S = 5 V	20 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 3.3 V	26 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 5 V	30 dB	<u>4/</u> , <u>5/</u>

f = 900 MHz:

±0.25 dB error, (delta from +25°C, V _S = 5 V)	33 dB	<u>6/</u> , <u>5/</u>
±0.25 dB error, V _S = 3.3 V	20 dB	<u>4/</u> , <u>5/</u>
±0.25 dB error, V _S = 5 V	23 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 3.3 V	27 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 5 V	30 dB	<u>4/</u> , <u>5/</u>

f = 4000 MHz:

±0.25 dB error, (delta from +25°C, V _S = 5 V)	5 dB	<u>6/</u> , <u>5/</u>
±0.25 dB error, V _S = 3.3 V	4 dB	<u>4/</u> , <u>5/</u>
±0.25 dB error, V _S = 5 V	5 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 3.3 V	30 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 5 V	33 dB	<u>4/</u> , <u>5/</u>

f = 6000 MHz:

±0.25 dB error, (delta from +25°C, V _S = 5 V)	25 dB	<u>6/</u> , <u>5/</u>
±0.25 dB error, V _S = 3.3 V	20 dB	<u>4/</u> , <u>5/</u>
±0.25 dB error, V _S = 5 V	20 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 3.3 V	35 dB	<u>4/</u> , <u>5/</u>
±2.00 dB error, V _S = 5 V	35 dB	<u>4/</u> , <u>5/</u>

Maximum input level:

f = 50 MHz	8 dBm	<u>4/</u>
f = 100 MHz	6 dBm	<u>4/</u>
f = 900 MHz	6 dBm	<u>4/</u>
f = 4000 MHz	10 dBm	<u>4/</u>
f = 6000 MHz	14 dBm	<u>4/</u>

Minimum input level:

f = 50 MHz	-18 dBm	<u>4/</u>
f = 100 MHz	-18 dBm	<u>4/</u>
f = 900 MHz	-18 dBm	<u>4/</u>
f = 4000 MHz	-18 dBm	<u>4/</u>
f = 6000 MHz	-17 dBm	<u>4/</u>

4/ Error referred to best-fit line at +25°C.

5/ Dynamic range is the ratio of maximum to minimum input level applied to the input to maintain the specified error. It is calculated by $20 \cdot \log(V_{rms_max}/V_{rms_min})$.

6/ Output delta from +25°C. Output voltage at -55°C and +125°C.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 4

1.4.1 Operating performance characteristics - continued. 3/

Enable time (ON):

CFLTR = COUT = ROUT = OPEN, f = 900 MHz, Vs = 3.3 V	9 μs
CFLTR = 1 nF, COUT = ROUT = OPEN, f = 900 MHz, Vs = 3.3 V	42 μs
CFLTR = COUT = ROUT = OPEN, f = 900 MHz, Vs = 5 V	8 μs
CFLTR = 1 nF, COUT = ROUT = OPEN, f = 900 MHz, Vs = 5 V	40 μs

Enable time (OFF):

CFLTR = COUT = ROUT = OPEN, f = 900 MHz, Vs = 3.3 V	16 μs
CFLTR = 1 nF, COUT = ROUT = OPEN, f = 900 MHz, Vs = 3.3 V	17 μs
CFLTR = COUT = ROUT = OPEN, f = 900 MHz, Vs = 5 V	25 μs
CFLTR = 1 nF, COUT = ROUT = OPEN, f = 900 MHz, Vs = 5 V	27 μs

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):	
Device type 01	100 krads(Si) <u>7/</u>
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):	
Device type 02	50 krads(Si) <u>8/</u>
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.2)	≤ 80 MeV-cm ² /mg <u>9/</u>

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

- 7/ Device type 01 may be dose rate sensitive in space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for device type 01.
- 8/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.
- 9/ Limits are characterized at initial qualification and after any design or process changes that may affect the SEP characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, customers are requested to contact the manufacturer.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 5

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org/>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 6

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C VS = 5.0 V and 3.3 V, ENBL = VS, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
RMS CONVERSION (f = 50 MHz), input RFIN to output VRMS								
Linearity error <u>3/</u>	LE	Dynamic range = 21 dB, <u>4/, 5/</u> -16 dBm ≤ VIN ≤ 5 dBm	4, 5, 6	01, 02	-1	+1	dB	
			M, D, P, L, R	4	01	-1		+1
			M, D, P, L	4	02	-1		+1
Conversion gain, VOUT = (gain x VIN) + intercept	GAIN		4, 5, 6	01, 02	4.0	5.4	V/V rms	
			M, D, P, L, R	4	01	4.0		5.4
			M, D, P, L	4	02	4.0		5.4
Output intercept <u>6/</u>	INT		1, 2, 3	01, 02	-0.05	+0.1	V	
			M, D, P, L, R	1	01	-0.05		+0.1
			M, D, P, L	1	02	-0.05		+0.1
Output voltage, high power in	POHI	PIN = 5 dBm, 400 mV rms, VS = 5.0 V	1, 2, 3	01, 02	1.15		V	
			M, D, P, L, R	1	01	1.15		
			M, D, P, L	1	02	1.15		
		PIN = 5 dBm, 400 mV rms, VS = 3.3 V	1, 2, 3	01, 02	1.2			
			M, D, P, L, R	1	01	1.2		
			M, D, P, L	1	02	1.2		
Output voltage, low power in	POLO	PIN = -21 dBm, 20 mV rms	1, 2, 3	01, 02	0.08		V	
			M, D, P, L, R	1	01	0.08		
			M, D, P, L	1	02	0.08		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 7

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C Vs = 5.0 V and 3.3 V, ENBL = Vs, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
RMS CONVERSION (f = 100 MHz), input RFIN to output VRMS								
Linearity error <u>3/</u>	LE	Dynamic range = 21 dB <u>4/</u> , <u>5/</u> , Vs = 2.97 <u>7/</u> , 3.3 V, 5.0 V	4, 5, 6	01, 02	-1	+1	dB	
		-16 dBm ≤ VIN ≤ 5 dBm	M, D, P, L, R	4	01	-1		+1
			M, D, P, L	4	02	-1		+1
Conversion gain, VOUT = (gain x VIN) + intercept	GAIN	Vs = 2.97 <u>7/</u> , 3.3 V, 5.0 V	4, 5, 6	01, 02	5.3	7.8	V/V rms	
			M, D, P, L, R	4	01	5.3		7.8
			M, D, P, L	4	02	5.3		7.8
Output intercept <u>6/</u>	INT	Vs = 2.97 <u>7/</u> , 3.3 V, 5.0 V	1, 2, 3	01, 02	-0.05	+0.1	V	
			M, D, P, L, R	1	01	-0.05		+0.1
			M, D, P, L	1	02	-0.05		+0.1
Output voltage, high power in	POHI	PIN = 5 dBm, 400 mV rms	1, 2, 3	01, 02	2.2		V	
			M, D, P, L, R	1	01	2.2		
			M, D, P, L	1	02	2.2		
Output voltage, low power in	POLO	PIN = -21 dBm, 20 mV rms	1, 2, 3	01, 02	0.08		V	
			M, D, P, L, R	1	01	0.08		
			M, D, P, L	1	02	0.08		
RMS CONVERSION (f = 900 MHz), input RFIN to output VRMS								
Linearity error <u>3/</u> , <u>8/</u>	LE	Dynamic range = 35 dB, <u>4/</u> , <u>5/</u> -25 dBm ≤ VIN ≤ 10 dBm, Vs = 5.0 V	4, 5, 6	01, 02	-1	+1	dB	
		Dynamic range = 35 dB, <u>4/</u> , <u>5/</u> -25 dBm ≤ VIN ≤ 5 dBm, Vs = 3.3 V			-1	+1		
Conversion gain, VOUT = (gain x VIN) + intercept <u>8/</u>	GAIN		4, 5, 6	01, 02	6.3	8	V/V rms	
Output intercept <u>6/</u> , <u>8/</u>	INT		1, 2, 3	01, 02	-0.05	+0.08	V	
Output voltage, high power in <u>8/</u>	POHI	PIN = 5 dBm, 400 mV rms	1, 2, 3	01, 02	2.53		V	
Output voltage, low power in <u>8/</u>	POLO	PIN = -21 dBm, 20 mV rms	1, 2, 3	01, 02	0.13		V	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 8

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C VS = 5.0 V and 3.3 V, ENBL = VS, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
RMS CONVERSION (f = 4000 MHz), input RFIN to output VRMS								
Linearity error <u>3/</u>	LE	Dynamic range = 21 dB, <u>4/, 5/</u> -16 dBm ≤ VIN ≤ 5 dBm	4, 5, 6	01, 02	-1	+1	dB	
			M, D, P, L, R	4	01	-1		+1
			M, D, P, L	4	02	-1		+1
Conversion gain, VOUT = (gain x VIN) + intercept	GAIN	VS = 3.3 V	4, 5	01, 02	3.0	4.8	V/V rms	
			6		2.4	4.1		
			M, D, P, L, R	4	01	3.0		4.8
		M, D, P, L	4	02	3.0	4.8		
		VS = 5 V	4, 5	01, 02	3.0	4.8	V/V rms	
			6		2.5	4.1		
M, D, P, L, R	4		01	3.0	4.8			
M, D, P, L	4	02	3.0	4.8				
Output intercept <u>6/</u>	INT		1, 2, 3	01, 02	-0.05	+0.1	V	
			M, D, P, L, R	1	01	-0.05		+0.1
			M, D, P, L	1	02	-0.05		+0.1
Output voltage, high power in <u>8/</u>	POHI	PIN = 5 dBm, 400 mV rms	1, 2	01, 02	1.0		V	
			3		0.7			
			M, D, P, L, R	1	01	1.0		
			M, D, P, L	1	02	1.0		
Output voltage, low power in <u>8/</u>	POLO	PIN = -21 dBm, 20 mV rms	1, 2, 3	01, 02	0.07		V	
			M, D, P, L, R	1	01	0.07		
			M, D, P, L	1	02	0.07		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 9

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C Vs = 5.0 V and 3.3 V, ENBL = Vs, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RMS CONVERSION (f = 6000 MHz), input RFIN to output VRMS							
Linearity error <u>3/, 8/</u>	LE	Dynamic range = 20 dB, <u>4/, 5/</u> -15 dBm ≤ VIN ≤ 15 dBm, Vs = 5.0 V	4, 6	01, 02	-1	+1	dB
		Dynamic range = 30 dB, <u>4/, 5/</u> -5 dBm ≤ VIN ≤ 15 dBm, Vs = 5.0 V	5		-1	+1	
	LE	Dynamic range = 20 dB <u>4/, 5/</u> -15 dBm ≤ VIN ≤ 15 dBm, Vs = 3.3 V	4, 6	01, 02	-1	+1	dB
		Dynamic range = 30 dB <u>4/, 5/</u> -5 dBm ≤ VIN ≤ 15 dBm, Vs = 3.3 V	5		-1	+1	
Conversion gain, VOUT = (gain x VIN) + intercept <u>8/</u>	GAIN		4, 5, 6	01, 02	1.52	3.0	V/V rms
Output intercept <u>6/, 8/</u>	INT		1, 2, 3	01, 02	-0.01	+0.1	V
Output voltage, high power in <u>8/</u>	POHI	PIN = 5 dBm, 400 mV rms	1, 2, 3	01, 02	0.61		V
Output voltage, low power in <u>8/</u>	POLO	PIN = -21 dBm, 20 mV rms	1, 2, 3	01, 02	0.03		V
DC PARAMETER							
Output offset	VOS	No signal at RFIN	1, 2, 3	01, 02		150	mV
			M, D, P, L, R	1	01	150	
			M, D, P, L	1	02	150	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 10

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C Vs = 5.0 V and 3.3 V, ENBL = Vs, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
ENABLE INTERFACE, pin ENBL								
Logic level to enable power, high condition <u>9/</u>	VIH	RFIN = 0 dBm, f = 100 MHz	1, 3	01, 02	1.8	Vs	V	
			M, D, P, L, R	1	01	1.8		Vs
			M, D, P, L	1	02	1.8		Vs
Logic level to disable power, low condition <u>9/</u>	VIL	RFIN = 0 dBm, f = 100 MHz	1, 3	01, 02	0	0.5	V	
			M, D, P, L, R	1	01	0		0.5
			M, D, P, L	1	02	0		0.5
Input current when high	IIH	ENBL = Vs, Vs = 2.97 V <u>7/</u> , 3.3 V, 5.0 V, RFIN = 0dBm, f = 100MHz	1, 2, 3	01, 02		0.26	μA	
			M, D, P, L, R	1	01			0.26
			M, D, P, L	1	02			0.26
Input current when low	IIL	ENBL = 0 V, Vs = 2.97 V <u>7/</u> , 3.3 V, 5.0 V, RFIN = 0dBm, f = 100MHz	1, 2, 3	01, 02		10	nA	
			M, D, P, L, R	1	01			10
			M, D, P, L	1	02			10
OUTPUT RESPONSE TIME								
Power-up response time <u>8/</u> , <u>10/</u>	tPOR	CFLTR = COUT = open, RFIN = 0 dBm, f = 900 MHz	9, 10, 11	01, 02		6	μs	
		CFLTR = 1 nF, COUT = open, RFIN = 0 dBm, f = 900 MHz	9, 10, 11			25		
		CFLTR = open, COUT = 100 nF, ROUT = 1 kΩ, RFIN = 0 dBm, f = 900 MHz, Vs = 5 V	9, 10, 11			46		
		CFLTR = open, COUT = 100 nF, ROUT = 1 kΩ, RFIN = 0 dBm, f = 900 MHz, Vs = 3.3 V	9, 10, 11			60		

See footnotes at end of table

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 11

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C Vs = 5.0 V and 3.3 V, ENBL = Vs, CFLTR = 1 nF, COUT = open unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
POWER SUPPLIES							
Quiescent current <u>11/</u>	IQ	No signal at RFIN, Vs = 2.97 V <u>7/</u> , 3.3 V, 5.0 V, 5.25 V	1, 2, 3	01, 02		1.5	mA
			M, D, P, L, R	1	01	1.5	
			M, D, P, L	1	02	1.5	
		RFIN = 5 dbm, f = 100 MHz, Vs = 2.97 V <u>7/</u> , 3.3 V, 5.0 V, 5.25 V	1, 2, 3	01, 02		4	
			M, D, P, L, R	1	01	4	
			M, D, P, L	1	02	4	
Total supply current when disabled <u>9/</u> , <u>11/</u>	IQZ	No signal at RFIN, ENBL = 0 V, Vs = 2.97 V <u>7/</u> , 3.3 V, 5.0 V, 5.25 V	1, 3	01, 02		5	µA
			2			130	
			M, D, P, L, R	1	01	5	
			M, D, P, L	1	02	5	

- 1/ Device type 01 supplied to this drawing has been characterized through all levels M, D, P, L, and R of irradiation. Device type 02 supplied to this drawing has been characterized through all levels M, D, P, and L of irradiation. However, device type 01 is only tested at the "R" level and device type 02 is only tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurement for any RHA level, TA = +25°C.
- 2/ Device type 01 may be dose rate sensitive in space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for device type 01. For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.
- 3/ Error referred to best-fit line at +25°C.
- 4/ The available output swing and, therefore, the dynamic range are altered by the supply voltage, see Figure 8 in Output Swing subsection of section 6.7 Application notes.
- 5/ Dynamic range is the ratio of maximum to minimum input level applied to the input to maintain the specified error. It is calculated by 20*log(Vrms_max/Vrms_min).
- 6/ Calculated using linear regression.
- 7/ Test added to ensure device functionality at low voltage and low temperature condition (TA = -55°C at V = 2.97 V) where for supply level V < 2.97 V at TA = -55°C there is a known design issue.
- 8/ Parameter is part of device initial characterization which is only repeated after major design and process changes or with subsequent wafer lots. Not tested post irradiation.
- 9/ If the input of the device is driven while the device is disabled (ENBL = 0 V), the leakage current of less than 5 µA increases as a function of input level and increases exponentially at TA = +125°C.
- 10/ The response time is measured from 10% to 90% of settling level; see Figure 5 in Power Consumption, Enable, and Power On/Off Response Time subsection of section 6.7 Application notes.
- 11/ Supply current is input-level dependent; see Figure 4 in Power Consumption, Enable, and Power On/Off Response Time subsection of Section 6.7 Application notes.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 12

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature 3/	Bias Vs =5.5V for Single event latch-up(SEL) test No SEL occurs at effective LET
01 and 02	No SEL	+125°C	LET ≤ 80 MeV-cm ² /mg

1/ For single event phenomenon (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature is T_A = +125°C ±10°C for latch-up .

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 13

Device types	01, 02	
Case outline	H	
Terminal number	Terminal symbol	Description
1	COMM	Device ground pin.
2	VPOS	Supply voltage pin. Operational range 3.3 V to 5.0 V.
3	ENBL	Enable pin. Connect pin to Vpos for normal operation. Connect pin to ground for disable mode for a supply current less than 1 μ A.
4	VRMS	Output pin. Rail-to-rail voltage output with limited 3 mA current drive capability. The output has an internal 100 Ω series resistance. High resistive loads are recommended to preserve output swing.
5	COMM	Device ground pin.
6	COMM	Device ground pin.
7	COMM	Device ground pin.
8	FLTR	Square-domain filter pin. Connection for an external capacitor to lower the corner frequency of the square-domain (or modulation) filter. Capacitor is connected between FLTR and Vs and forms a low-pass filter with an 8 k Ω on-chip resistor. The on-chip capacitor provides filtering with an approximate 100 kHz corner frequency. For simple waveforms, no further filtering of the demodulated signal is required.
9	RFIN	Signal input pin. Internally ac-coupled after internal termination resistance. Nominal 50 Ω input impedance.
10	COMM	Device ground pin.

FIGURE 1. Terminal connections.

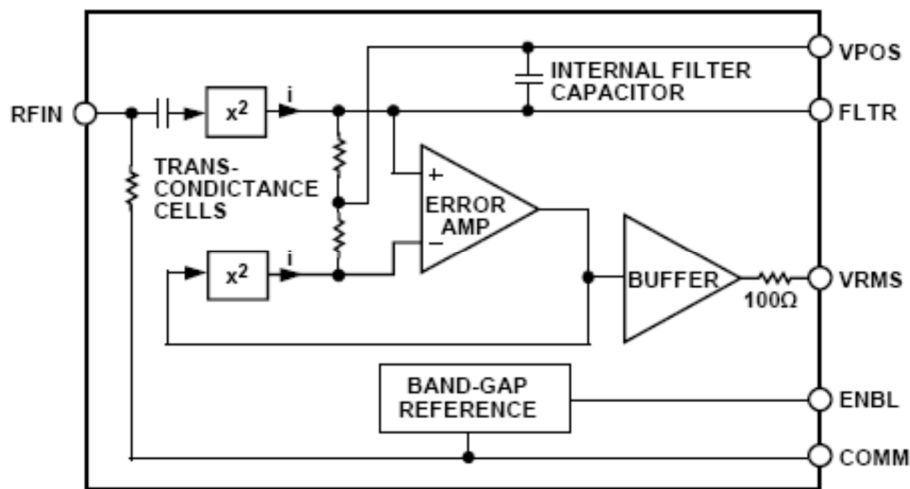


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 14

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u> , <u>2/</u> , <u>3/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>2/</u>
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>2/</u> , <u>3/</u>
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 4, 5, 6 <u>2/</u>
Group E end-point electrical parameters (see 4.4)	---	1, 4 <u>2/</u>

- 1/ PDA applies to subgroup 1 only. Delta's are not excluded from PDA.
2/ See Table IIB for delta parameters.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameter	Device types	Symbol	Limits		Units
			Min	Max	
Quiescent current (Vs = 3.3 V, no RFIN)	01, 02	IQ	-0.1	+0.1	mA
Quiescent current (Vs = 3.3 V, RFIN = 5 dBm, f = 100 MHz)	01, 02	IQ	-0.4	+0.4	mA
Total supply current when disabled (Vs = 3.3 V, no RFIN)	01, 02	IQZ	-1.0	+1.0	μA
Conversion gain (fIN = 100 MHz, Vs = 3.3 V)	01, 02	GAIN	-0.5	+0.5	V/Vrms
Output Offset (Vs = 3.3 V)	01, 02	VOS	-0.03	+0.03	V
Output Offset (Vs = 5 V)	01, 02	VOS	-0.03	+0.03	V

- 1/ 240 hour burn in and group C end point electrical parameters. Deltas are performed at TA = +25°C.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 15

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 4, 5, 6, 9, 10, and 11 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table IA.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02, and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be $+125^{\circ}\text{C}$ and the maximum rated operating temperature $\pm 10^{\circ}\text{C}$ for single event latchup testing.
- f. Bias conditions shall be $V_S = 5.5$ V for latchup measurements.
- g. For SEP test limits, see Table IB herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 16

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions Single Event Phenomenon (SEP).
- b. Occurrence of latch-up (SEL).

6.8 Application notes.

OUTPUT SWING

At any given frequency, the output voltage is nominally the conversion gain times the input rms voltage. The output voltage swings from near ground to 4.9 V on a 5.0 V supply. Figure 3 shows the output swing of this device to a CW input for various supply voltages. It is clear from Figure 3 that operating the device at lower supply voltages reduces the dynamic range as the output headroom decreases.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 17

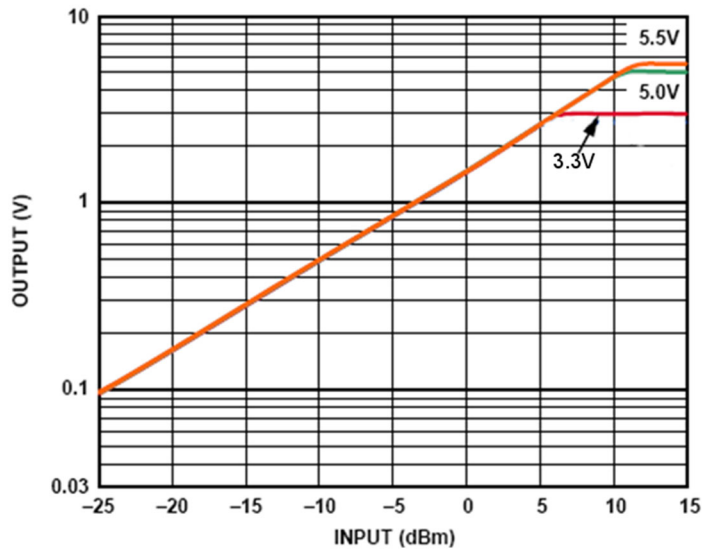


Figure 3. Output swing for supply voltages of 2.7 V, 3.3 V, 5.0 V, and 5.5 V.

POWER CONSUMPTION, ENABLE, AND POWER-ON/POWER-OFF RESPONSE TIME

The quiescent current consumption of this device varies with the size of the input signal from approximately 1.1 mA for no signal up to 6.2 mA at an input level of 0.7 V rms (10 dBm, re: 50 Ω). If the input is driven beyond this point, the supply current increases sharply (as shown in Figure 4). There is little variation in quiescent current with power supply voltage. This device can be disabled either by pulling ENBL (Pin 3) to COMM (Pins 1,5,6,7 or 10) or by removing the supply power to the device. Disabling the device via the ENBL function reduces the leakage current to less than 1 μA.

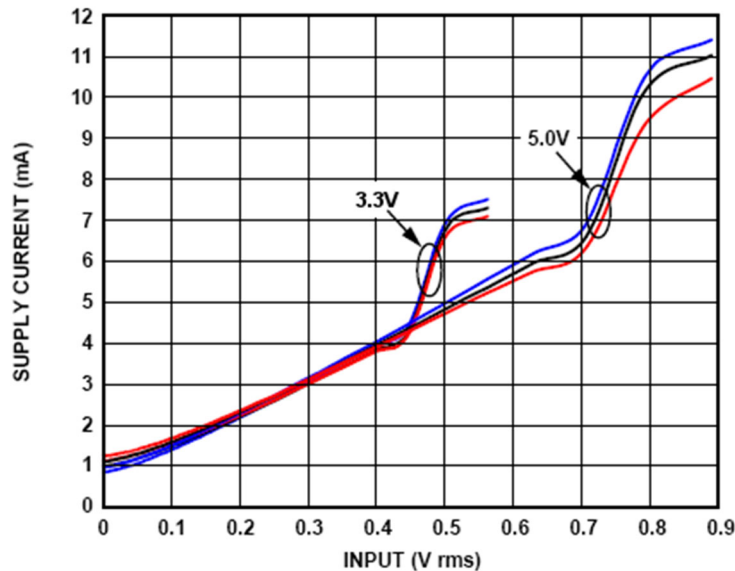


Figure 4. Supply current vs. input level; supplies = 3.3 V and 5.0 V; $T_A = -55^\circ\text{C}, +25^\circ\text{C}, \text{ and } +125^\circ\text{C}.$

If the input of this device is driven while the device is disabled (ENBL = COMM), the leakage current of less than 1 μA increases as a function of input level. When the device is disabled, the output impedance increases to approximately 33.5 kΩ. The turn-on time and pulse response is strongly influenced by the size of the square-domain filter and output shunt capacitor. Figure 5 shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 μF output filter capacitor and no square-domain filter capacitor. The falling edge is particularly dependent on the output shunt capacitance, as shown in Figure 5.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-11239
		REVISION LEVEL C	SHEET 18

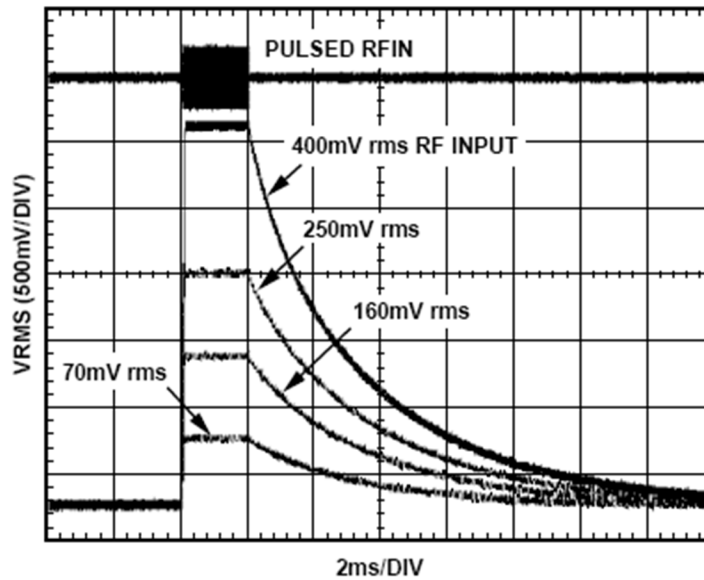


Figure 5. Output response to various RF input pulse levels, supply = 3.3 V, frequency = 900 MHz, square-domain filter open, output filter = 0.1 μ F.

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

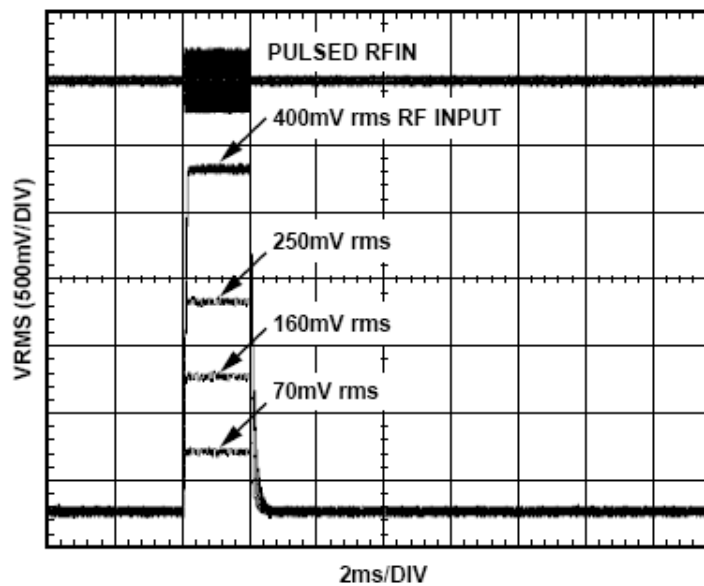


Figure 6. Output response to various RF input pulse levels, supply = 3.3 V, frequency = 900 MHz, square-domain filter open, output filter = 0.1 μ F with parallel 1 k Ω .

The square-domain filter improves the rms accuracy for high crest factors (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section), but it can hinder the response time. For optimum response time and low ac residual, both the square-domain filter and the output filter should be used. The square-domain filter at FLTR can be reduced to improve response time, and the remaining ac residual can be decreased by using the output filter, which has a smaller time constant.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
C

5962-11239

SHEET
19

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-07-14

Approved sources of supply for SMD 5962-11239 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R1123901VHA	24355	ADL5501AL/QMLR
5962L1123902VHA	24355	ADL5501AL/QMLL

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

24355

Vendor name
and address

Analog Devices
Rt 1 Industrial Park
PO Box 9106
Norwood, MA 02062
Point of contact:
7910 Triad Center Drive
Greensboro, NC 27409-9605

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