

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add new footnote 5/ to t <sub>AVQV1</sub> resulting in changes to the rest of the footnote sequence in Table IA. Removed erroneous footnote from t <sub>AVET</sub> parameter in Table IA. Changed footnotes 5/ through 8/ to be 6/ through 9/ and added footnote 5/ at the end of Table IA. - lhI	12-05-01	Charles F. Saffle
B	Vendor corrected Figure 1 for dimensions A1 and c. Update drawing to reflect current MIL-PRF-38535 requirements. Remove all references to Class M. - llb	14-07-14	Charles F. Saffle
C	Update to current MIL-PRF-38535 requirements. - llb	19-07-17	Charles F. Saffle



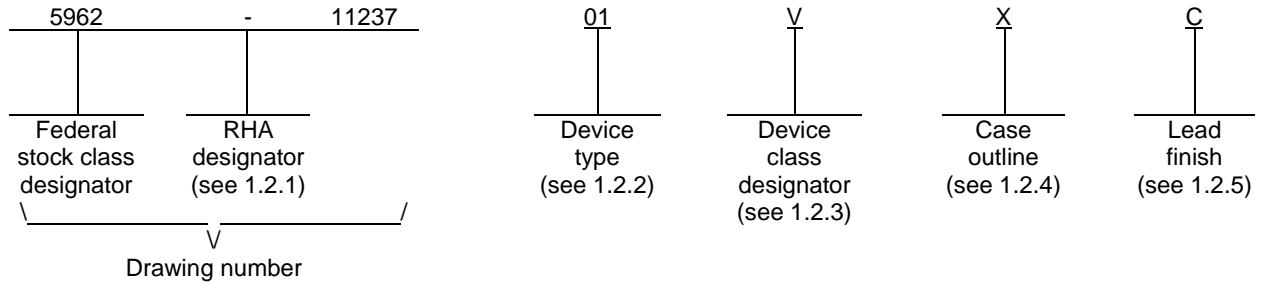
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Laura H. Leeper	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Rajesh Pithadia																		
	APPROVED BY Charles F. Saffle	<p align="center">MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K X 32-BIT (16M) WITH EMBEDDED EDAC, LOW VOLTAGE SRAM, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 12-03-21																		
	REVISION LEVEL C		<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE <b>67268</b></td> <td><b>5962-11237</b></td> </tr> </table>	SIZE A	CAGE CODE <b>67268</b>	<b>5962-11237</b>													
SIZE A	CAGE CODE <b>67268</b>	<b>5962-11237</b>																	
AMSC N/A		SHEET 1 OF 26																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	SMV512K32	512K X 32-bit CMOS SRAM	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q and V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	76	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>2</b>

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range, (V <sub>DD1</sub> ).....	-0.3 V dc to +2.0 V dc
Supply voltage range, (V <sub>DD2</sub> ).....	-0.3 V dc to +3.8 V dc
Voltage range on any pin.....	-0.3 V dc to +3.8 V dc
Storage temperature range, (T <sub>STG</sub> ).....	-65°C to +150°C
Power dissipation, (P <sub>D</sub> ).....	1.2 W
Junction temperature, (T <sub>J</sub> ).....	+150°C
Input current, dc (I <sub>i</sub> ).....	±5 mA
Thermal resistance, junction-to-case, (θ <sub>JC</sub> ):	
Case X.....	+5°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V <sub>DD1</sub> ).....	+1.7 V dc to +1.9 V dc
Supply voltage range, (V <sub>DD2</sub> ).....	+3.0 V dc to +3.6 V dc
Supply voltage, (V <sub>SS</sub> ).....	0 V dc
Operating case temperature range, (T <sub>C</sub> ).....	-55°C to +150°C
Input voltage, dc.....	0 V dc to V <sub>DD2</sub>

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org>.)

1/ Over operating free-air temperature range (unless otherwise noted).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>3</b>

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing waveform(s). The timing waveform(s) shall be as specified on figures 4 through 17.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>4</b>

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>DD1</sub> = 1.7 V to 1.9 V V <sub>DD2</sub> = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
High-level input voltage	V <sub>IH</sub>		1, 2, 3	All	0.7 x V <sub>DD2</sub>		V	
Low-level input voltage	V <sub>IL</sub>		1, 2, 3	All		0.3 x V <sub>DD2</sub>		
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA, V <sub>DD2</sub> = V <sub>DD2</sub> (min)	1, 2, 3	All	0.8 x V <sub>DD2</sub>			
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4 mA, V <sub>DD2</sub> = V <sub>DD2</sub> (min)	1, 2, 3	All		0.2 x V <sub>DD2</sub>		
Input capacitance C <sub>IN</sub> <u>1/</u>	C <sub>IN</sub>	f = 1 MHz at 0 V	4	All		2	pF	
Bidirectional I/O capacitance <u>1/</u>	C <sub>IO</sub>	See 4.1.1e	4	All		2.5		
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD2</sub> and V <sub>SS</sub>	1, 2, 3	All	-500	500	nA	
Three state output leakage current	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>DD2</sub> and V <sub>SS</sub> , V <sub>DD2</sub> = V <sub>DD2</sub> (max); GZ = V <sub>DD2</sub> (max)	1, 2, 3	All	-500	500		
Short-circuit output current <u>2/ 3/</u>	I <sub>OS</sub>	V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>DD2</sub> V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>SS</sub>	1, 2, 3	All	-46	46	mA	
Supply current operating @ 1 MHz (Write)	I <sub>DD1</sub> <sup>(OP1)</sup>	Inputs: V <sub>IL</sub> = V <sub>SS</sub> + 0.2 V V <sub>IH</sub> = V <sub>DD2</sub> - 0.2 V, I <sub>OUT</sub> = 0 A, V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)	1, 3	All		18		
			2			31		
Supply current operating @ 1 MHz (Read)	I <sub>DD1</sub> <sup>(OP1)</sup>		1, 3	All		13		
			2			27		
Supply current operating @ 50.0 MHz (Write)	I <sub>DD1</sub> <sup>(OP2)</sup>		1, 3	All		635		
			2			460		
Supply current operating @ 50.0 MHz (Read)	I <sub>DD1</sub> <sup>(OP2)</sup>		1, 3	All		365		
			2			315		
Supply current operating @ 1 MHz (Write)	I <sub>DD2</sub> <sup>(OP1)</sup>		1, 3	All		255		μA
			2					
Supply current operating @ 1 MHz (Read)	I <sub>DD2</sub> <sup>(OP1)</sup>		1, 3	All		5.2		mA
			2			5.1		
Supply current operating @ 50.0 MHz (Write)	I <sub>DD2</sub> <sup>(OP2)</sup>	1, 3	All		5.9			
		2			1.2			

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>5</b>

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>DD1</sub> = 1.7 V to 1.9 V V <sub>DD2</sub> = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current operating @ 50.0 MHz (Read)	I <sub>DD2</sub> ( <sup>OP2</sup> )		1, 3	All		275	mA
			2			120	
Supply current standby @ 0 MHz <u>4/</u>	I <sub>DD1</sub> ( <sup>SB</sup> )	CMOS inputs, I <sub>OUT</sub> = 0 A E1Z = V <sub>DD2</sub> - 0.2 V, E2 = GND, V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)	1, 3	All		0.375	mA
	I <sub>DD2</sub> ( <sup>SB</sup> )		2			17	
Supply current standby A(18:0) @ 50.0 MHz	I <sub>DD1</sub> ( <sup>SB</sup> )		1, 3	All		4.4	mA
	I <sub>DD2</sub> ( <sup>SB</sup> )		2			2.1	
Functional test		See 4.4.1c	7, 8A, 8B	All			
AC Characteristics Read Cycle							
Read cycle time	t <sub>AVA1</sub>	See figure 4	9, 10, 11	All	20		ns
Address to data valid from address change <u>5/</u>	t <sub>AVQV1</sub>					20	
Output hold time	t <sub>AXQX</sub>				7.5		
GZ-controlled output enable time	t <sub>GLQX1</sub>	See figure 6	9, 10, 11	All	3.5		
GZ-controlled output data valid	t <sub>GLQV</sub>					8.6	
GZ-controlled output enable tri- state time	t <sub>GHQZ1</sub>				3.5	5	
E-controlled output enable time	t <sub>ETQX</sub>	See figure 5	9, 10, 11	All	3.5		
E-controlled access time	t <sub>ETQV</sub>					20	
E-controlled tri-state time	t <sub>ETQZ</sub>					3.5	5
Address to error flag valid	t <sub>AVMV</sub>	See figure 4	9, 10, 11	All		20	
Address to error flag hold time from address change	t <sub>AXMX</sub>					7.5	
GZ-controlled error flag valid	t <sub>GLMV</sub>	See figure 6	9, 10, 11	All		8.6	
GZ-controlled error flag enable time	t <sub>GLMX</sub>					3.5	
E-controlled error enable time	t <sub>ETMX</sub>	See figure 5	9, 10, 11	All	3.5		

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>6</b>

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>DD1</sub> = 1.7 V to 1.9 V V <sub>DD2</sub> = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Characteristics Read Cycle – Continued.							
E-controlled error flag time	t <sub>ETMV</sub>		9, 10, 11	All		20	ns
GZ-controlled error flag tri-state time <u>6/</u>	t <sub>GHMZ</sub>	See figure 6	9, 10, 11	All	3.5	5	
Chip enable change to MBE tri-state <u>6/</u>	t <sub>EFMZ</sub>	See figure 5	9, 10, 11	All	3.5	5	
AC Characteristics Write Cycle							
Write-through cycle time	t <sub>AVAV</sub>	See figures 7, 9, 10 and 12	9, 10, 11	All	20		ns
Write cycle time with GZ always high <u>7/</u>	t <sub>AVAV2</sub>	See figures 8 and 11			13.8		
Device enable to end of write (WZ-controlled)	t <sub>ETWH</sub>	See figures 7, 8, and 9			12		
Device enable to end of write (E-controlled) <u>6/</u>	t <sub>ETWH2</sub>	See figures 10 and 12			11		
Address setup time for write (E-controlled)	t <sub>AVET</sub>	See figures 10, 11, and 12			1.4		
E-controlled tri-state time	t <sub>EFQZ</sub>	See figures 7, 9, 10, and 12			3.5	5	
Address setup time for write (WZ-controlled)	t <sub>AVWL</sub>	See figures 7, 8, 9			8.5		
Write pulse width	t <sub>WLWH</sub>				7.9		
Address hold time for write-through (WZ-controlled) <u>6/</u>	t <sub>WHAX</sub>	See figures 7 and 9			8.5		
Address hold time for write (WZ-controlled) with GZ always high <u>7/</u>	t <sub>WHAX1</sub>	See figure 8			2.3		
Address hold time for device enable (E-controlled)	t <sub>EFAX</sub>	See figures 10, 11, and 12			0.1		
Device enable pulse width (E-controlled) <u>6/</u>	t <sub>ETEF</sub>				19.5		
Device enable pulse width (E-controlled) with GZ always high <u>7/</u>	t <sub>ETEF1</sub>	See figure 11			12.3		
Data set-up time	t <sub>DVWH</sub>	See figures 7, 8, 9, 10, and 12			8.2		
Data hold time	t <sub>WHDX</sub>				0.2		
Write disable time to device disable for write-through	t <sub>WHEF</sub>		8.5				

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 7

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>DD1</sub> = 1.7 V to 1.9 V V <sub>DD2</sub> = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
AC Characteristics Write Cycle – Continued.								
Write disable time to device disable with GZ always high <u>7/</u>	t <sub>WHEF1</sub>	See figure 8	9, 10, 11	All			ns	
Write disable time. Write pulse width high for write-through	t <sub>WHWL</sub>	See figures 7 and 9			12.1			
Write disable time. Write pulse width with GZ always high <u>7/</u>	t <sub>WHWL1</sub>	See figure 8			2.6			
WZ-controlled tri-state end time	t <sub>WHQX</sub>	See figure 7 and 10			3			
WZ-controlled output data valid	t <sub>WHQV</sub>					10		
WZ-controlled tri-state time	t <sub>WLQZ</sub>	See figure 7			2	3.3		
GZ-controlled output enable time	t <sub>GLQX</sub>	See figure 9 and 12			1.3			
GZ-controlled output data valid	t <sub>GLQV</sub>					8.6		
GZ-controlled error flag enable time	t <sub>GLMX</sub>					3.5		
GZ-controlled error flag valid	t <sub>GLMV</sub>							8.6
Chip enable change to MBE tri-state <u>6/</u>	t <sub>EFMZ</sub>				See figures 7, 9, 10, and 12	3.5		5
WZ-controlled output MBE tri-state time <u>6/</u>	t <sub>WLMZ</sub>	See figure 7	2	3.3				
AC Characteristics for EDAC Function								
User programmable, BUSYZ low to SCRUBZ low	t <sub>BLSL</sub>	See figures 13 and 14	9, 10, 11	All		<u>8/</u>	ns	
User programmable, BUSYZ low  to BUSYZ low	t <sub>LBLBL</sub>	See figure 14				<u>9/</u>		
SCRUBZ low to SCRUBZ high	t <sub>SLSH</sub>	See figures 13 and 14			200	504		
SCRUBZ high to SCRUBZ high	t <sub>SHSH</sub>				50	120		
Device enable to MBE high	t <sub>ETMH</sub>				5.5			
GZ high to MBE high	t <sub>GHHM</sub>				6.5			

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 8



TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>DD1</sub> = 1.7 V to 1.9 V V <sub>DD2</sub> = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Characteristics for EDAC Function – Continued.							
Address valid to MBE high	t <sub>AVMH</sub>	See figures 15, 16, and 17	9, 10, 11	All	0.9		ns
MBE high to MBE low	t <sub>MHML</sub>				12.8		
MBE low to device disable	t <sub>MLEF</sub>				0.4		
MBE low to GZ low	t <sub>MLGL</sub>				1.8		
MBE low to address change	t <sub>MLAX</sub>				0.1		
MBE high to data change	t <sub>MHQX</sub>	See figures 16 and 17			4.5		
MBE high to data valid	t <sub>MHQV</sub>					8.2	
Memory enable change to output data tri-state	t <sub>EFQZ</sub>				3.5	5	
Memory enable change to MBE tri-state <sup>6/</sup>	t <sub>EFMZ</sub>	See figure 14			3.5	5	
GZ-controlled error flag enable time	t <sub>GLMX</sub>	See figure 13			3.5		
E-controlled error flag enable time	t <sub>ETMX</sub>	See figure 14			3.5		
E1Z low to BUSYZ low	t <sub>INITE</sub>					160	
MBE low to BUSYZ low	t <sub>INIT MBE</sub>	See figure 13				160	
SCRUBZ low to MBE valid	t <sub>SLMV</sub>	See figures 13 and 14				146	
E1Z high to SCRUBZ high	t <sub>E1ZSH</sub>	See figure 14				20	
E1Z high to BUSYZ high	t <sub>E1ZBH</sub>					20	
MBE high to BUSYZ high	t <sub>MHBH</sub>	See figure 15				20	

<sup>1/</sup> Measured for initial qualification and after process or design changes that could affect input/output capacitance.

<sup>2/</sup> Provided as a design limit but not guaranteed or tested.

<sup>3/</sup> No more than one output may be shorted at a time for a maximum duration of one second.

<sup>4/</sup> V<sub>IH</sub> = V<sub>DD2</sub>(max), V<sub>IL</sub> = 0 V.

<sup>5/</sup> At 5 pF load.

<sup>6/</sup> Parameters ensured by design and/or characterization if not production tested.

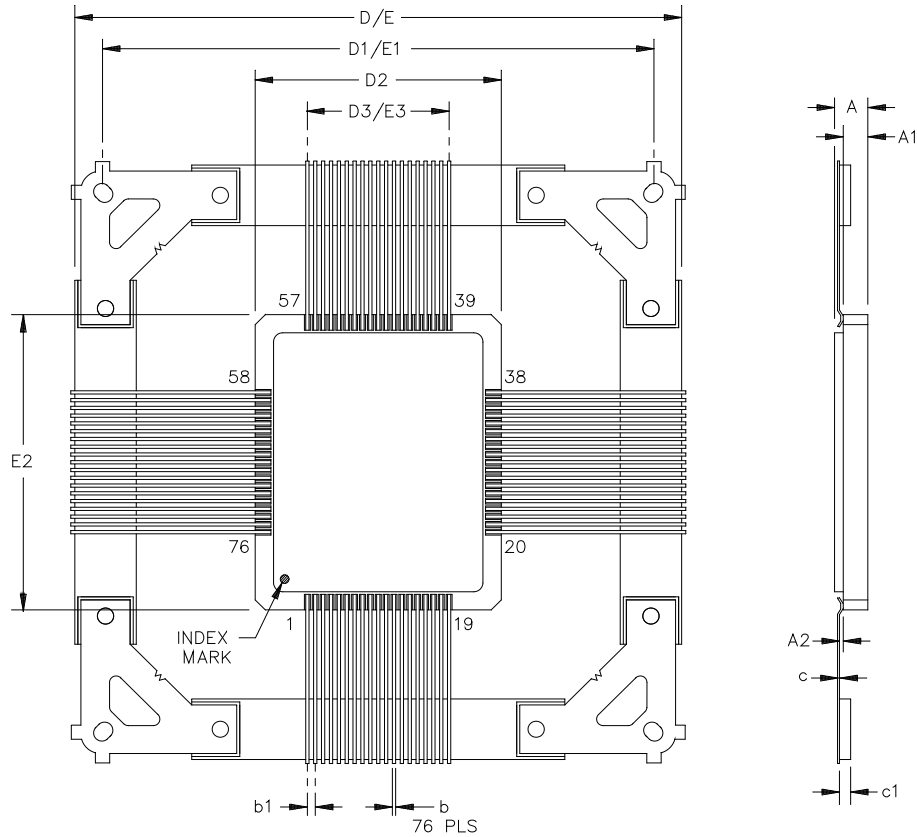
<sup>7/</sup> Write-only operations with GZ fixed high (no write-through).

<sup>8/</sup> See Table IB for typical timing characteristics for Scrub Rate Variation options.

<sup>9/</sup> See Table IC for typical timing characteristics for BUSYZ Low to SCRUBZ Low Delay variation options.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET <b>9</b>

Case outline X



NOTE: A. All linear dimensions are in millimeters.  
 B. The leads are gold plated and can be solderdipped.  
 C. Lid is connected to GND leads.  
 D. Tie-bar dimensions are for reference only.

Symbol	Dimension (unit : mm)		
	Min.	Nom.	Max.
A			2.67
A1			2.29
A2	0.05		0.36
b	0.15		0.25
b1		0.635	
c	0.10		0.20
c1		0.9	
D/E			51.31
D1/E1	45.640	45.720	45.800
D2	20.262	20.462	20.662
D3/E3		11.43	
E2	25.062	25.312	25.562

FIGURE 1. Case outline.

<p><b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990</p>	<p>SIZE <b>A</b></p>		<p><b>5962-11237</b></p>
		<p>REVISION LEVEL <b>C</b></p>	<p>SHEET 10</p>

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V <sub>SS2</sub>	39	V <sub>SS2</sub>
2	DQ0	40	DQ31
3	DQ1	41	DQ30
4	DQ2	42	DQ29
5	DQ3	43	DQ28
6	DQ4	44	DQ27
7	DQ5	45	DQ26
8	DQ6	46	DQ25
9	DQ7	47	DQ24
10	V <sub>SS1</sub>	48	V <sub>SS1</sub>
11	DQ8	49	DQ23
12	DQ9	50	DQ22
13	DQ10	51	DQ21
14	DQ11	52	DQ20
15	DQ12	53	DQ19
16	DQ13	54	DQ18
17	DQ14	55	DQ17
18	DQ15	56	DQ16
19	V <sub>DD1</sub>	57	V <sub>DD1</sub>
20	V <sub>DD1</sub>	58	V <sub>DD1</sub>
21	V <sub>DD1</sub>	59	V <sub>DD1</sub>
22	A11	60	A10
23	A12	61	A9
24	A13	62	A8
25	A14	63	A7
26	A15	64	A6
27	A16	65	WZ
28	E1Z	66	A18
29	GZ	67	V <sub>SS1</sub>
30	E2	68	A17
31	V <sub>DD2</sub>	69	A5
32	V <sub>SS1</sub>	70	A4
33	SCRUBZ	71	A3
34	BUSYZ	72	A2
35	MBE (See note)	73	A1
36	V <sub>DD2</sub>	74	A0
37	MSS	75	V <sub>SS2</sub>
38	V <sub>SS2</sub>	76	V <sub>SS2</sub>

Note: A 1-k $\Omega$  resistor must be attached from the MBE pin to ground to insure that MBE cannot float high during time intervals when it is actively driven HIGH by the memory or actively driven by the external memory control.

FIGURE 2. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 11

SRAM Device Control Operation Truth Table

E1Z	E2	GZ	WZ	MBE	I/O Mode	Mode
H	X	X	X	X	DQ(31:0) 3-state	Standby without EDAC scrub enable
L	L	X	X	X	DQ(31:0) 3-state	Standby with EDAC scrub enable <u>1/</u>
L	H	L	H	X	DQ(31:0) Data out	Word Read
L	H	X	L	X	DQ(31:0) Data in	Word Write
L	H	H	H	L	DQ(31:0) 3-state	3-state
L	H	H	H	H	DQ(31:0) Data in/out	EDAC function select (see EDAC Function Select Truth Table) <u>2/</u>

Notes:

- 1/ During SCRUB mode, MBE is 3-state if GZ is high and indicates multiple or single bit error if GZ is low.  
2/ Special precautions must be observed to prevent accidental over-writing of the Control Register in the memory after a bit error is detected and the memory drives MBE high.

Example Control Settings for Resetting MBE

Sequence	E1Z	E2	GZ	WZ	MBE	I/O Mode	Mode
1	L	H	L	H	L	DQ(31:0) Data out	Normal read mode with EDAC enabled
2	L	H	L	H	H	DQ(31:0) Data out	MBE driven high when single bit or multiple bit error (depending on user configuration) is detected during read
3	H	L	L	H	H	DQ(31:0) Data out	Memory disabled
4	H	L	H	H	H→L	DQ(31:0) 3-state	Outputs tri-stated and MBE pulled low by load R
5	L	H	H	H	L	DQ(31:0) 3-state	Read at a last known error free address <u>1/</u>
6	L	H	L	H	L	DQ(31:0) Data out	Output enable-controlled read <u>2/</u>

Notes:

- 1/ During this operation MBE drive circuitry in the memory is tri-stated but MBE is held low by the 1-kΩ resistor to ground.  
2/ During this operation MBE is actively driven low by the MBE drive circuitry in the memory after a time,  $t_{GMLV}$ , and the memory is back to the original state corresponding to normal read mode with EDAC enabled.

FIGURE 3. Truth Tables.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 12

EDAC Control Operation Mode Truth Table

MBE (OUTPUT)	SCRUBZ	BUSYZ	I/O Mode	Mode
H	H	L	Read	Data error detected <u>1/</u>
L	H	H	Read	Valid data out <u>1/</u>
X	H	H	X	Device ready
X	H	L	X	Device ready/early scrub request coming
X	L	X	Not accessible	Device busy (scrub in progress)

Notes:

1/ MBE is only valid in EDAC operation modes (Read with EDAC enable or scrub). MBE indicates Multiple Bit Error if A[12] bit in the control register is '0'. MBE indicates Single Bit Error if A[12] bit in the control register is '1'.

EDAC Function Select Truth Table 1/

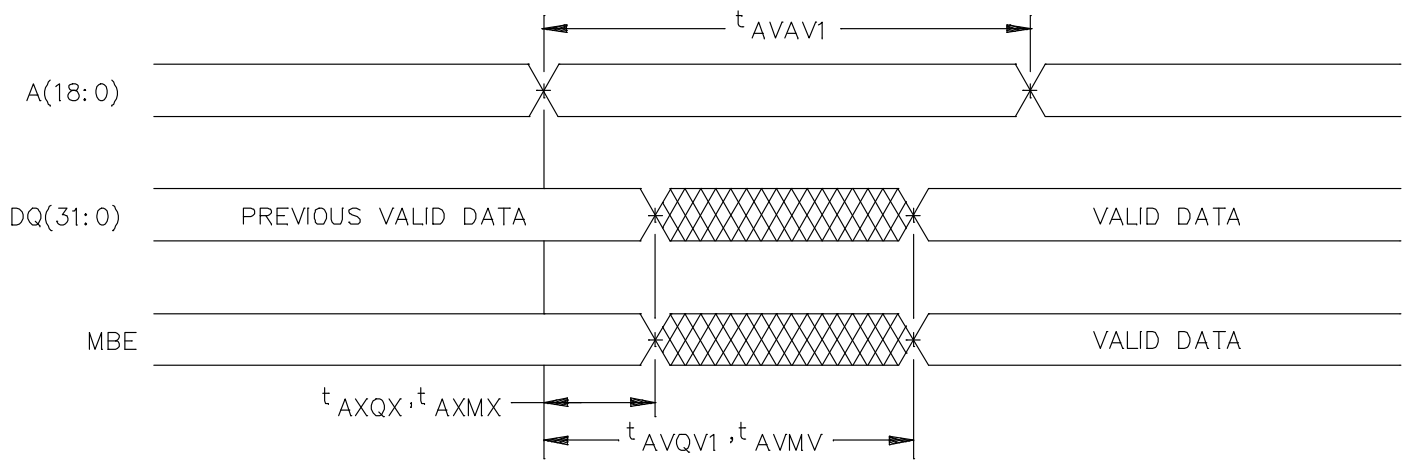
E1Z	E2	GZ	WZ	MBE	A7	A8	A9	A10	Mode
L	H	H	H	H	X	X	L	L	Write control register
L	H	H	H	H	X	X	H	L	Read control register
L	H	H	H	H	H	X	X	H	Address counter read

Notes:

1/ All other combinations of A7-A10 are reserved and should be avoided.

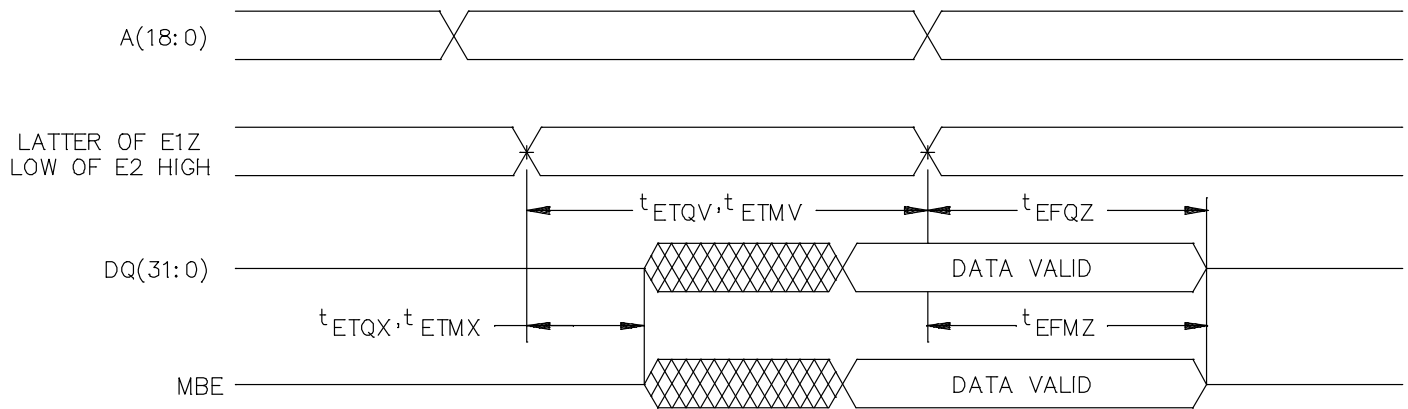
FIGURE 3. Truth Tables – Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL C	SHEET 13



Assumptions: E1Z low, E2 high, WZ high, GZ low and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

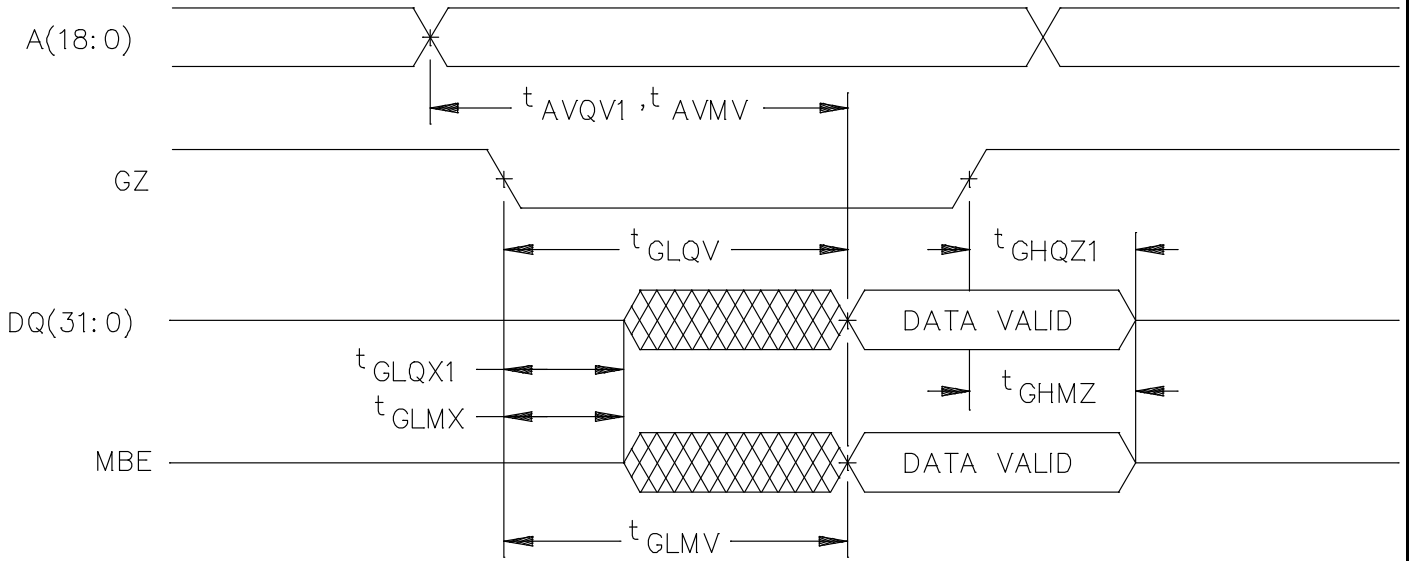
FIGURE 4. SRAM Read Cycle 1, Address-Controlled Access.



Assumptions: GZ low, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

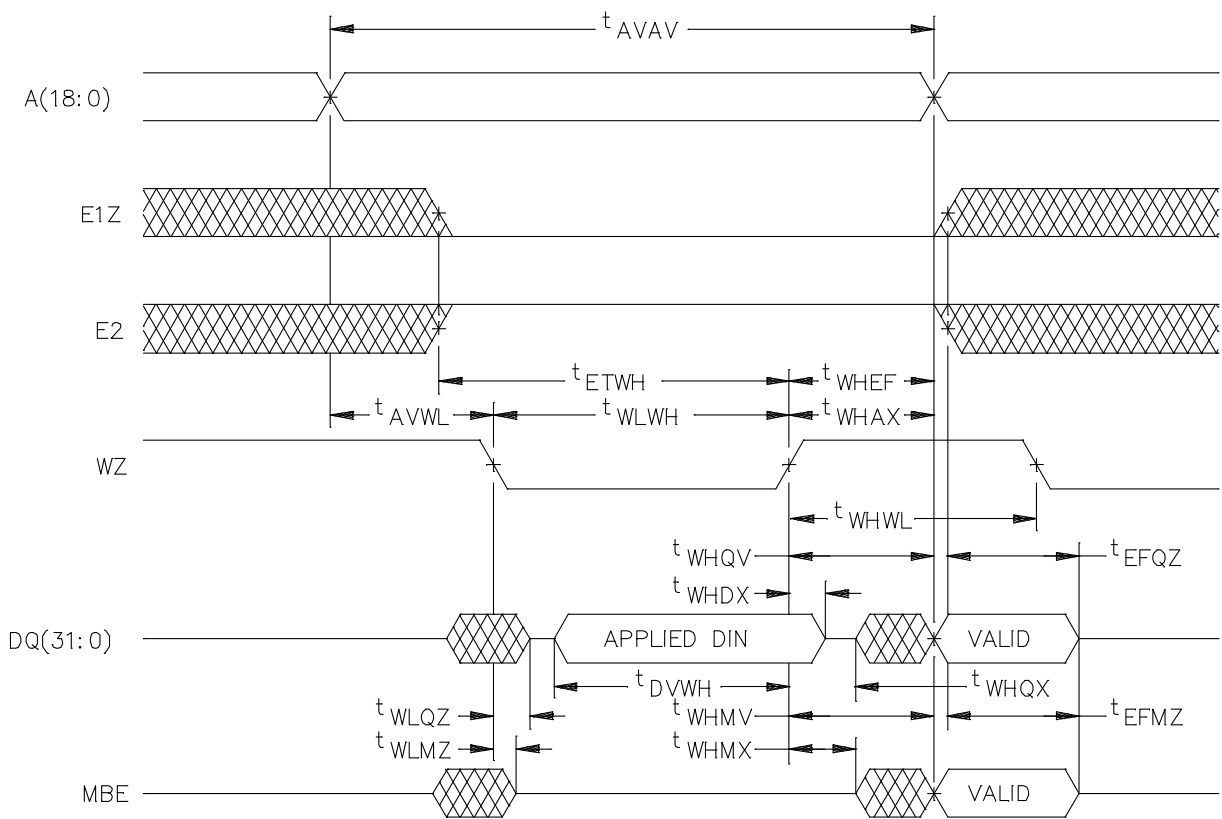
FIGURE 5. Read Cycle 2, Chip Enable-Controlled Access.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 14



Assumptions: E1Z low, E2 high, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

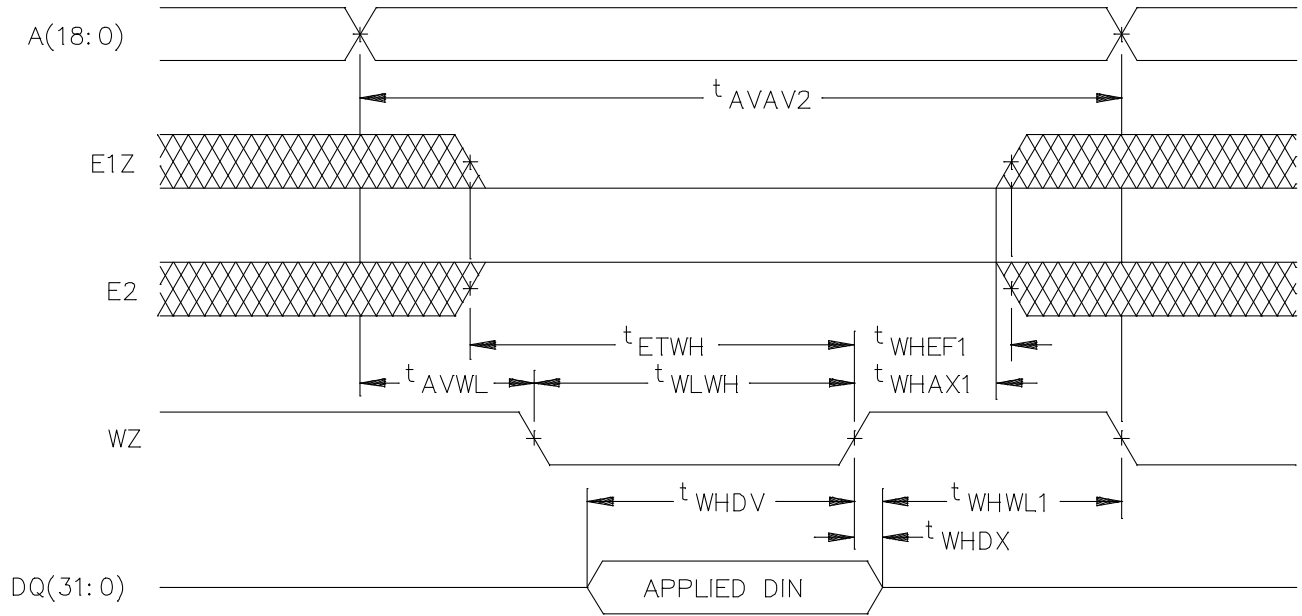
FIGURE 6. Read Cycle 3, Output Enable-Controlled Access.



Assumption: SCRUBZ high, GZ low

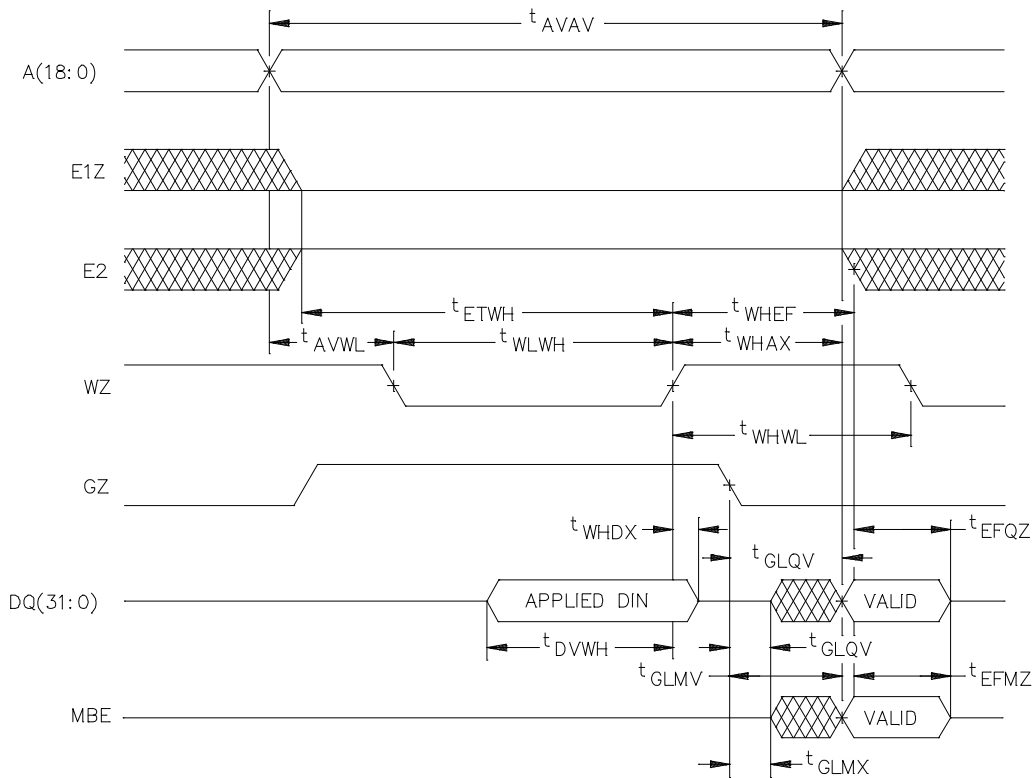
FIGURE 7. SRAM Write Cycle 1, WZ Controlled Access.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 15



Assumptions: SCRUBZ high, GZ high

FIGURE 8. SRAM Write Cycle 1a, WZ-Controlled Write Only Write Only With GZ Fixed High.



Assumptions: SCRUBZ high

FIGURE 9. SRAM Write Cycle 2, WZ Controlled Write Data Write Through Controlled by GZ.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

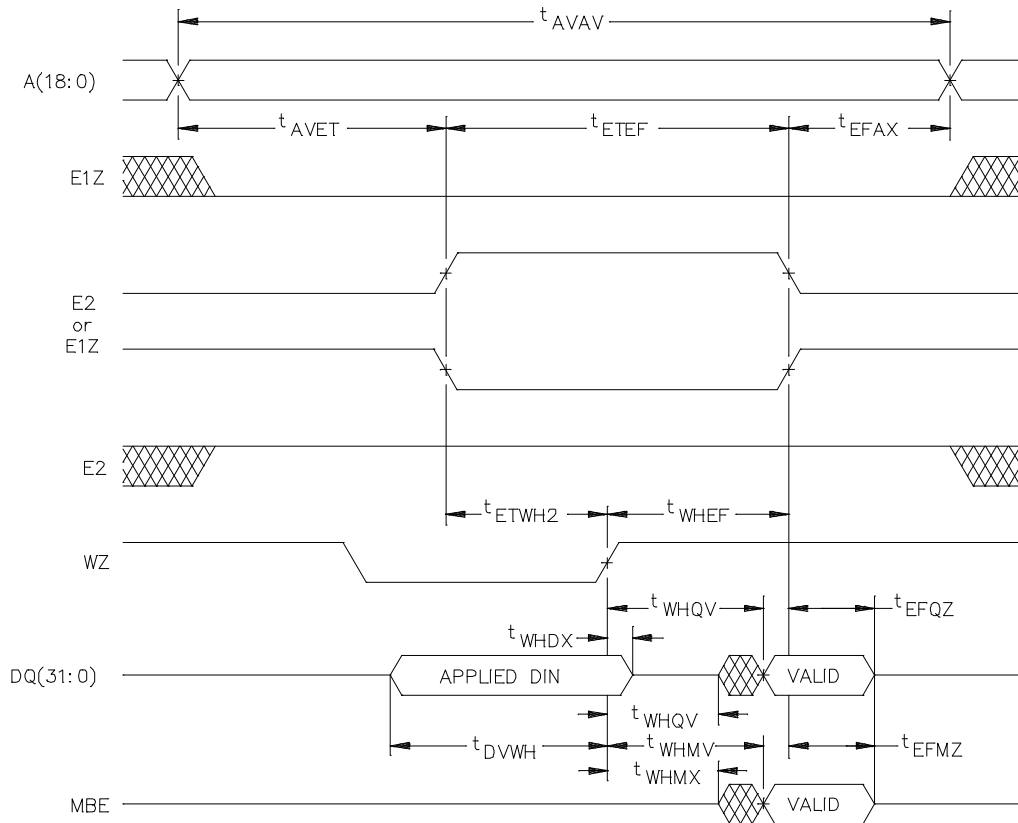
**5962-11237**

REVISION LEVEL  
**C**

SHEET

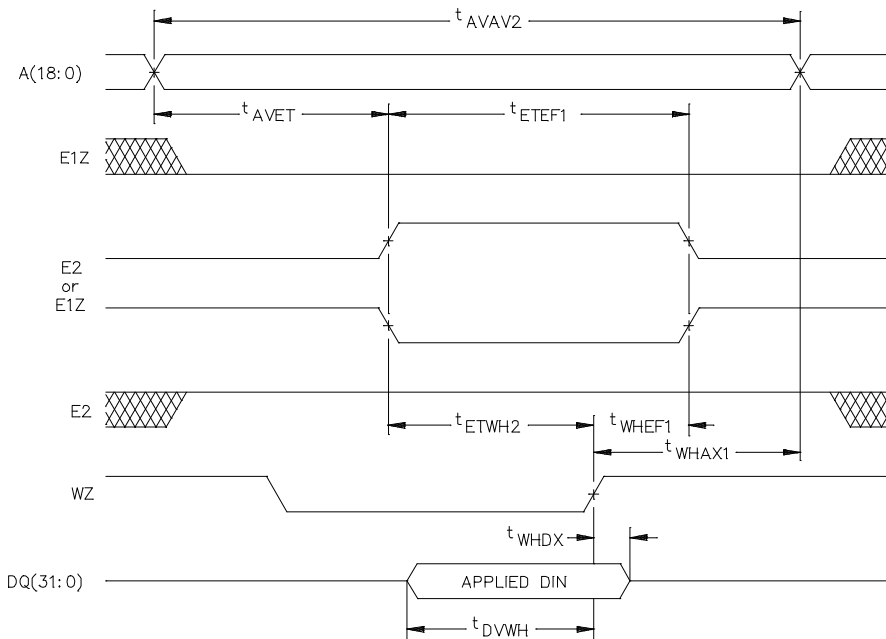
16





Assumptions: Either E1Z/E2 scenario can occur, SCRUBZ high, GZ low

FIGURE 10. SRAM Write Cycle 3, Enable Controlled Write With Data Write Through Controlled by WZ.



Assumptions: Either E1Z/E2 scenario can occur, SCRUBZ high, GZ High

FIGURE 11. SRAM Write Cycle 3a, Enable Controlled Write Only With GZ Fixed High.

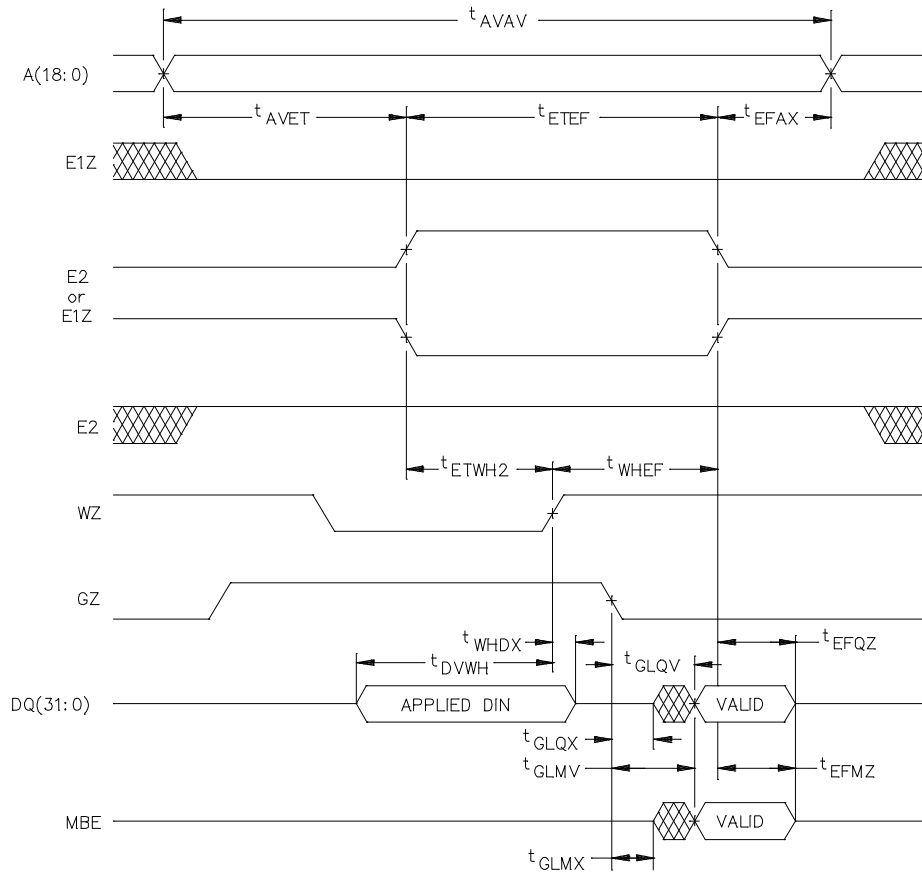
**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

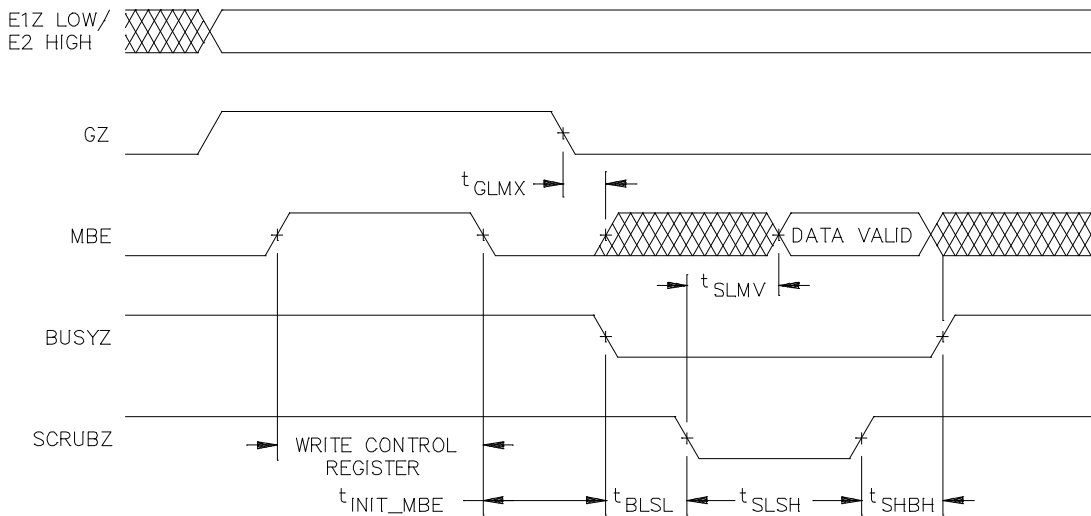
**5962-11237**

SHEET  
**17**



Assumptions: Either E1Z/E2 scenario can occur, SCRUBZ high

FIGURE 12. SRAM Write Cycle 4, Enable Controlled Write with Data Write Through Controlled by GZ.



Assumption: WZ is high

FIGURE 13. Scrub Cycle Controlled MBE.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

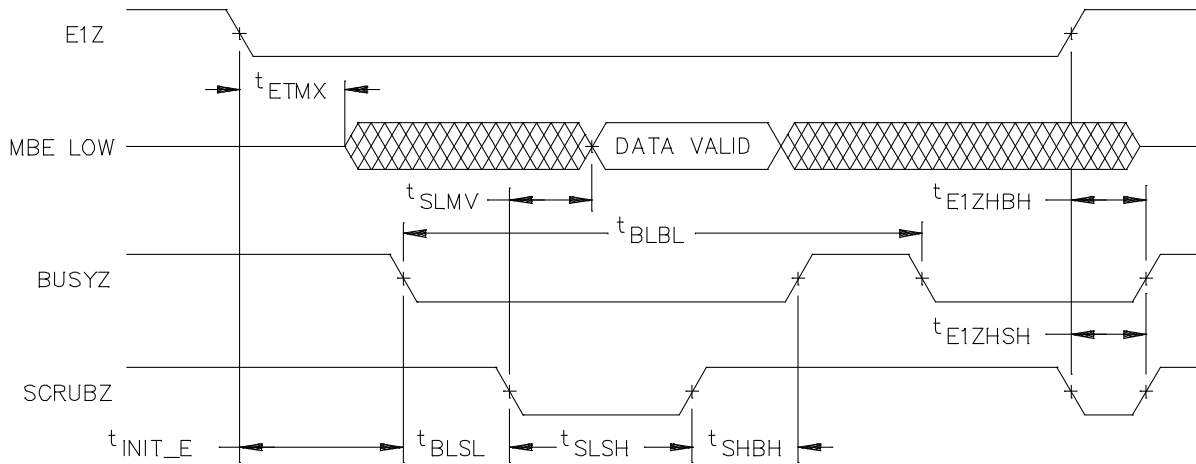
SIZE  
**A**

**5962-11237**

REVISION LEVEL  
**C**

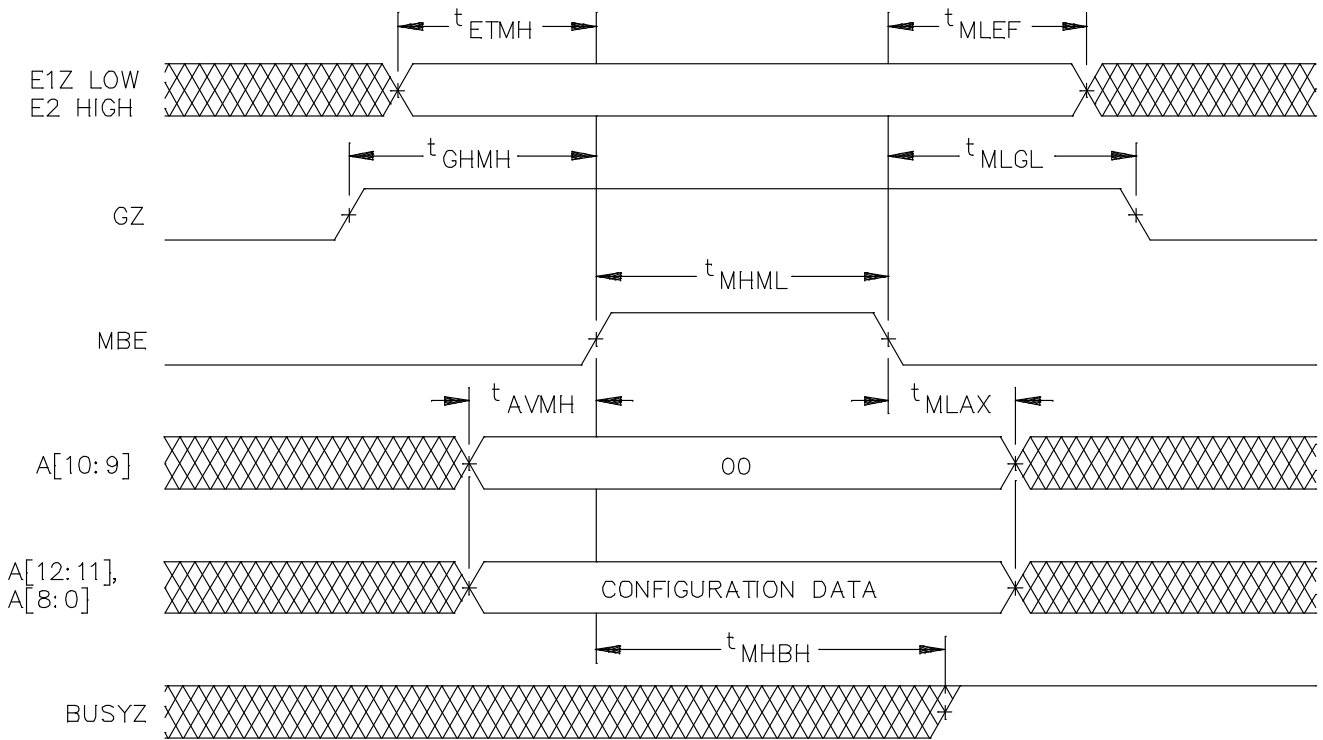
SHEET

18



Assumptions: E2 and GZ are low, WZ is high

FIGURE 14. Scrub Cycle Controlled E1Z.



Assumptions: SCRUBZ and WZ are high

FIGURE 15. Control Register Write Cycle.

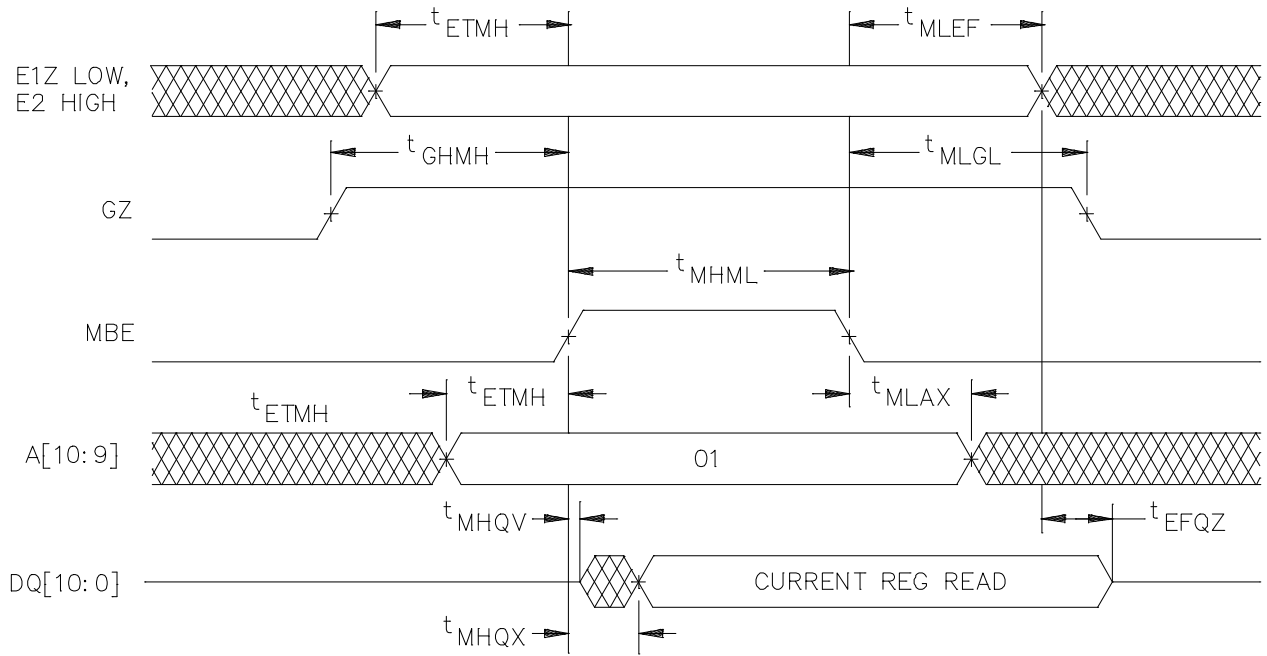
**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

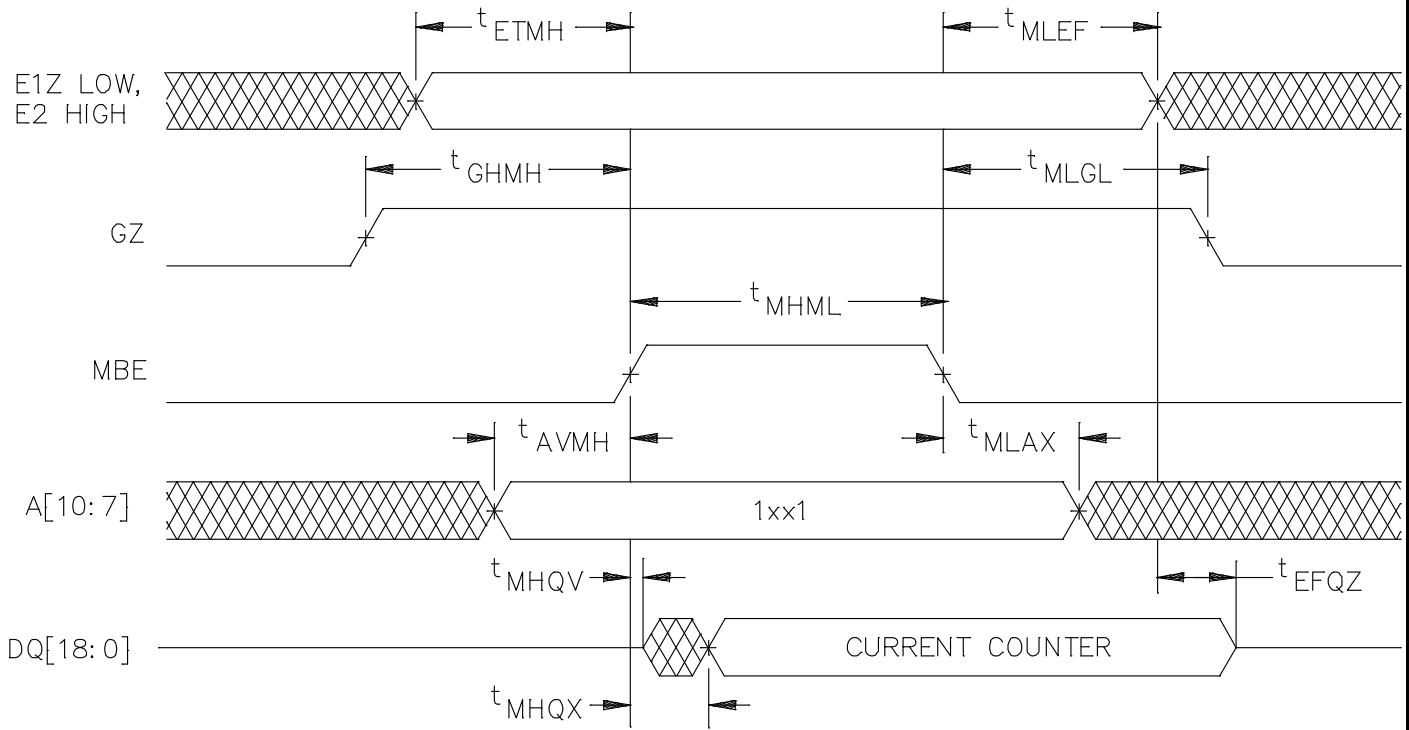
**5962-11237**

SHEET  
**19**



Assumptions: SCRUBZ and WZ are high

FIGURE 16. Control Register Read Cycle.



Assumptions: SCRUBZ and WZ are high

FIGURE 17. Address Counter Read.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 20

TABLE IB. – Scrub Rate Variation.

(Voltage = 1.8 V, Temperature = -55°C to 125°C)

VALUE	MAX (ns)
0000	N/A
0001	N/A
0010	N/A
0011	N/A
0100	1,500
0101	3,100
0110	6,100
0111	12,200
1000	24,200
1001	48,300
1010	96,400
1011	192,500
1100	384,500
1101	770,000
1110	1,500,00
1111	3,200,00

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
C

**5962-11237**

SHEET  
21

TABLE IC. BUSYZ Low to SCRUBZ Low Delay Variation.

(Voltage = 1.8 V, Temperature = -55°C to 125°C)

VALUE	MAX (ns)
0000	80
0001	180
0010	270
0011	370
0100	460
0101	600
0110	650
0111	800
1000	900
1001	1000
1010	1200
1011	1300
1100	1400
1101	1500
1110	1600
1111	1600

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-11237**

SHEET  
**22**

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C<sub>IN</sub> and C<sub>OUT</sub> measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL C	SHEET 23

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in (method 1015)	Required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1	1Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7	1, 7
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B shall test the functionality of the device.

4/ \* indicates PDA applies to subgroup 1 and 7.

5/ \*\* see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Symbol	Limit	Unit
Supply current standby at 0 MHz	I <sub>DD2</sub> (SB)	± 10% of specified value in Table I or 35 μA whichever is greater 2/	μA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ If device is tested at or below 35 μA, no deltas are required.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
C

**5962-11237**

SHEET  
24



4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL <b>C</b>	SHEET 25

6.7 Notes.

EDAC Control Register Programming 1/ 2/

ADDR BIT	PARAMETER	VALUE	FUNCTION
A [3:0]	Scrub rate – Rates are approximate and will vary with temperature and voltage conditions as well as process parameters	0-15	As SCRUB rate changes from 0 – 15, then the interval between SCRUB cycles will change as follows: 0 = N/A            6 = 222 kHz        11 = 7 kHz 1 = N/A            7 = 111 kHz        12 = 3.5 kHz 2 = N/A            8 = 55 kHz         13 = 1.75 kHz 3 = N/A            9 = 28 kHz         14 = 0.875 kHz 4 = 888 kHz      10 = 14 kHz        15 = 0.433 kHz 5 = 444 kHz See Table III
A [7:4]	BUSYZ to SCRUBZ – Delays are approximate and will vary with temperature and voltage conditions as well as process parameters	0-15	If A[7:4] changes from 0 to 15, the interval t <sub>BLSL</sub> between falling edges of BUSYZ and SCRUBZ will change as follows: 0 = 80 ns            6 = 480 ns        11 = 820 ns 1 = 160 ns          7 = 560 ns        12 = 880 ns 2 = 220 ns          8 = 620 ns        13 = 960 ns 3 = 280 ns          9 = 680 ns        14 = 1020 ns 4 = 360 ns          10 = 760 ns       15 = 1080 ns 5 = 420 ns See Table IV
A [8]	EDAC bypass bit	0/1	0: Enable EDAC 1: Disable EDAC including scrub
A [11]	Scrub enable bit	0/1	0: Enable scrub 1: Disable scrub
A [12]	SE/DE indication bit	0/1	0: MBE indicates multiple-bit error 1: MBE indicates single-bit error

Notes:

- 1/ A(10:9) must be '00' during control register programming according to EDAC Function Select Truth Table in Figure 3.
- 2/ A(18:13) are don't care.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-11237</b>
		REVISION LEVEL C	SHEET 26

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-17

Approved sources of supply for SMD 5962-11237 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-1123701VXC	01295	SMV512K32HFG

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln.  
PO Box 660199  
Dallas, TX 75243

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