REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 07, 08, 09, 10, 11, and 12. Delete radiation exposure circuit. - ro	12-03-30	C. SAFFLE
B	Add device types 13, 14, 15 and 16 for vendor CAGE 65342. Remove class M references. - jt	14-03-10	C.SAFFLE

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
11-07-15

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, LINEAR, CMOS, MICROPROCESSOR SUPERVISORY CIRCUIT, MONOLITHIC SILICON

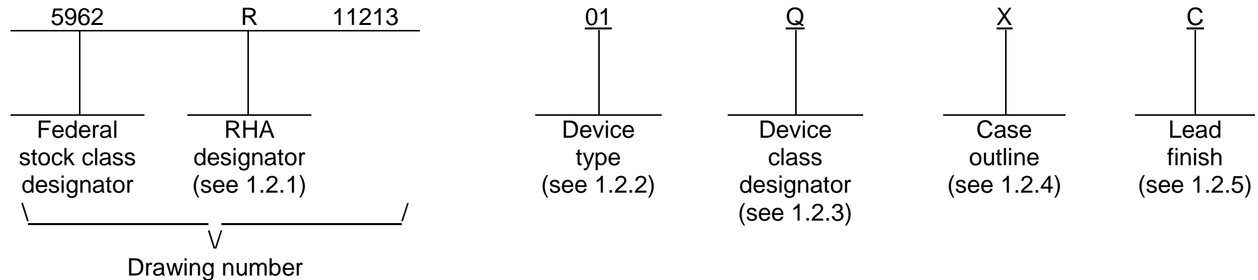
SIZE	CAGE CODE	
A	**67268**	**5962-11213**

SHEET 1 OF 33

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL705ARH	Radiation hardened, 5.0 V microprocessor supervisory circuit
02	ISL705BRH	Radiation hardened, 5.0 V microprocessor supervisory circuit
03	ISL705CRH	Radiation hardened, 5.0 V microprocessor supervisory circuit
04	ISL706ARH	Radiation hardened, 3.3 V microprocessor supervisory circuit
05	ISL706BRH	Radiation hardened, 3.3 V microprocessor supervisory circuit
06	ISL706CRH	Radiation hardened, 3.3 V microprocessor supervisory circuit
07	ISL705AEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
08	ISL705BEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
09	ISL705CEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
10	ISL706AEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
11	ISL706BEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
12	ISL706CEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
13	UT01VS50L	Radiation hardened, 5.0 V microprocessor supervisory circuit
14	UT01VS50D	Radiation hardened, 5.0 V microprocessor supervisory circuit
15	UT01VS33L	Radiation hardened, 3.3 V microprocessor supervisory circuit
16	UT01VS33D	Radiation hardened, 3.3 V microprocessor supervisory circuit

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) .... 0.3 V to 6.5 V
All other inputs .... -0.3 V to (V_{DD} + 0.3 V)
Power dissipation (P_D) .... 2.5 W
Lead temperature (soldering, 10 seconds) .... +300°C
Junction temperature (T_J) .... +175°C
Storage temperature range .... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) .... 15°C/W
Thermal resistance, junction-to-ambient (θ_{JA}) .... 140°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}):
Device types 01, 02, 03, 07, 08, 09, 13, 14 .... 4.75 V to 5.5 V
Device types 04, 05, 06, 10, 11, 12, 15, 16 .... 3.15 V to 3.6 V
Ambient operating temperature range (T_A) .... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rads(Si)/s):
Device types 01, 02, 03, 04, 05, 06 .... 100 krads (Si) 2/
Device types 07, 08, 09, 10, 11, 12 .... 100 krads (Si) 3/
Device types 13, 14, 15, 16 ……………………………………………... 300 krads (Si) 4/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):
Device types 07, 08, 09, 10, 11, 12 .... 50 krads(Si) 3/
Single event phenomenon (SEP)
No single event latch-up (SEL) occurs to effective LET (see 4.4.4.2)
Device types 01-12 ………………………………………………………. ≤ 86 $MeV/mg/cm^2$ 5/
Device types 13, 14, 15, 16... ≤ 110 $MeV/mg/cm^2$ 5/

The manufacturer supplying RHA device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 12 on this drawing has performed characterization testing to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1. Therefore these parts may be considered ELDRS free at a level of 100 krads(Si). The manufacturer will perform only high dose rate testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, condition A for device types 01, 02, 03, 04, 05, and 06. The manufacturer will perform high dose rate and low dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, conditions A and D for device types 07, 08, 09, 10, 11, and 12.

______

2/ The manufacturer supplying device types 01, 02, 03, 04, 05, and 06 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a level of 100 krads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).

3/ The manufacturer supplying device types 07, 08, 09, 10, 11, and 12 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

4/ The manufacturer supplying device types 13, 14, 15 and 16 guaranteed by design that the device does not contain bipolar transistor elements. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified with MIL-STD-883 method 1019, condition A to a maximum total dose of 300 krads (Si). The manufacturer will perform high dose rate lot acceptance testing on a lot by lot basis in accordance with MIL-STD-883, method 1019, conditions A for device types 13, 14, 15 and 16.

5/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but, are not production tested. See manufacturer's SEE test report for more information.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of this documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Operating supply voltage	V_{DD}			1,2,3	01,02, 03,07 08,09 13,14	1.2	5.5	V
					04,05, 06,10, 11,12, 15,16	1.2	3.6	
Supply current	I_{DD}	V_{DD} = 5.5 V		1,2,3	01,02, 03,07,		530	µA
			M,D,P,L,R 2/ M,D,P,L,R,F	1	08,09, 13,14		530	
		V_{DD} = 3.6 V		1,2,3	04,05, 06,10,		400	
			M,D,P,L,R 2/	1	11,12		400	
		VDD = 3.6 V		1, 2, 3	15, 16		450	
			M,D,P,L,R,F 2/	1			450	
Reset section								
Reset threshold voltage	V_{rt}			1,2,3	01,02, 03,07,	4.50	4.75	V
			M,D,P,L,R 2/ M,D,P,L,R,F	1	08,09 13,14	4.50	4.75	
				1,2,3	04,05, 06,10,	3.0	3.15	
			M,D,P,L,R 2/ M,D,P,L,R,F	1	11,12, 15,16	3.0	3.15	
Reset threshold voltage hysteresis	V_{RTHYS}			1,2,3	All	20		mV
			M,D,P,L,R 2/ M,D,P,L,R,F	1		20		
Reset pulse width	T_{rs}	V_{DD} = 4.75 V		9,10,11	All	140	280	ms
			M,D,P,L,R 2/ M,D,P,L,R,F	9		140	280	
Reset output voltage	V_{OUT}	V_{DD} = 4.75 V, 3/ I_{SOURCE} = 800 µA		1,2,3	01,02, 03,07,	V_{DD} – 1.5		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1	08,09, 13,14	V_{DD} – 1.5		
		V_{DD} = 4.75 V, I_{SINK} = 3.2 mA		1,2,3			0.4	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Reset section – continued.								
Reset output voltage	V_{OUT}	V_{DD} = 3.15 V, 3/ I_{SOURCE} = 500 μA		1,2,3	04,05, 06,10	0.8 x V_{DD}		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1	11,12, 15, 16	0.8 x V_{DD}		
		V_{DD} = 3.15 V, I_{SINK} = 1.2 mA		1,2,3			0.3	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.3	
		V_{DD} = 1.2 V, I_{SINK} = 100 μA		1,2,3	01,03, 04,06,		0.3	
			M,D,P,L,R 2/ M,D,P,L,R,F	1	07,09, 10,12, 13, 14, 15, 16		0.3	
		V_{DD} = 1.2 V, I_{SOURCE} = 4 μA		1,2,3	02,05,	0.9		
			M,D,P,L,R 2/	1	08,11	0.9		
Reset output leakage current	I_{LEAK}	V_{OUT} = V_{DD}		1,2,3	03,06,		1	μA
			M,D,P,L,R 2/ M,D,P,L,R,F	1	09,12, 14,16		1	
Watchdog section								
Watchdog time-out period	t_{WD}	V_{DD} = 5.5 V		9,10,11	01,02, 03,07,	1.00	2.25	s
			M,D,P,L,R 2/ M,D,P,L,R,F	9	08,09, 13,14	1.00	2.25	
		V_{DD} = 3.6 V		9,10,11	04,05, 06,10,	1.00	2.25	
			M,D,P,L,R 2/ M,D,P,L,R,F	9	11,12, 15,16	1.00	2.25	
Watchdog input (WDI) pulse width	t_{WP}	V_{DD} = 4.75 V, V_{IL} = 0.4 V, V_{IH} = 0.8 x V_{DD}		9,10,11	01,02, 03,07,	50		ns
			M,D,P,L,R 2/ M,D,P,L,R,F	9	08,09, 13, 14	50		
		V_{DD} = 3.15 V, V_{IL} = 0.4 V, V_{IH} = 0.8 x V_{DD}		9,10,11	04,05, 06,10,	100		
			M,D,P,L,R 2/ M,D,P,L,R,F	9	11,12, 15,16	100		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Watchdog section – continued.								
Watchdog input (WDI) threshold voltage	V_{IL}	V_{DD} = 4.75 V		1,2,3	01,02, 03,07, 08,09, 13, 14		0.8	V
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.8	
		V_{DD} = 3.15 V		1,2,3	04,05, 06,10, 11,12, 15,16		0.6	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.6	
	V_{IH}	V_{DD} = 5.5 V		1,2,3	01,02, 03,07, 08,09, 13,14	3.5		
			M,D,P,L,R 2/ M,D,P,L,R,F	1		3.5		
		V_{DD} = 3.6 V		1,2,3	04,05, 06,10, 11,12, 15,16	0.7 x V_{DD}		
			M,D,P,L,R 2/ M,D,P,L,R,F	1		0.7 x V_{DD}		
Watchdog input (WDI) current	I_{WDI}	WDI pin = V_{DD} = 5.5 V		1,2,3	01,02, 03,07, 08,09		100	µA
			M,D,P,L,R 2/	1			100	
		WDI pin = V_{DD} = 5.5 V		1,2,3	13, 14		35	
			M,D,P,L,R, F 2/	1			35	
		WDI pin = 0 V, V_{DD} = 5.5 V		1,2,3	01,02, 03, 07, 08,09	-100		
			M,D,P,L,R 2/	1		-100		
		WDI pin = 0 V, V_{DD} = 5.5 V		1,2,3	13,14	-35		
			M,D,P,L,R,F 2/	1		-35		
		WDI pin = V_{DD} = 3.6 V		1,2,3	04,05, 06,10, 11,12		5	
			M,D,P,L,R 2/	1			5	
		WDI pin = V_{DD} = 3.6		1,2,3	15, 16		20	
			M,D,P,L,R,F 2/	1			20	
		WDI PIN = 0 V, V_{DD} = 3.6V		1,2,3	04,05, 06,10, 11,12	-5		
			M,D,P,L,R 2/	1		-5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Watchdog section - continued.								
Watchdog input (WDI) current	I_{WDI}	WDI pin = 0 V, V_{DD} = 3.6 V		1, 2, 3	15, 16	-20		µA
			M,D,P, L,R,F 2/	1		-20		
Watchdog output $\overline{WDO}$ voltage	$V_{\overline{WDO}}$	V_{DD} = 4.75 V, I_{SOURCE} = 800 µA		1,2,3	01,02, 03,07, 08,09 13, 14	V_{DD} – 1.5		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1		V_{DD} – 1.5		
		V_{DD} = 4.75 V, I_{SINK} = 1.2 mA		1,2,3			0.4	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.4	
Watchdog output $\overline{WDO}$ voltage	$V_{\overline{WDO}}$	V_{DD} = 3.15 V, I_{SOURCE} = 500 µA		1,2,3	04,05, 06,10, 11,12 15,16	0.8 x V_{DD}		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1		0.8 x V_{DD}		
		V_{DD} = 3.15 V, I_{SINK} = 500 µA		1,2,3			0.3	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Manual reset section							
Manual reset ($\overline{MR}$) pull-up current	$I_{\overline{MR}}$	$\overline{MR}$ = 0 V, V_{DD} = 5.5 V	1,2,3	01,02, 03,07,	-500	-100	µA
		M,D,P,L,R 2/ M,D,P,L,R,F	1	08,09 13,14	-500	-100	
		$\overline{MR}$ = 0 V, V_{DD} = 3.6 V	1,2,3	04,05, 06,10,	-250	-25	
		M,D,P,L,R 2/ M,D,P,L,R,F	1	11,12 15,16	-250	-25	
Manual reset ($\overline{MR}$) pulse width	$t_{\overline{MR}}$	V_{DD} = 4.75 V	9,10,11	01,02, 03,07,	150		ns
		M,D,P,L,R 2/ M,D,P,L,R,F	9	08,09 13,14	150		
		V_{DD} = 3.15 V	9,10,11	04,05, 06,10,	150		
		M,D,P,L,R 2/ M,D,P,L,R,F	9	11,12 15,16	150		
Manual reset ($\overline{MR}$) input threshold voltage	V_{IL}	V_{DD} = 4.75 V	1,2,3	01,02, 03,07,		0.8	V
		M,D,P,L,R 2/ M,D,P,L,R,F	1	08,09 13,14		0.8	
		V_{DD} = 3.15 V	1,2,3	04,05, 06,10,		0.6	
		M,D,P,L,R 2/ M,D,P,L,R,F	1	11,12 15,16		0.6	
	V_{IH}	V_{DD} = 5.5 V	1,2,3	01,02, 03,07,	2.0		
		M,D,P,L,R 2/ M,D,P,L, R,F	1	08,09 13,14	2.0		
		V_{DD} = 3.6 V	1,2,3	04,05, 06,10,	0.7 x V_{DD}		
		M,D,P,L,R 2/ M,D,P,L,R,F	1	11, 12, 15,16	0.7 x V_{DD}		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Manual reset section – continued.								
Manual reset ($\overline{MR}$) to reset out delay	t_{MD}			9,10,11	All		100	ns
			M,D,P,L,R 2/ M,D,P,L,R,F	9			100	
Threshold detector section								
Threshold detector input (PFI) threshold voltage	V_{PFI}	V_{DD} = 5.0 V		1,2,3	01,02, 03,07, 08,09, 13,14	1.20	1.30	V
			M,D,P,L,R 2/ M,D,P,L,R,F	1		1.20	1.30	
		V_{DD} = 3.3 V		1,2,3	04,05, 06,10, 11,12, 15,16	0.576	0.624	
			M,D,P,L,R 2/ M, D,P,L,R,F	1		0.576	0.624	
Threshold detector input (PFI) current	I_{PFI}			1,2,3	01, 02,03, 04,05, 06,07, 08,09, 10,11, 12	-10.0	+10.0	nA
			M,D,P,L,R 2/	1		-10.0	+10.0	
Threshold detector input (PFI) current	I_{PFI}	4/		1, 2, 3	13,14, 15,16	-20.0	+20.0	
			M,D,P,L,R,F 2/ 4/	1		-20.0	+20.0	
Threshold detector output ($\overline{PFO}$) voltage	V_{PFO}	V_{DD} = 4.75 V, I_{SOURCE} = 800 μA		1,2,3	01,02, 03,07, 08,09, 13,14	V_{DD} – 1.5		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1		V_{DD} – 1.5		
		V_{DD} = 4.75 V, I_{SINK} = 3.2 mA		1,2,3			0.4	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Threshold detector section - continued.								
Threshold detector output ($\overline{PFO}$) voltage	V_{PFO}	V_{DD} = 3.15 V, I_{SOURCE} = 500 µA		1, 2, 3	04,05, 06,10, 11,12 15,16	0.8 x V_{DD}		V
			M,D,P,L,R 2/ M,D,P,L,R,F	1		0.8 x V_{DD}		
		V_{DD} = 3.15 V, I_{SINK} = 1.2 mA		1,2,3			0.3	
			M,D,P,L,R 2/ M,D,P,L,R,F	1			0.3	
PFI rising threshold crossing to PFO delay	t_{RPFI}			9,10,11	01,02, 03,07, 08,09, 13, 14		15	µs
			M,D,P,L,R 2/ M,D,P,L,R,F	9			15	
				9,10,11	04,05 06,10, 11,12 15,16		20	
			M,D,P,L,R 2/ M,D,P,L,R,F	9			20	
PFI falling threshold crossing to PFO delay	t_{FPFI}			9,10,11	01,02, 03,07, 08,09 13,14		35	µs
			M,D,P,L,R 2/ M,D,P,L,R,F	9			35	
				9,10,11	04,05, 06,10, 11,12, 15,16		40	
			M,D,P,L,R 2/ M,D,P,L,R,F	9			40	

1/ Unless otherwise specified, V_{DD} = 4.75 V to 5.5 V for devices 01, 02, 03, 07, 08, 09,13 and 14 V_{DD} = 3.15 V to 3.6 V for devices 04, 05, 06, 10, 11, 12,15 and 16. Reset is the only parameter operable within 1.2 V and the minimum recommended operating supply voltage.

TABLE IA. Electrical performance characteristics – Continued.

2/ RHA device types 01, 02, 03, 04, 05, and 06 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation. However, device types 01, 02, 03, 04, 05, and 06 are only tested at the R level in accordance with MIL-STD-883, method 1019, condition A (see 1.5 herein).

RHA device types 07, 08, 09, 10, 11, and 12 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation for condition A and M, D, P, and L for condition D. However, device types 07, 08, 09, 10, 11, and 12 are only tested at the R level in accordance with MIL-STD-883, method 1019, condition A and tested at the L level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

The manufacturer supplying device types 13, 14, 15 and 16 guaranteed by design that the device does not contain bipolar transistor elements. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified with MIL-STD-883 method 1019, condition A to a maximum total dose of 300 krads (Si). The manufacturer will perform high dose rate lot acceptance testing on a lot by lot basis in accordance with MIL-STD-883, method 1019, conditions A for device types 13, 14, 15 and 16.

Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ For device types 03 and 09, a 1.54 kΩ was used as the pull up resistance value. For device types 06 and 12, a 1.02 kΩ was used as the pull up resistance value.

4/ For device types 13, 14, 15 and 16: Guaranteed by design but not tested.

TABLE IB. SEP test limits. 1/, 2/

Device type	SEP	Temperature (T_C)	Bias V_{DD}	No SEL, effective linear energy transfer (LET)
01, 02, 03, 07, 08, 09	SEL	+125°C	5.5 V	≤ 86 MeV-cm^2/mg 3/
04, 05, 06, 10, 11, 12	SEL	+125°C	3.6 V	≤ 86 MeV-cm^2/mg 3/
13, 14	SEL	+125°C	5.5 V	≤110MeV- cm^2/mg 4/
15, 16	SEL	+125°C	3.6 V	≤110MeV- cm^2/mg 4/

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Guaranteed by design or process but not tested.
4/ Tested for initial qualification.

Case X

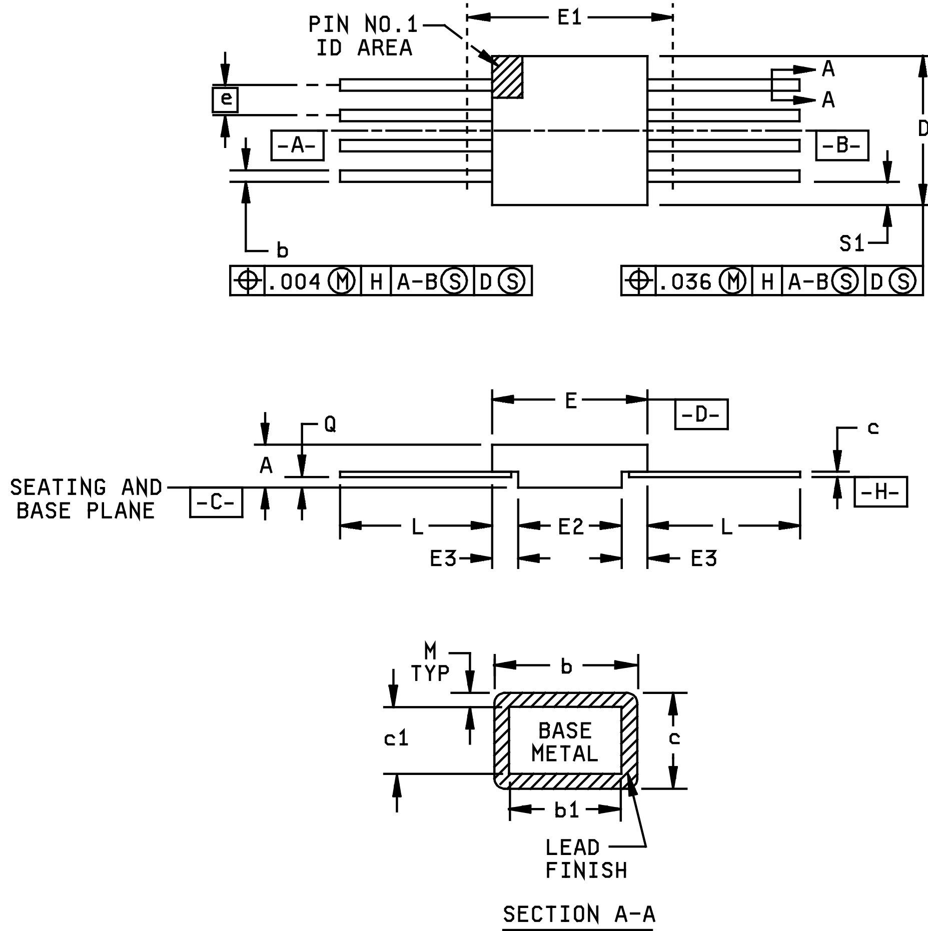


FIGURE 1. Case outline.

Case X

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.070	0.115	1.18	2.92	
b	0.015	0.022	0.38	0.56	
b1	0.015	0.019	0.38	0.48	
c	0.004	0.009	0.10	0.23	
c1	0.004	0.007	0.10	0.18	
D	0.245	0.265	6.22	6.73	4
E	0.245	0.265	6.22	6.73	
E1	---	0.280	---	7.11	4
E2	0.170	0.180	4.32	4.57	
E3	0.030	---	0.76	---	8
e	0.050 BSC		1.27 BSC		
k	---	---	---	---	3
L	0.250	0.370	6.35	9.40	
Q	0.026	0.045	0.66	1.14	9
S1	0.005	---	0.13	---	7
M	---	0.0015	---	0.04	
N	8		8		

NOTES:

1. The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
6. N is the maximum number of terminal positions.
7. Measure dimension S1 at all four corners.
8. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
9. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outline – Continued.

Device type	01, 04, 07, 10, 13, 15	02, 05, 08, 11	03, 06, 09, 12, 14, 16
Case outline	X		
Terminal number	Terminal symbol		
1	$\overline{MR}$	$\overline{MR}$	$\overline{MR}$
2	V_{DD}	V_{DD}	V_{DD}
3	GND	GND	GND
4	PFI	PFI	PFI
5	$\overline{PFO}$	$\overline{PFO}$	$\overline{PFO}$
6	WDI	WDI	WDI
7	$\overline{RST}$	RST	$\overline{RST_OD}$
8	$\overline{WDO}$	$\overline{WDO}$	$\overline{WDO}$

FIGURE 2. Terminal connections.

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APR 97

Terminal symbol	Description
$\overline{MR}$	Manual reset input. An active low TTL/CMOS compatible (150 ns minimum pulse width) input that may be used to generate a reset pulse.
V_{DD}	Power supply voltage. Connect the voltage to be monitored to this pin.
GND	Ground. This pin should be tied to power ground. It establishes the reference for voltage detection.
PFI	Threshold detector input. The input pin for the threshold detector, which may be used to monitor a power fail or low battery condition, or for monitoring other voltage supply levels.
$\overline{PFO}$	Threshold detector output. A low active output that indicates that the input connected to the PFI pin is less than V_{PFI}.
WDI	Watchdog input. A three state watchdog input that monitors microprocessor activity. If the microprocessor does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not three stated, $\overline{WDO}$ goes low. As long as $\overline{RST}$ is asserted of the WDI input is three stated, the watchdog timer will stay cleared and will not count. As soon as the reset is released and WDI is driven high or low, the timer will start counting. Floating WDI or connecting WDI to a high impedance three state buffer disables the watchdog feature (WDON = “1”).
$\overline{RST}$	Reset. On power up, once V_{DD} reaches 1.2 V, $\overline{RST}$ is guaranteed logic low. As V_{DD} rises, $\overline{RST}$ stays low. When V_{DD} rises above the reset threshold, 4.65 V (typical), an internal timer releases $\overline{RST}$ after about 200 ms. $\overline{RST}$ pulses low whenever V_{DD} goes below the reset threshold. If this brownout condition occurs in the middle of a previously initiated reset pulse, the pulse will continue for at least 140 ms. On power-down, once V_{DD} falls below the reset threshold, $\overline{RST}$ stays low and is guaranteed low until V_{DD} drops below 1.2 V.
RST	Reset. RST is an active high, push pull output. RST is guaranteed to be logic high once V_{DD} reaches 1.2 V. RST is the inverse of $\overline{RST}$.
$\overline{RST_OD}$	Reset. $\overline{RST_OD}$ is an active low, open drain output that goes low when reset is asserted. This pin may be pulled up to V_{DD} with a resistor consistent with the sink and leakage current specifications of the output. Behavior is otherwise identical to the $\overline{RST}$ pin.
$\overline{WDO}$	Watchdog output. This output goes low if the microprocessor does not toggle the WDI input within 1.6 seconds and WDI is not three stated. This pin is usually connected to the non-maskable interrupt input of the microprocessor. When V_{DD} drops below V_{rt}, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. $\overline{RESET}$ goes low simultaneously, thus preventing an interrupt. If WDI is left unconnected, $\overline{WDO}$ can be used as low line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{DD} drops below V_{rt}, thus functioning as a low line output.

FIGURE 2. Terminal connections – Continued.

Device types 01, 04, 07, 10, 13 and 15.

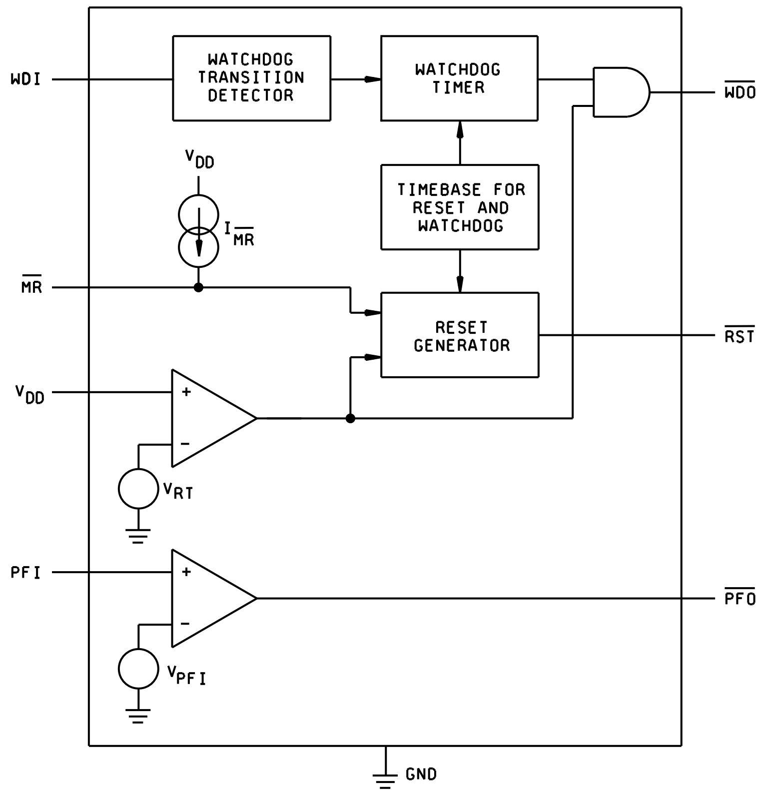


FIGURE 3. Block diagram.

Device types 02, 05, 08, and 11.

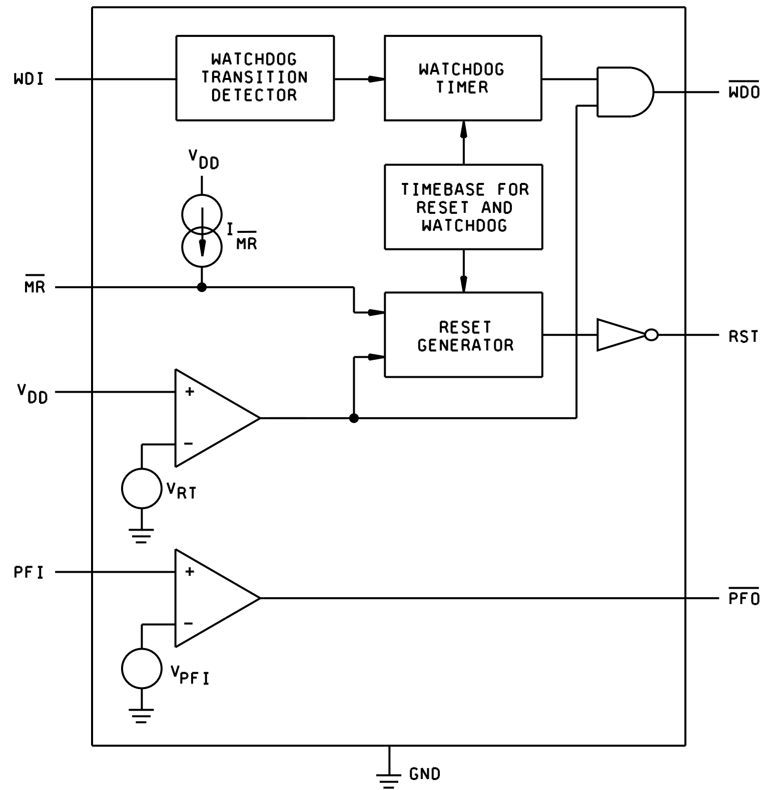


FIGURE 3. Block diagram - continued.

Device types 03, 06, 09, 12, 14 and 16.

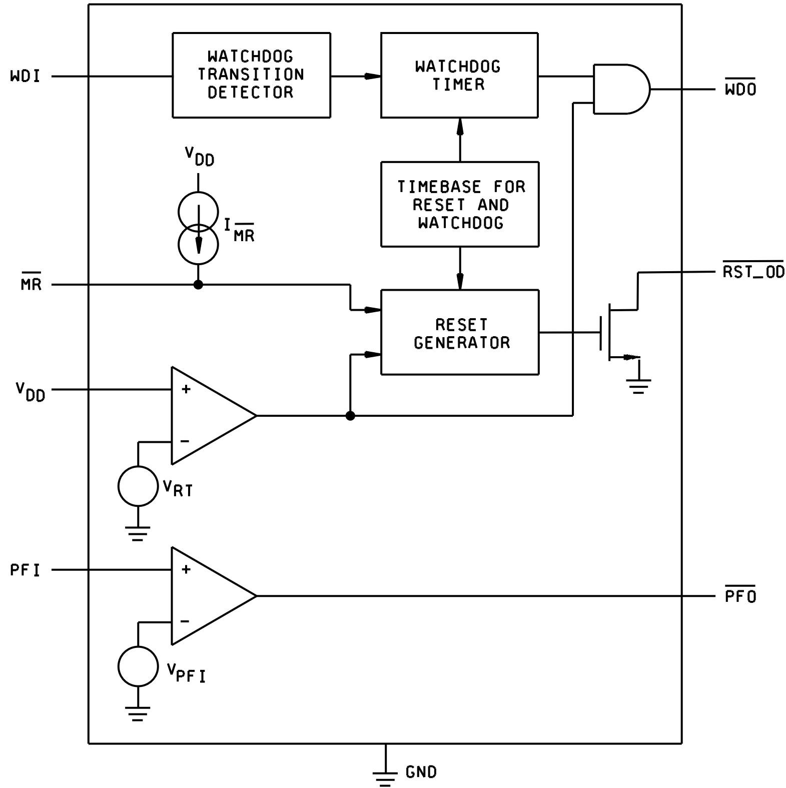


FIGURE 3. Block diagram - continued.

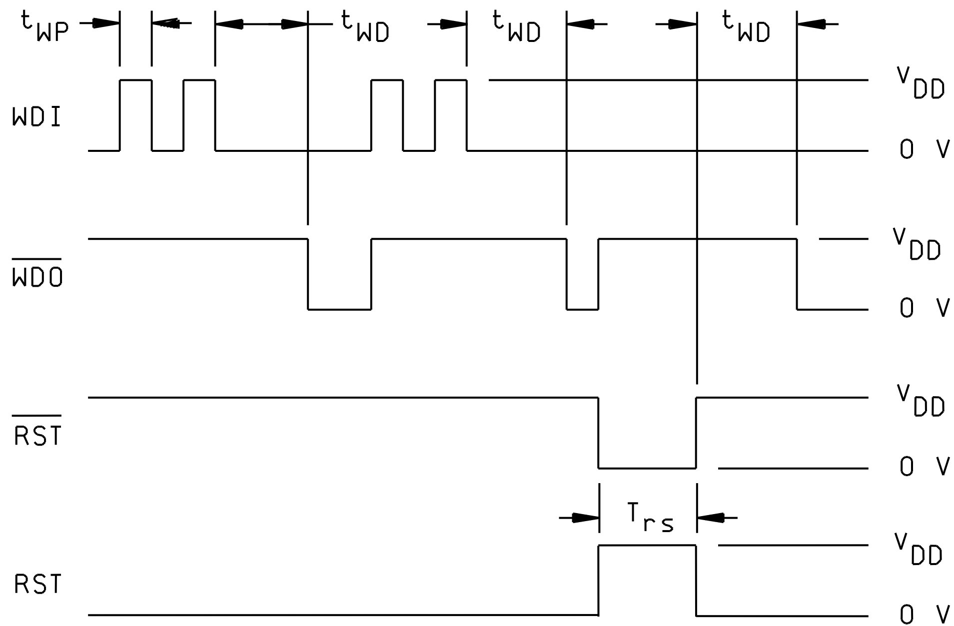


FIGURE 4. Timing waveforms.

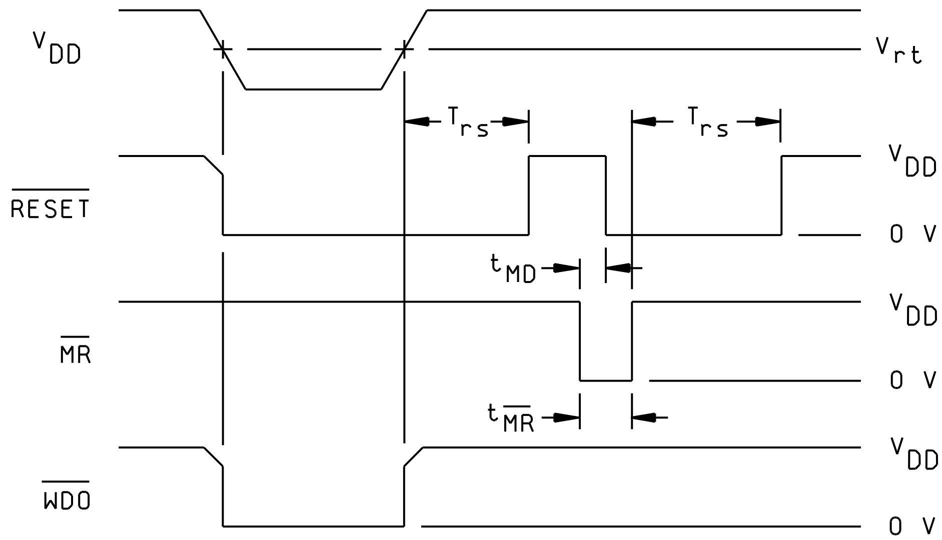


FIGURE 4. Timing waveforms – continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,9	1,9
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1, 2, 3, 2/, 3/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 3/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 9, and deltas.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Delta limits
Supply current	I_{DD}	±10%

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein for device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, 13 14, 15 and 16. In addition for device types 07, 08, 09, 10, 11, and 12 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post anneal end point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (for example, 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be for device types 01, 02, 03, 07, 08, 09, 13 and 14 V_{DD} = 5.5 V, for device types 04, 05, 06, 10, 11, 12,15 and 16 V_{DD} = 3.6 V for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

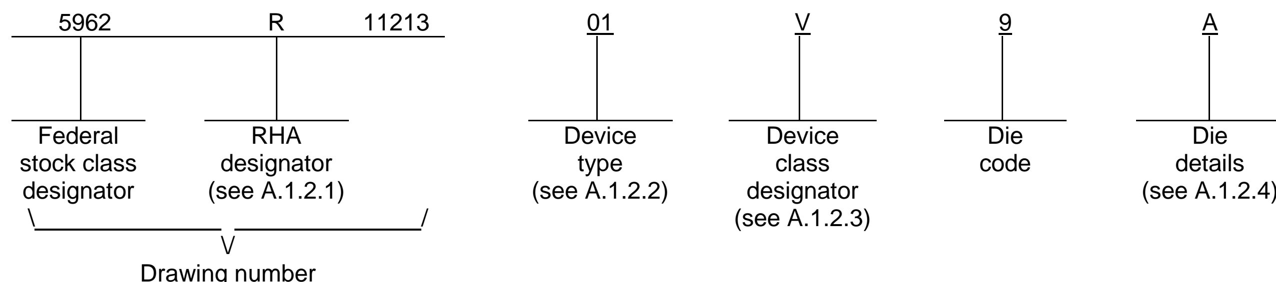
b. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-11213

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL705ARH	Radiation hardened, 5.0 V microprocessor supervisory circuit
02	ISL705BRH	Radiation hardened, 5.0 V microprocessor supervisory circuit
03	ISL705CRH	Radiation hardened, 5.0 V microprocessor supervisory circuit
04	ISL706ARH	Radiation hardened, 3.3 V microprocessor supervisory circuit
05	ISL706BRH	Radiation hardened, 3.3 V microprocessor supervisory circuit
06	ISL706CEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
07	ISL705AEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
08	ISL705BEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
09	ISL705CEH	Radiation hardened, 5.0 V microprocessor supervisory circuit
10	ISL706AEH	Radiation hardened, 3.3V microprocessor supervisory circuit
11	ISL706BEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
12	ISL706CEH	Radiation hardened, 3.3 V microprocessor supervisory circuit
13	UT01VS50L	Radiation hardened, 5.0 V Microprocessor supervisory circuit

A.1.2.2 Device types. The device types identify the circuit function as follows – continued:

Device type	Generic number	Circuit function
14	UT01VS50D	Radiation hardened, 5.0 V microprocessor supervisory circuit
15	UT01VS33L	Radiation hardened, 3.3V microprocessor supervisory circuit
16	UT01VS33D	Radiation hardened, 3.3 V microprocessor supervisory circuit

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad locations and related electrical functions, interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1
13, 14, 15, 16	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1
13, 14, 15, 16	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1
13, 14, 15, 16	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1
13, 14, 15, 16	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.1.1, and 4.4.4.2.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

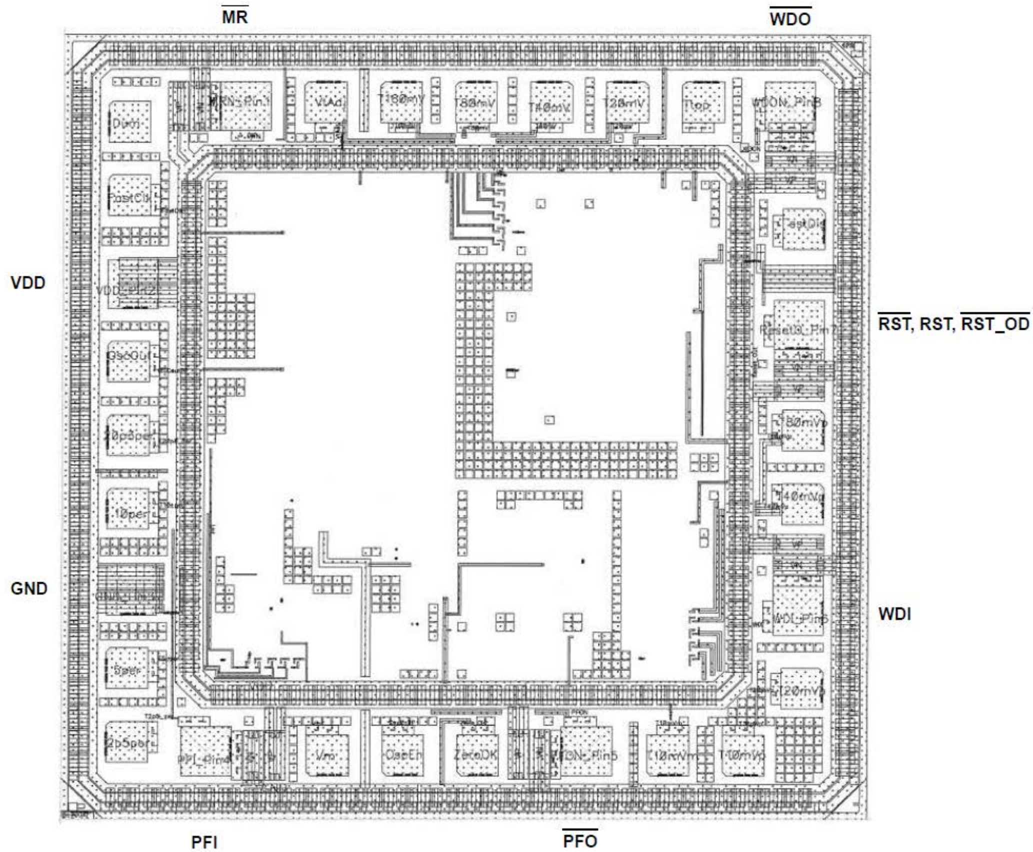
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
Die size: 79.9 mils x 79.9 mils (2030 μm x 2030 μm).
Die thickness: 19 mils ±1 mils (483 μm +/-25.4 μm).

Interface materials.
Top metallization: Al Cu
Thickness: 2.7 μm +/-0.4 μm
Backside metallization: None

Glassivation.
Type: Silicon Nitride (Si_3N_4) over Silicon Oxide (SiO_2)
Silicon Nitride thickness: 1.2 μm ±0.12 μm
Silicon Oxide thickness: 0.3 μm ±0.03 μm

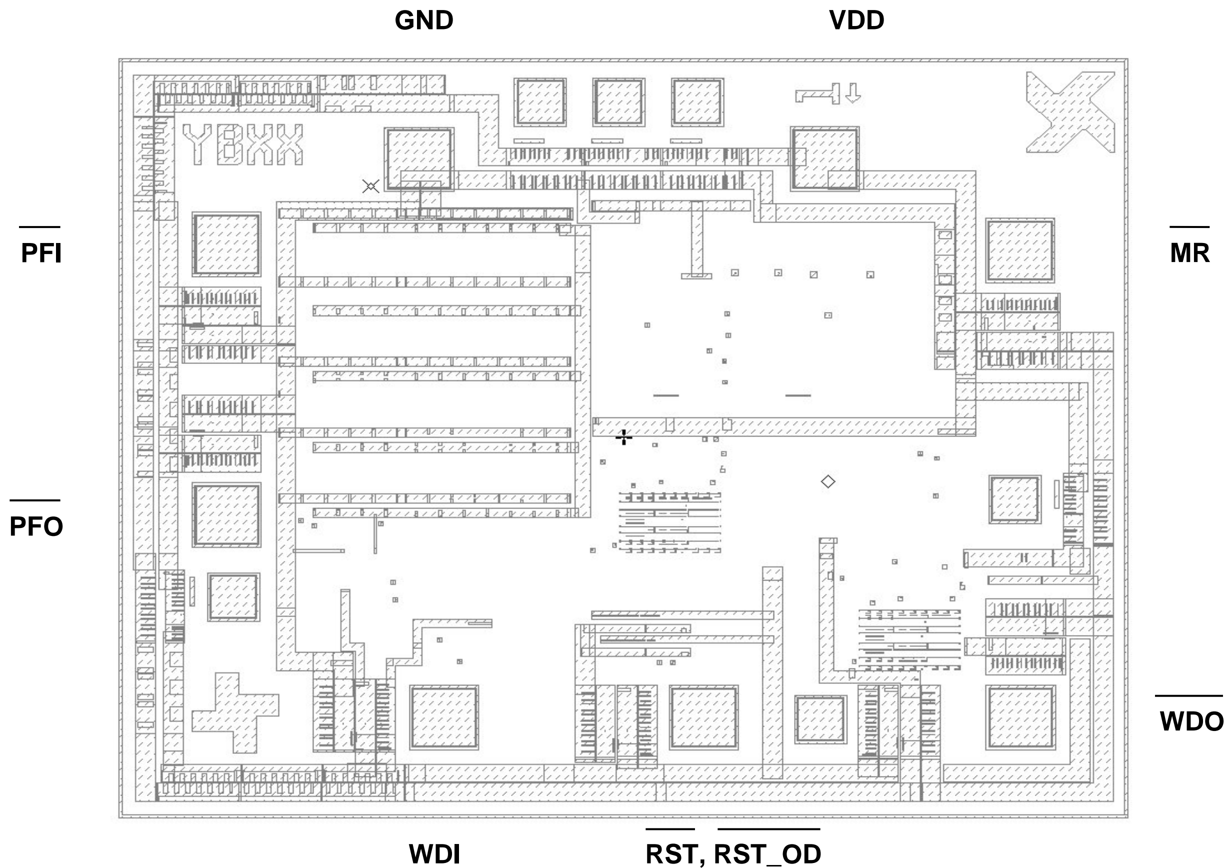
Process: 0.6μ BiCMOS JI (junction isolated)

Assembly related information.
Substrate potential: Unbiased. (May be left floating or connected to GND).
Special assembly instructions: None
Packaged Device Weight: 0.31 grams (typical)

FIGURE A-1. Die bonding pad locations and electrical functions.

APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-11213



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
Die size: 69.3 mils x 56.3 mils (1760 µm x 1430 µm).
Die thickness: 17.5 mils ±1 mils (444.5 µm +/- 25.4 µm).

Interface materials.
Top metallization: Al Cu
Thickness: Contact Manufacturer
Backside metallization: None

Glassivation.
Type: Silicon Nitride (Si_3N_4) over Silicon Oxide (SiO_2)
Silicon Nitride thickness: Contact Manufacturer
Silicon Oxide thickness: Contact Manufacturer

Process: 0.35 µm CMOS JI (Triple- Well Junction Isolated CMOS)

Assembly related information.
Substrate potential: Unbiased. (May be left floating or connected to GND).
Special assembly instructions: None
Packaged Device Weight: 0.45 grams (typical)

Figure A-2. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-03-10

Approved sources of supply for SMD 5962-11213 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1121301QXC	34371	ISL705ARHQF
5962R1121301VXC	34371	ISL705ARHVF
5962R1121301V9A	34371	ISL705ARHVX
5962R1121302QXC	34371	ISL705BRHQF
5962R1121302VXC	34371	ISL705BRHVF
5962R1121302V9A	34371	ISL705BRHVX
5962R1121303QXC	34371	ISL705CRHQF
5962R1121303VXC	34371	ISL705CRHVF
5962R1121303V9A	34371	ISL705CRHVX
5962R1121304QXC	34371	ISL706ARHQF
5962R1121304VXC	34371	ISL706ARHVF
5962R1121304V9A	34371	ISL706ARHVX
5962R1121305QXC	34371	ISL706BRHQF
5962R1121305VXC	34371	ISL706BRHVF
5962R1121305V9A	34371	ISL706BRHVX
5962R1121306QXC	34371	ISL706CRHQF
5962R1121306VXC	34371	ISL706CRHVF
5962R1121306V9A	34371	ISL706CRHVX
5962R1121307VXC	34371	ISL705AEHVF
5962R1121307V9A	34371	ISL705AEHVX
5962R1121308VXC	34371	ISL705BEHVF
5962R1121308V9A	34371	ISL705BEHVX
5962R1121309VXC	34371	ISL705CEHVF
5962R1121309V9A	34371	ISL705CEHVX
5962R1121310VXC	34371	ISL706AEHVF
5962R1121310V9A	34371	ISL706AEHVX

DATE: 14-03-10

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1121311VXC	34371	ISL706BEHVF
5962R1121311V9A	34371	ISL706BEHVX
5962R1121312VXC	34371	ISL706CEHVF
5962R1121312V9A	34371	ISL706CEHVX
5962R1121313QXC	65342	UT01VS50LRXQC
5962F1121313QXC	65342	UT01VS50LFXQC
5962R1121314QXC	65342	UT01VS50DRXQC
5962F1121314QXC	65342	UT01VS50DFXQC
5962R1121315QXC	65342	UT01VS33LRXQC
5962F1121315QXC	65342	UT01VS33LFXQC
5962R1121316QXC	65342	UT01VS33DRXQC
5962F1121316QXC	65342	UT01VS33DFXQC
5962R1121313VXC	65342	UT01VS50LRXVC
5962F1121313VXC	65342	UT01VS50LFXVC
5962R1121314VXC	65342	UT01VS50DRXVC
5962F1121314VXC	65342	UT01VS50DFXVC
5962R1121315VXC	65342	UT01VS33LRXVC
5962F1121315VXC	65342	UT01VS33LFXVC
5962R1121316VXC	65342	UT01VS33DRXVC
5962F1121316VXC	65342	UT01VS33DFXVC
5962R1121313V9A	65342	UT01VS50LR-V-DIE
5962F1121313V9A	65342	UT01VS50LF-V-DIE
5962R1121314V9A	65342	UT01VS50DR-V-DIE
5962F1121314V9A	65342	UT01VS50DF-V-DIE
5962R1121315V9A	65342	UT01VS33LR-V-DIE
5962F1121315V9A	65342	UT01VS33LF-V-DIE
5962R1121316V9A	65342	UT01VS33DR-V-DIE
5962F1121316V9A	65342	UT01VS33DF-V-DIE
5962R1121313Q9A	65342	UT01VS50LR-Q-DIE
5962F1121313Q9A	65342	UT01VS50LF-Q-DIE
5962R1121314Q9A	65342	UT01VS50DR-Q-DIE
5962F1121314Q9A	65342	UT01VS50DF-Q-DIE
5962R1121315Q9A	65342	UT01VS33LR-Q-DIE

DATE: 14-03-10

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1121315Q9A	65342	UT01VS33LF-Q-DIE
5962R1121316Q9A	65342	UT01VS33DR-Q-DIE
5962F1121316Q9A	65342	UT01VS33DF-Q-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.