REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to paragraph 3.2.4. Added V_{OH}/V_{OL} test circuit to figure 4 and renamed. Reference figure 4 in Table IA. Changes to paragraph 4.2.1c (1), Table IIA and Table IIB. Added CGA requirements per MIL-PRF-38535. - glg	14-09-08	Charles Saffle
B	Change CGA package outline X column diameter (dimension b, Min/Max) from 0.46/0.56mm to 0.43/0.59mm. - glg	16-04-22	Charles Saffle
C	Updated V_{OH2}/ V_{OL2} test conditions in table IA. Corrected pin description G2 on figure 2 terminal connections. Updated table IB SEP test limits for SEU based on actual test report. Added 4.4.3.1 subgroup 5 salt atmosphere test paragraph. Updated paragraph 4.4.4.3a to reflect RHA plan. - glg	19-10-01	James Eschmeyer

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Laura Leeper

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
12-12-19

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4M X 18-bit, 1.8 VOLT, 2-WORD AND 4-WORD BURST, RADIATION HARDENED, SYNCHRONOUS STATIC RANDOM ACCESS MEMORY (SSRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-11201**

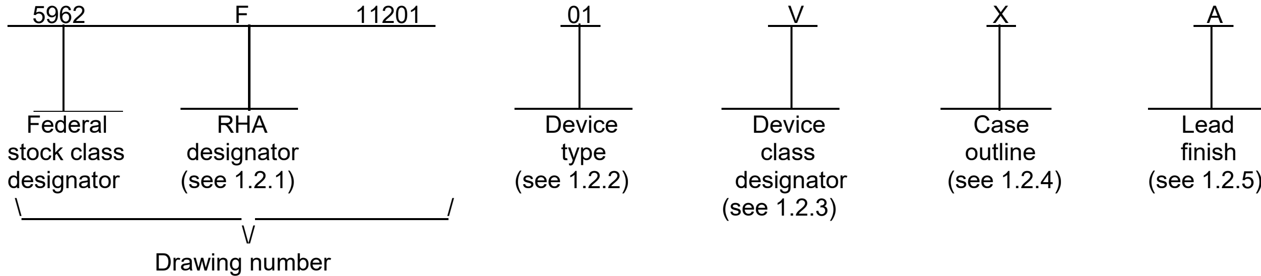
SHEET 1 OF 30

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Maximum Operating Frequency
01	1542AV18-250	4M X 18-bit rad-hard SSRAM 2-word burst	250 MHz
02	1543AV18-250	4M X 18-bit rad-hard SSRAM 4-word burst	250 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	165	Ceramic column grid array (CCGA) 1/

1/ Terminal lead finish A is tin-lead alloy. Package case outline X solder column material is Sn= 20% and Pb=80%.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD})	-0.5 V dc to + 2.9 V dc
Supply voltage range to outputs (V_{DDQ})	-0.5 V dc to V_{DD} 3/
Reference supply voltage (V_{REF})	0.95 V dc 4/
DC voltage range on any input	-0.5 V dc to V_{DD} + 0.3 V dc 5/
DC voltage range on any output pin in High-Z	-0.5 V dc to V_{DDQ} + 0.3 V dc
Current into outputs (Low)	20 mA
Storage temperature range	-65ºC to +150ºC
Case temperature range, (T_C)	-55ºC to +125ºC
Maximum junction temperature (T_J)	150ºC 6/
Lead temperature (soldering, 10 seconds)	+260º
Thermal resistance, junction-to-case (Θ_{JC})	8.9º C/W 7/
Maximum power dissipation (P_D)	
01	3.23 W
02	2.42 W
Maximum operating supply current (V_{DD} + V_{DDQ}) = I_{DD}	
01	1700 mA
02	1275 mA
Maximum operating frequency	
01	250 MHz
02	250 MHz

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	1.7 V dc to 1.9 V dc
Supply voltage to outputs (V_{DDQ})	1.4 V dc to V_{DD} 3/
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	V_{REF} + 0.1 V dc to V_{DDQ} + 0.3 V dc 4/ 5/
Input low voltage range (V_{IL})	-0.3 V dc to V_{REF} – 0.1 V dc 4/ 5/
Case operating temperature range (T_C)	-55ºC to +125ºC 6/

1.5 Radiation features

Maximum total dose available (Dose rate = 50-300 rads(Si)/s)	300 Krads(Si)
Single event phenomenon (SEP) :	
No SEL occurs at effective LET(see 4.4.4.4)	≤ 120 MeV-cm^2/mg 8/
No SEU occurs at on set LET (see 4.4.4.4)	≤ 0.13 MeV-cm^2/mg 8/
(Single event upset rate =1.34 x 10^{-7} errors/bit-day)	
Dose rate induced upset	2.0 x 10^9 rad(Si)/sec 8/
Dose rate induced latch-up survivability	1.5 x 10^{11} rad(Si)/sec 8/
Neutron irradiation	2.0 x 10^{14} n/cm^2 8/

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ $V_{DDQ} \leq V_{DD}$ at all times.

4/ V_{REF}(Min) = 0.68V or 0.46V_{DDQ}, whichever is larger. V_{REF}(Max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.

5/ Overshoot: V_{IH}(AC) < V_{DDQ} +0.85V (Pulse width less than t_{CYC}/2), Undershoot: V_{IL}(AC) > -1.5V (Pulse width less than t_{CYC}/2).

6/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

7/ Tested initially and after any design or process changes which may affect this parameter.

8/ Typical. Contact the device manufacturer for detailed lot information.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org).

JEDEC Solid State Technology Association (JEDEC)

JESD 78 - IC Latch-Up Test.
JEDEC MO-158 BE-1 - Microelectronic Outlines

(Copies of this document are available online at https://www.jedec.org).

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of this document are available from https://standards.ieee.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.1.1 Solderability test for CGA packages. Solderability testing for case outline X for CGA packages have been verified during the solder column attachment process in accordance with method 2003 of MIL-STD-883.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load and V_{OH}/V_{OL} test circuit. The output load and V_{OH}/V_{OL} test circuit shall be as specified on figure 4.

3.2.5 Block diagram. The block diagram shall be as specified on figure 5.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 6.

3.2.7 Radiation test circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in Appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 IEEE 1149.1 Serial Boundary Scan (JTAG). The SRAMs described in this document incorporate a serial boundary scan Test Access Port (TAP). This feature is fully compliant with IEEE Standard 1149.1-2001. The TAP operates using standard 1.8V I/O logic levels.

3.10.1 Disabling the JTAG feature. It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied to LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively connect to V_{DD} through a pull-up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55° \le T_C \le +125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Output HIGH Voltage 4/ 5/	V_{OH1}	I_{OH} = -0.1 mA, 50 ohm impedance See figure 4	1, 2, 3	All	V_{DDQ} -0.20	V_{DDQ}	V
Output LOW Voltage 4/ 5/	V_{OL1}	I_{OL} = 0.1 mA, 50 ohm impedance See figure 4	1, 2, 3	All	V_{SS}	0.20	V
Output HIGH Voltage 6/	V_{OH2}	I_{OH} = -2.0 mA, 50 ohm impedance $V_{DD(Min)}$ = 1.3V, $V_{DD(Max)}$ = 1.5V See figure 4	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Output LOW Voltage 6/	V_{OL2}	I_{OL} = 2.0 mA, 50 ohm impedance $V_{DD(Min)}$ = 0.0V, $V_{DD(Max)}$ = 0.3V See figure 4	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Input HIGH Voltage 7/	V_{IH}		1, 2, 3	All	V_{REF} +0.1	V_{DDQ} +0.3	V
Input LOW Voltage 7/	V_{IL}		1, 2, 3	All	-0.3	V_{REF} -0.1	V
Input Reference Voltage 8/	V_{REF}	Typical value = 0.75 V	1, 2, 3	All	0.68	0.95	V
Input Leakage Current	I_X	$GND \le V_I \le V_{DDQ}$	1, 2, 3	All	-20	20	uA
Output Leakage Current	I_{OZ}	$GND \le V_I \le V_{DDQ}$, output disabled	1, 2, 3	All	-20	20	uA
V_{DD} Operating Supply Current	I_{DD}	V_{DD} = max, I_{OUT} = 0 mA $f = f_{MAX} = 1/t_{CYC}$	1, 2, 3	01, 03		1700	mA
				02, 04		1275	mA
Automatic CE Power-Down Current	I_{SB1}	V_{DD} = max, both ports deselected, inputs static $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ $f = f_{MAX} = 1/t_{CYC}$	1, 2, 3	01, 03		660	mA
				02, 04		570	mA
Input Capacitance 9/	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8, V_{DDQ} = 1.5V See 4.4.1e	4	All		10	pF
Clock Input Capacitance 9/	C_{CLK}		4	All		10	pF
Output Capacitance 9/	C_{OUT}		4	All		10	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits Min	Limits Max	Units
Functional tests		T_A = 25°C , See 4.4.1e	7, 8A, 8B	All			
K Clock Cycle Time	t_{CYC}	See Figure 5 as applicable. 10/ 11/	9, 10, 11	All	4.0	8.4	ns
Input Clock (K/$\overline{K}$) HIGH	t_{KH}		9, 10, 11	All	1.6	---	ns
Input Clock (K/$\overline{K}$) LOW	t_{KL}		9, 10, 11	All	1.6	---	ns
K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	$t_{KH\overline{K}H}$		9, 10, 11	All	1.8	---	ns
Address Setup to K Clock Rise	t_{SA}		9, 10, 11	All	0.5	---	ns
Control Setup to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	t_{SC}		9, 10, 11	All	0.5	---	ns
Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS}_0$, $\overline{BWS}_1$ $\overline{BWS}_2$, $\overline{BWS}_3$)	t_{SCDDR}		9, 10, 11	All	0.5	---	ns
$D_{[x:O]}$ Setup to Clock (K/$\overline{K}$) Rise	t_{SD}		9, 10, 11	All	0.5	---	ns
Address Hold after K Clock Rise	t_{HA}		9, 10, 11	All	0.5	---	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions -55° ≤ T_C ≤ 125°C 1.7 V ≤ V_{DD} ≤ 1.9 V 1.4V ≤ V_{DDQ} ≤ V_{DD} Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Control Hold after to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	t_{HC}	See Figure 5 as applicable 10/ 11/	9, 10, 11	All	0.5	---	ns
Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$ $\overline{BWS_2}$, $\overline{BWS_3}$)	t_{HCDDR}		9, 10, 11	All	0.5	---	ns
$D_{[x:0]}$ Hold after Clock (K/$\overline{K}$) Rise	t_{HD}		9, 10, 11	All	0.5	---	ns
K/$\overline{K}$ Clock Rise to Data Valid	t_{CO}		9, 10, 11	All	---	0.85	ns
Data Output Hold after Output K/$\overline{K}$ Clock Rise (Active to Active)	t_{DOH}		9, 10, 11	All	-0.85	---	ns
K/$\overline{K}$ Clock Rise to Echo Clock Valid	t_{CCQO}		9, 10, 11	All	---	0.85	ns
Echo Clock Hold after C/$\overline{C}$ Clock Rise	t_{CQOH}		9, 10, 11	All	-0.85	---	ns
Echo Clock High to Data Valid	t_{CQD}		9, 10, 11	All	---	0.50	ns
Echo Clock High to Data Invalid	t_{CQDOH}		9, 10, 11	All	-0.30	---	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4\ V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Min	
Output Clock ($CQ/\overline{CQ}$) High 12/	t_{CQH}	See Figure 5 as applicable. 10/ 11/	9, 10, 11	All	1.55	---	ns
CQ Clock High to $\overline{CQ}$ Clock Rise (rising edge to rising edge) 12/	$t_{CQH\overline{CQ}H}$		9, 10, 11	All	1.55	---	ns
Clock ($K/\overline{K}$) Rise to High-Z (Active to High-Z) 13/ 14/	t_{CHZ}		9, 10, 11	All	---	0.45	ns
Clock ($K/\overline{K}$) Rise to Low-Z 7/ 13/ 14/	t_{CLZ}		9, 10, 11	All	-0.45	---	ns
Echo Clock High to QVLD Valid 15/	t_{QVLD}		9, 10, 11	All	-0.5	0.5	ns
Clock Phase Jitter	$t_{KC\ Var}$		9, 10, 11	All	---	0.20	ns
DLL Lock Time (K)	$t_{KC\ Lock}$		9, 10, 11	All	10240	---	cycles
K static to DLL reset	$t_{KC\ Reset}$		9, 10, 11	All	30	---	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

1/ All voltage referenced to ground.
2/ Power up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time, $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
3/ RHA parts supplied to this drawing have been characterized through all levels M, D, P, L, R and F of irradiation. However, these devices are only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
4/ Outputs are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
5/ Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
6/ Tested limits for V_{OH2} are MIN=1.3V, MAX=1.5V for 50 Ohm termination and -2mA output current. Tested limits for V_{OL2} are MIN=0.0V, MAX=0.3V for 50 Ohm termination and 2mA output current.
7/ Parameters guaranteed by characterization but not production tested.
8/ V_{REF}(min) = 0.68V or 0.46 V_{DDQ}, whichever is larger, V_{REF}(max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.
9/ Tested initially and after any design or process changes that may affect these parameters.
10/ Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 4(a), AC test loads.
11/ When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timing of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
12/ These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ – 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
13/ t_{CHZ} and t_{CLZ} are specified with a load capacitance of 5 pF as in Figure 4(b), AC test loads. Transition is measured ±100 mV from steady-state voltage.
14/ At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} is less than t_{CO}.
15/ t_{QVLD} spec is applicable to both rising and falling edges of QVLD signal.

Table IB. SEP test limits 1/ 2/

Device type	Single Event Upset 3/ V_{DD} = 1.7 V, V_{DD} = 1.4 V		Single Event Latch-up 4/ V_{DD} = 1.9 V, V_{DDQ} = 1.9 V
	Effective LET No upsets [MeV/(mg/cm^2)] 5/	Maximum device cross section(cm^2)	Effective LET No latch-up [MeV/(mg/cm^2)]
All	0.13	1.5 x 10^{-7}	120

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature T_A = +25°C ±10°C.
4/ Worst case test temperature T_A = +125°C ±10°C.
5/ For single event upset rate = 1.34 x 10^{-7} errors/bit-day (SEU rate 17.18 device-day/events) consider geosynchronous orbit CREME96.

Case outline X

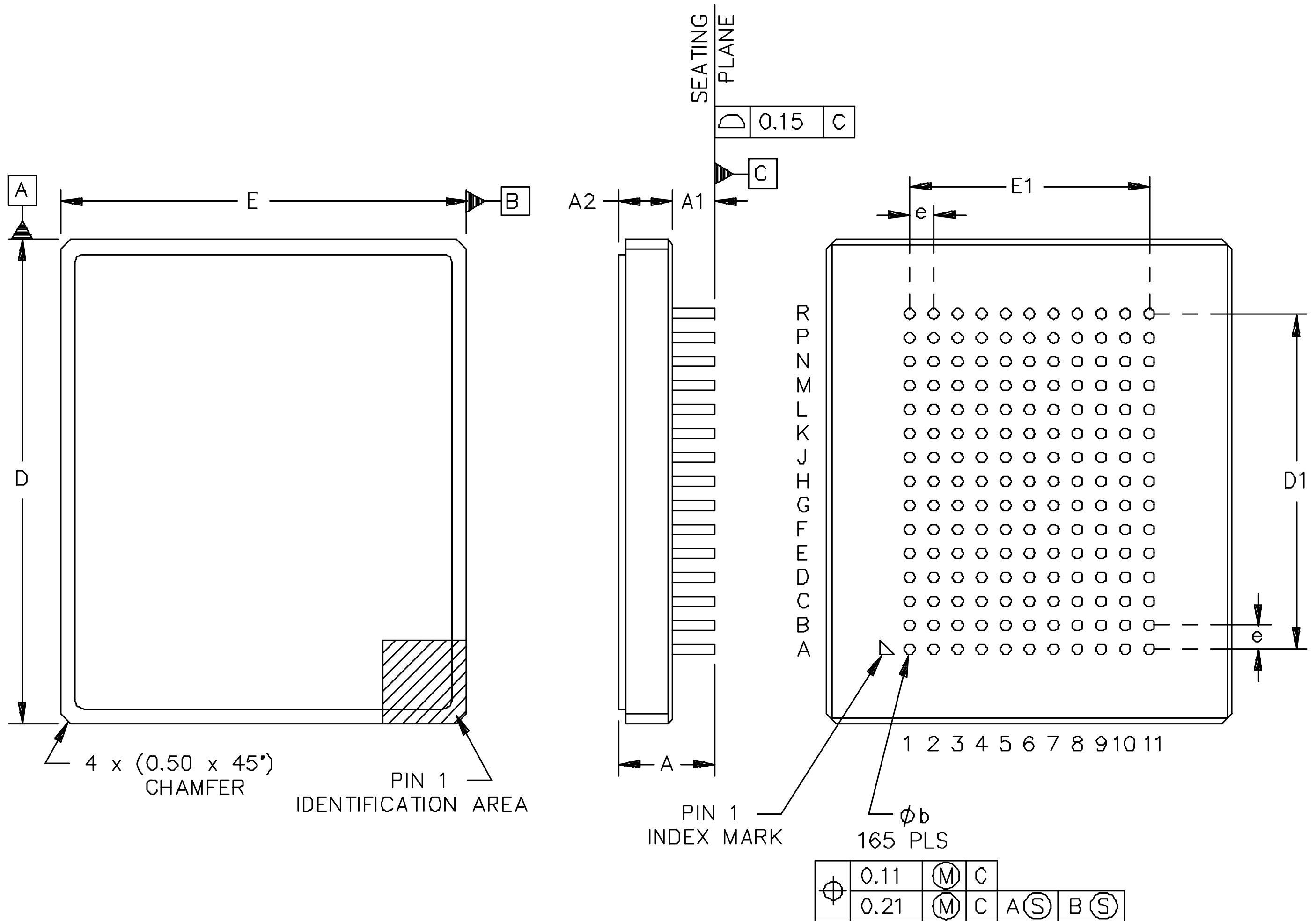


FIGURE 1. Case outline.

Case outline X

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.38		0.212
A1	2.11	2.31	0.083	0.091
A2	2.59	3.07	0.102	0.121
b	0.43	0.59	0.017	0.023
e	1.27 BSC NOM		0.050	
D	24.75	25.25	0.974	0.994
D1	17.78 BSC NOM		0.700	
E	20.79	21.21	0.819	0.835
E1	12.70 BSC NOM		0.500	
N	165			

NOTES:
1. Index area: a notch or pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Reference JEDEC MO-158 BE-1 for lead pattern.

FIGURE 1. Case outline - continued.

Device type 01											
Case Outline= X											
	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Device type 02											
Case Outline= X											
	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

FIGURE 2. Terminal connections.

Pin Definitions

Pin	Name	Function
$D_{[x:0]}$	Input-Synchronous	**Data Input Signals**. Sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. Device Type= 01, 02: $D_{[17:0]}$.
$\overline{WPS}$	Input-Synchronous	**Write Port Select- Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$.
$\overline{BWS_0}$, $\overline{BWS_1}$	Input-Synchronous	**Byte Write Select 0 and 1 - Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. Device types 01, 02: S_0 controls D[8:0], S1 controls D[17:9]. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address Inputs.** Sampled on the rising edge of the K (Read address) and $\overline{K}$ (Write address) clocks during active read and write operations for device type 01 whereas sampled on the rising edge of the K clock during active read and write operations for device type 02. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 4M x 18 (2 arrays each of 2M x 18) for device type 01 and 4M x 18 (4 arrays each of 1M x 18) for device type 02. Therefore, 21 address inputs are needed to access the entire memory array of device type 01 and 20 address inputs for device type 02. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Output-Synchronous	**Data Output Signals.** These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of the K and $\overline{K}$ clocks during read operations. On deselecting the read port, Q[x:0] are automatically tri-stated. Device types 01, 02: Q[17:0]
$\overline{RPS}$	Input-Synchronous	**Read Port Select- Active LOW.** Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. De-asserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the K clock. Each read access consists of a burst of two sequential transfers for device type 01 whereas a burst of four sequential transfers for device type 02.
QVLD	Valid Output Indicator	**Valid Output Indicator.** The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through Q[x:0]. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through Q[x:0].
CQ	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics (Table IA).
$\overline{CQ}$	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics (Table IA).

FIGURE 2. Terminal connections - continued.

Pin Definitions - continued

Pin	Name	Function
ZQ	Input	**Output Impedance Matching Input.** This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off- Active LOW.** Connecting this pin to ground turns off the DLL inside the device. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR-I timing.
TDO	Output	**Test Data Out (TDO) for JTAG.**
TCK	Input	**Test Clock (TCK) Pin for JTAG.**
TDI	Input	**Test Data In (TDI) Pin for JTAG.**
TMS	Input	**Test Mode Select (TMS) Pin for JTAG**
NC, NC/144M, NC/288M	N/A	**Not Connected to the Die.** Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input.** Static input used to set reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device.**
V_{SS}	Ground	**Ground for the Device.**
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device.**

FIGURE 2. Terminal connections - continued.

Truth Table for device type 01 1/ 2/ 3/ 4/ 5/ 6/

Operation	K	RPSb	WPSb	DQ	DQ
Write Cycle: Load address on the rising edge of Kb clock; input write data on K and Kb rising edges.	L-H	X	L	D(A) at K(t) ↑	D(A + 1) at Kb (t) ↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K clock; wait one and a half cycle; read data on $\overline{K}$ and K rising edges.	L-H	L	X	Q(A) at K(t +2) ↑	Q(A + 1) at Kb (t +2) ↑
NOP: No Operation	L-H	H	H	D = X Q = High Z	D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

Write Cycle Descriptions for device type 01 1/ 7/

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L-H	-	During the data portion of a write sequence all four bytes ($D_{[17:0]}$) are written into the device.
L	L	-	L-H	During the data portion of a write sequence all four bytes ($D_{[17:0]}$) are written into the device.
L	H	L-H	-	During the data portion of a write sequence only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	-	L-H	During the data portion of a write sequence only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L-H	-	During the data portion of a write sequence only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]]}$ remains unaltered.
H	L	-	L-H	During the data portion of a write sequence only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0}$ remains unaltered.
H	H	L-H	-	No data is written into the devices during this portion of a write operation.
H	H	-	L-H	No data is written into the devices during this portion of a write operation.

1. X= "Don't Care," H = Logic HIGH, L= Logic LOW, ↑ represents rising edge.
2. Device powers up deselected with the outputs in a tri-state condition.
3. "A" represents address location latched by the devices when transaction was initiated. A + 1 represents the internal address sequence in the burst.
4. "t" represents the cycle at which a Read/Write operation is started. t + 1, and t + 2 are the first and second clock cycles respectively succeeding the "t' clock cycle.
5. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges.
6. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

FIGURE 3. Truth tables and device operations.

Truth Table for device type 02 1/ 2/ 3/ 4/ 5/ 6/

Operation	K	RPSb	WPSb	DQ	DQ	DQ	DQ
Write Cycle: Load address on the rising edge of K; input write data on two consecutive K and Kb rising edges.	L-H	H Note 7	L Note 8	D(A) at K(t+1) ↑	D(A + 1) at Kb(t+1) ↑	D(A+2) at K (t+2) ↑	D(A+3) at Kb (t+2) ↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K; wait two cycles; read data on two consecutive K and Kb rising edges.	L-H	L Note 8	X	Q(A) at K(t+2) ↑	Q(A+1) at Kb(t+2) ↑	Q(A+2) at K(t+3) ↑	Q(A+3) at Kb(t+3) ↑
NOP: No Operation	L-H	H	H	D = X	Q = High Z		D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State			Previous State

1. X= “Don’t Care,” H = Logic HIGH, L= Logic LOW, ↑ represents rising edge.
2. Device powers up deselected with the outputs in a tri-state condition.
3. “A” represents address location latched by the devices when transaction was initiated. A+1, A+2, and A+3 represent the internal address sequence in the burst.
4. “t” represents the cycle at which a Read/Write operation is started. t + 1, t+2 and t + 3 are the first, second and third clock cycles respectively succeeding the “t’ clock cycle.
5. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges, except when in single clock mode.
6. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If this signal was LOW to initiate the previous cycle, this signal becomes a “Don’t Care” for this operation.
8. This signal was HIGH on previous K clock rise. Initiating consecutive read or write operations on consecutive K clock rises is not permitted. The device ignores the second read or write request.

FIGURE 3. Truth tables and device operations - continued.

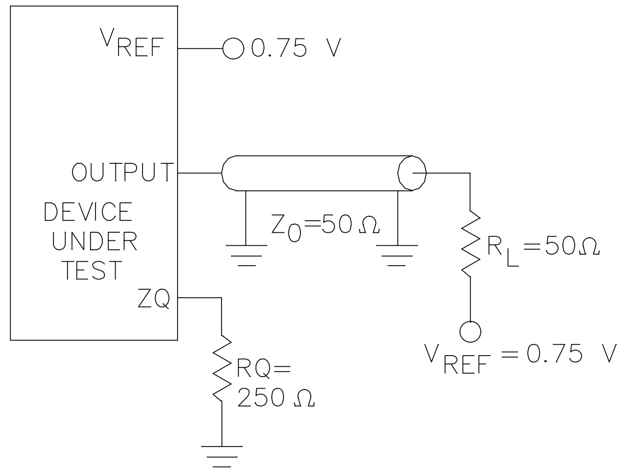
Write cycle descriptions for device type 02 1/ 2/

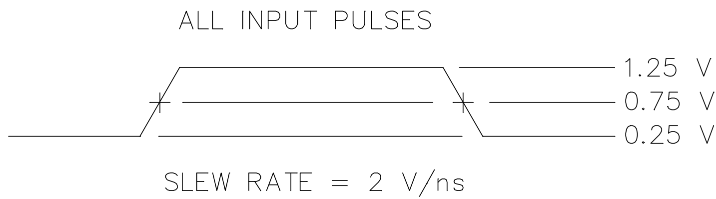
$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L-H	-	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	-	L-H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L-H	-	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[35:9]}$ remains unaltered.
L	H	H	H	-	L-H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[35:9]}$ remains unaltered.
H	L	H	H	L-H	-	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	-	L-H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L-H	-	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device, $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	-	L-H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device, $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L-H	-	During the data portion of a write sequence, only the lower byte ($D_{[35:27]}$) is written into the device, $D_{[26:0]}$ remains unaltered.
H	H	H	L	-	L-H	During the data portion of a write sequence, only the lower byte ($D_{[35:27]}$) is written into the device, $D_{[26:0]}$ remains unaltered.
H	H	H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L-H	No data is written into the device during this portion of a write operation.

1. X= "Don't Care," H = Logic HIGH, L= Logic LOW.
2. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

FIGURE 3. Truth tables and device operations - continued.

OUTPUT LOAD CIRCUIT





NOTE: 50Ω uniform transmission line terminated with a 50Ω load to VREF.

V_{OH}/V_{OL} TEST CIRCUIT

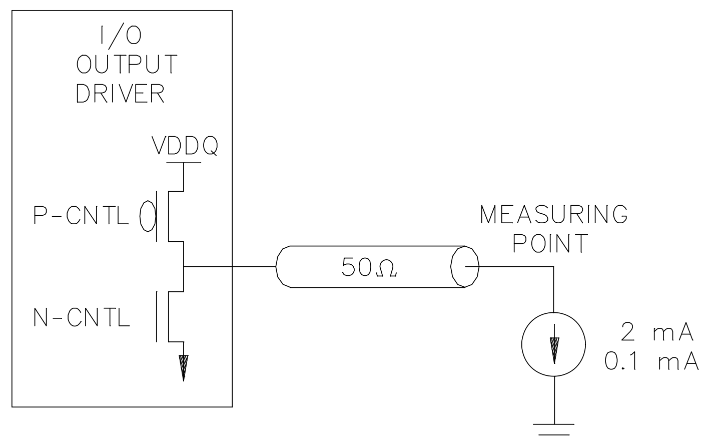


FIGURE 4. Output load circuit and V_{OH}/V_{OL} test circuit.

Device type 01

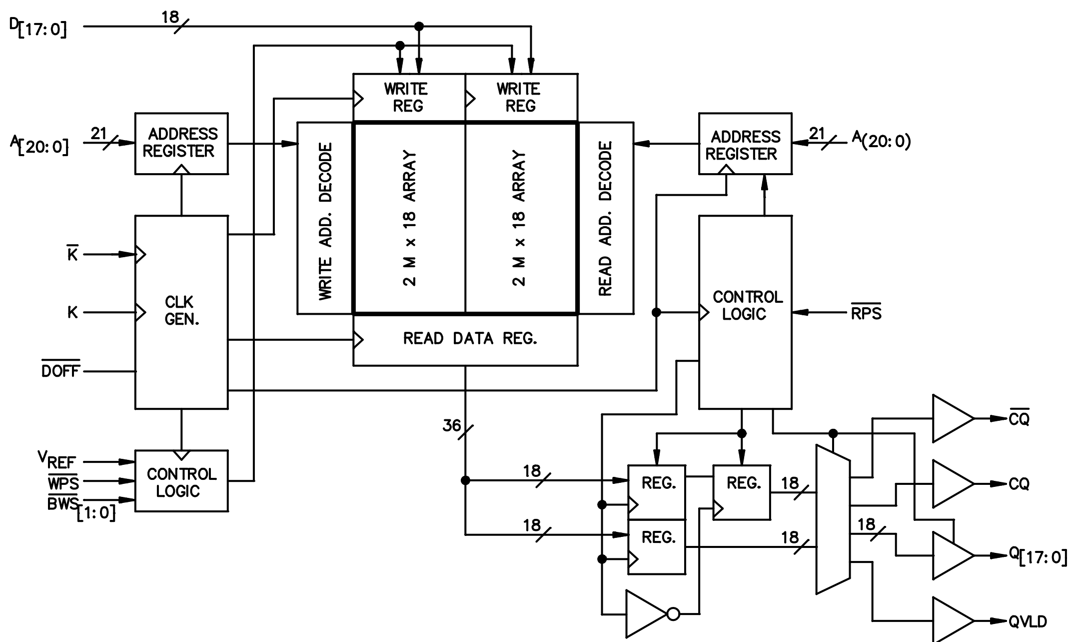


FIGURE 5. Block diagrams.

Device type 02

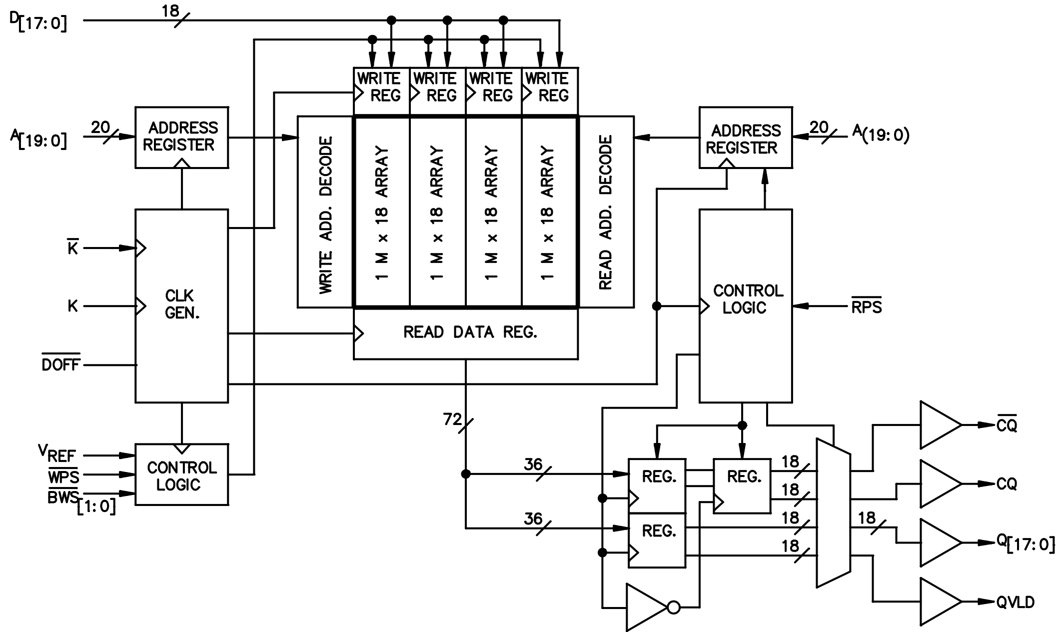


FIGURE 5. Block diagrams - continued.

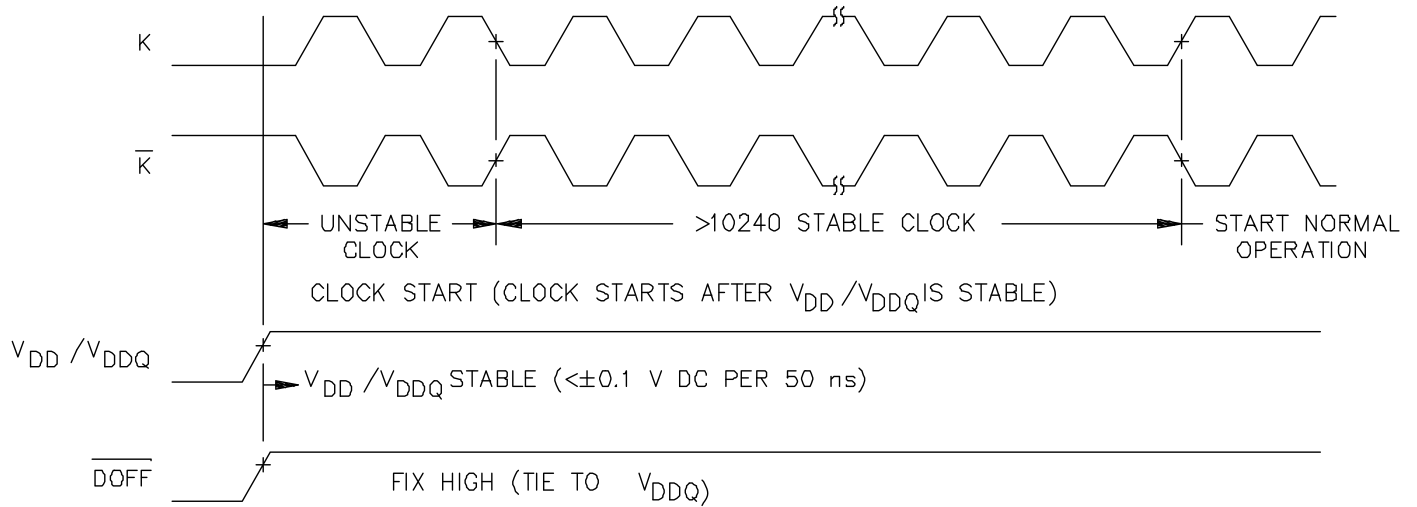
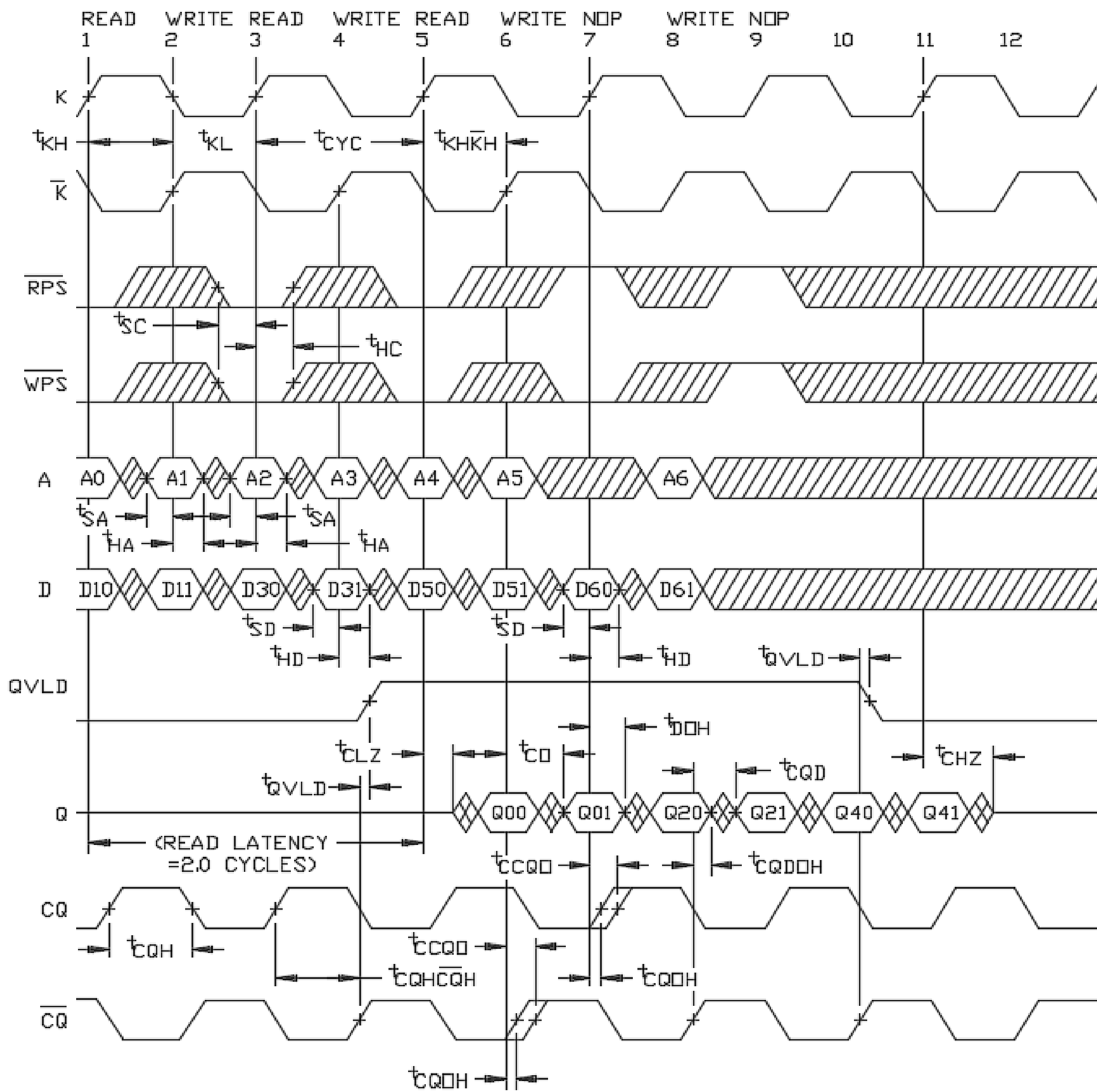


FIGURE 6. Timing waveforms.

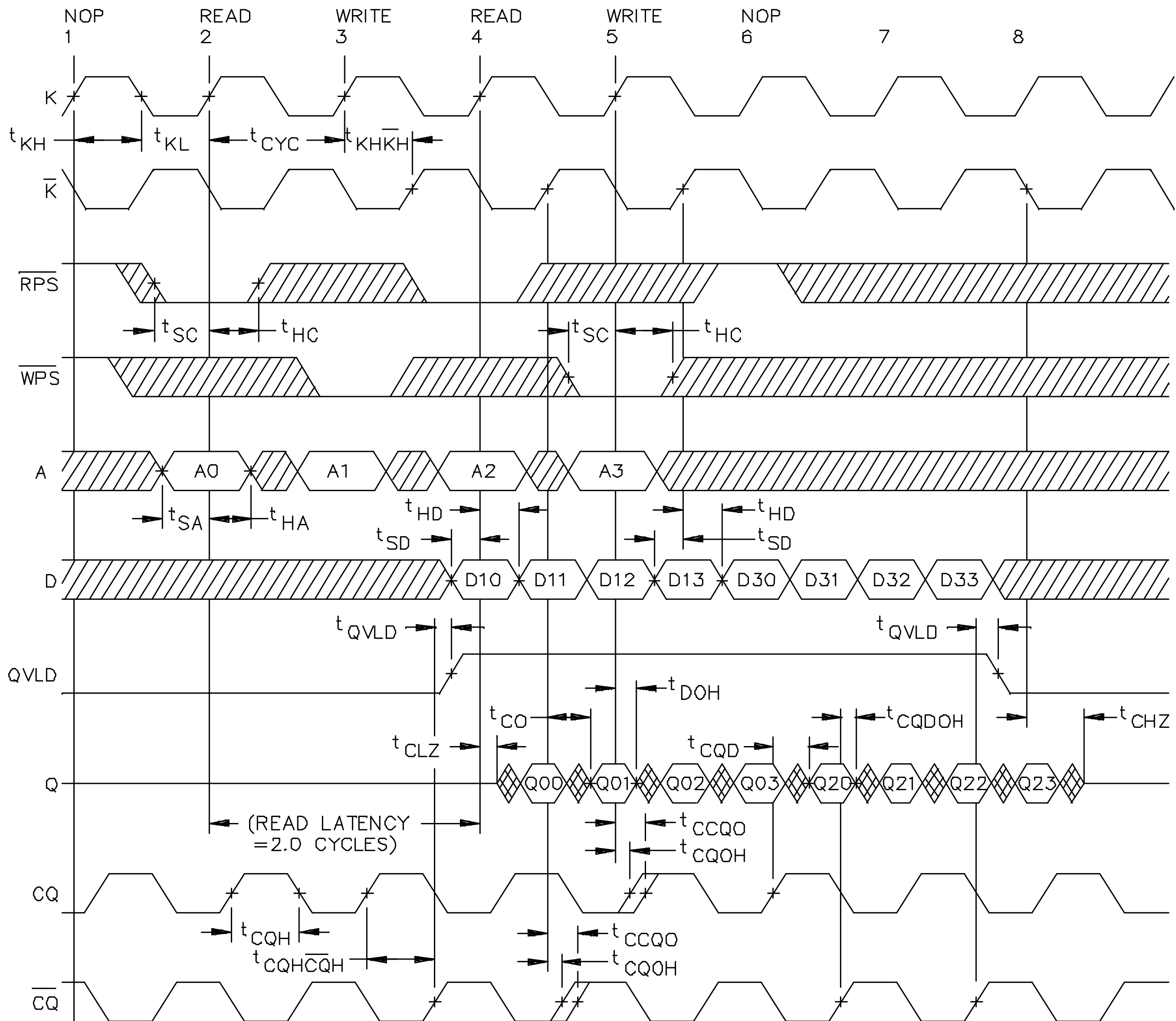
READ/WRITE/DESELECT SEQUENCE for device 01 1/ 2/ 3/



1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
2. Outputs are disabled (High Z) one clock cycle after a NOP.
3. In this example, if the address A0 = A1, then data Q00 = D10 and Q01 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

FIGURE 6. Timing waveforms - continued.

READ/WRITE/DESELECT SEQUENCE for device type 02 1/ 2/ 3/



1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
2. Outputs are disabled (High Z) one clock cycle after a NOP.
3. In this example, if the address A2 = A1, then data Q20 = D10 and Q21 = D11, Q22 = D12, and Q23 = D13. Write data is forwarded immediately as read results. This note applies to the whole diagram.

FIGURE 6. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

b. Interim and final electrical test parameters shall be as specified in Table IIA herein.

c. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

    (1) For class Q devices, the burn-in test operating frequency shall be greater than or equal to 0.5 MHz. For class V devices, the burn-in and Group C life test operating frequency shall be greater than or equal to 5.0 MHz.

d. Extra screening in addition to standard screening for device class Q:

    (1) Wafer Lot Acceptance Test for all lots - (Method 5007).
    (2) 100% internal visual, method 2010 condition A of MIL-STD-883.
    (3) 100% Non-destructive Bond Pull Alternative Method - (Method 2023).
    (4) 100% PIND - (Method 2020. Test Condition A).
    (5) Serialization.
    (6) Dynamic Burn-in Test - (Method 1015. 240 Hours at 125°C).
    (7) 3% defective allowable calculation (PDA) – (Functional Parameters at 25°C).
    (8) Radiography (X-Ray) - (Method 2012. Two views).

e. Additional screening performed for device class V:

    (1) Fine Leak and Gross Leak tests after Column attach.
    (2) 100% Electrical tests at 25°C after Column attach.
    (3) 100% External Visuals after Column attach – (Method 2009).

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in Table IIA herein.

b. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer’s TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.3.1 Subgroup 5 Salt Atmosphere testing. Testing is conducted on 12 devices with no failures before solder column attach and 3 devices with no failures after solder column attach.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in Table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in Table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C $\pm$5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq$ angle $\leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects are allowed.
b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.
c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
d. The particle range shall be $\geq$ 20 microns in silicon.
e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature $\pm$10ºC for single event upset testing.
f. Bias conditions shall be defined by the manufacturer for latchup measurements.
g. Test four devices with zero failures.

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1*,2,3,7*,8A, 8B,9,10,11 1/	1*,2,3,7*,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1*, 7*, 9 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1*, 7*, 9 Δ 1/ 2/	1*, 7*, 9 Δ 1/ 2/
6	Final electrical parameters	1*,2,3,7*,8A,8B,9, 10,11 1/	1*,2,3,7*,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4**,7,8A,8B,9, 10,11 4/	1,2,3,4**,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/ 6/	1,7,9	1,7,9
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach	1,7,9	1,7,9

1/ * Indicates PDA applies to subgroup 1 and 7.

2/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta limits shall be computed with reference to previous interim electrical parameters (see Line number 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.

3/ LGA packages only

4/ ** See 4.4.1d for subgroup 4.

5/ LGA package for all tests, plus CGA device for Column Pull and Salt Atmosphere.

6/ Subgroup 5 salt atmosphere testing is conducted on 12 devices with no failures before solder column attach and 3 devices with no failures after solder column attach.

Table IIB. Burn-in and operating life test delta limits at +25ºC.

Parameter 1/	Limit	Unit
I_{DD}, I_{SB1}	± 10% of the last measured value	mA
I_X, I_{OZ}	± 2 µA	µA
V_{OH2}, V_{OL2}	± 10% of the last measured value	mV

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 CGA packages lead finish. Microcircuits devices using column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark “A”. Terminal lead finish A for devices listed on this drawing are a tin (Sn) and lead (Pb) alloy. The solder column material contains compositions of Sn= 20% and Pb=80%.

6.8 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

APPENDIX A

Appendix A forms a part of SMD 5962-11201

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-10-01

Approved sources of supply for SMD 5962-11201 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN 3/
5962F1120101QXA	4/	CYRS1542AV18-250GCMB
5962F1120102QXA	4/	CYRS1543AV18-250GCMB
5962F1120101VXA	65786	CYRS1542AV18-250GCMB
5962F1120102VXA	65786	CYRS1543AV18-250GCMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ See 1.2.4 for description of the actual case outline lead finish.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 198 Champion Court San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.