REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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SHEET	15																			

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
13-03-26

REVISION LEVEL

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

MICROCIRCUIT, CMOS, OPERATIONAL AMPLIFIER, QUAD, MONOLITHIC SILICON

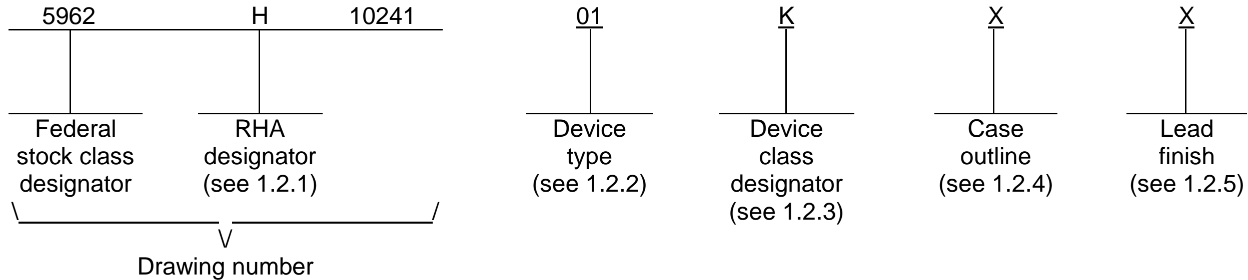
SIZE	CAGE CODE	
A	**67268**	**5962-10241**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHD5900	Quad operational amplifier
02	RHD5901	Quad operational amplifier, Hi-Z output control
03	RHD5902	Quad operational amplifier, High speed, Hi-Z output control

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	16	Flat package with formed leads

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+7.0 V dc
Input voltage (V_{IN}) range	V_{CC} +0.4 V, V_{EE} -0.4 V
Junction temperature (T_J)	+150°C
Power @ +25°C	200 mW
Thermal resistance, Junction to Case (Θ_{JC})	7° C/W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) range	+3.0 V dc to +5.5 V dc
Input Common Mode (V_{CM}) range	V_{CC} to V_{EE}
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features. 2/

Maximum Total Ionizing Dose (TID) ..(dose rate = 50 - 300 rad(Si)/s):	
In accordance with MIL-STD-883, method 1019, condition A	1 Mrad(Si)
Enhanced Low Dose Rate Sensitvity (ELDRS)	3/
Single Event Phenomenon (SEP) effective linear energy transfer (LET):	
No Single Event Latchup (SEL)	≤ 100 MeV-cm^2/mg 4/ 5/
Single Event Transient (SET)	≤ 59 MeV-cm2/mg 4/ 5/
Neutron Displacement Damage (> 1 x 10^{14} neutrons/cm^2)	3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ See section 4.3.5 for the manufacturer's radiation hardness assurance analysis and testing.
3/ Not tested, Immune by 100 percent CMOS technology.
4/ Single event testing performed at 100 Mev-cm^2/mg with no latch-up and up to 59 Mev-cm^2/mg with single event transients (voltage) limited as specified in Table IB.
5/ See table IB.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from the American Society for Testing and Materials, P O Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and and as specified on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.4 Switching diagram(s). The switching diagram(s) shall be as specified on figure 4.

3.2.5 Radiation exposure circuits. The radiation exposure circuits shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table IA and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = +5.0$ V, V_{EE} = GND unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input offset voltage 1/	V_{OS}		1,2,3	01,02	-3	3	mV
				03	-4	4	
Input offset current 1/	I_{OS}		1,2,3	All	-100	100	pA
Input bias current 1/	I_B		1,3	All	-100	100	pA
			2		-1	1	nA
Common Mode Rejection Ratio	CMRR		4,5,6	01,02	70		dB
				03	60		
Power supply rejection ratio	PSRR		4,5,6	All	70		dB
Output voltage high	V_{OH}	R_{OUT} = 3.6 kΩ to GND	1,2,3	All	4.90		V
Output voltage low	V_{OL}	R_{OUT} = 3.6 kΩ to V_{CC}	1,2,3	All		0.1	V
Short circuit output current 2/	$I_{O(SINK)}$	V_{OUT} to V_{CC}	1,2,3	01,02	-30	-75	mA
				03	-130	-290	
	$I_{O(SOURCE)}$	V_{OUT} to V_{EE}		01,02	45	55	
				03	110	210	
Slew rate 1/	SR	R_L = 8 kΩ, Gain = +1	9,10,11	01,02	2.0		V/µs
				03	12.0		
Open loop gain 1/	A_{OL}	R_L = 100 kΩ	4,5,6	All	90		dB
Unity gain bandwidth 1/	UGBW	R_L = 10 kΩ	4,5,6	01,02	4		MHz
				03	23		
Quiescent supply current 1/	I_{CCQ}	All amplifiers enabled, no loads	1,2,3	All		5.5	mA
		All amplifiers disabled		02,03		300	nA
Channel separation 2/	CH_{SEP}	R_L = 2 kΩ, f = 1.0 kHz	4,5,6	All	84		dB
Enable input voltage high 2/	V_{HI}	HI = enabled	1,2,3	02,03	3.5		V
Enable input voltage low 2/	V_{LO}	LO = disabled	1,2,3	02,03		1.5	V
Enable input current 2/	I_{EN}		1,2,3	02,03		10	nA
Output enable delay 2/	$t_{ON}EN$	See figure 4	9,10,11	02,03		500	ns
Output disable delay 2/	$t_{OFF}EN$		9,10,11	02,03		100	ns

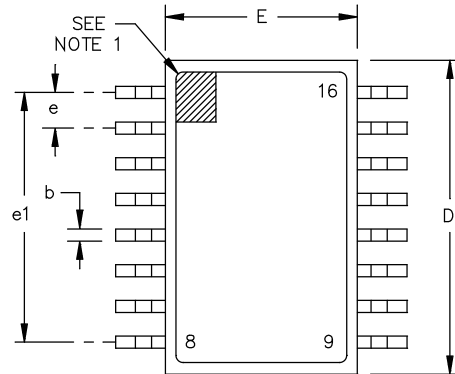
1/ These devices have been tested to (2 Mrad(Si)) to Method 1019, condition A of MIL-STD-883 at +25°C for these parameters to assure the requirements of RHA designator level "H" (1Mrad(Si)) are met.
2/ Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.

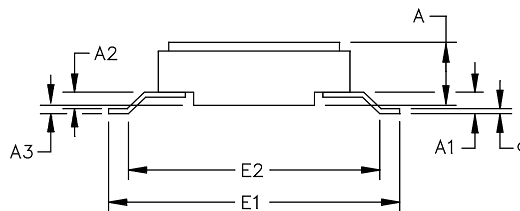
TABLE IB. SEP test limits. 1/

Device types	SEP	Temperature (T_C)	Conditions	Results	Effective linear energy transfer (LET)
01,02,03	SEL	+125°C	V_{CC} = +5.5 V and V_{EE} = +0 V	No SEL	< 100 MeV-cm^2/mg
			V_{CC} = +2.75 V and V_{EE} = -2.75 V	No SEL	
01,02,03	SET (transient voltage)	+25°C	V_{CC} = +5.0 V and V_{EE} = +0 V	Maximum voltage 240 mV Maximum duration 3.5 µS	< 59 MeV-cm^2/mg
			V_{CC} = +2.5 V and V_{EE} = -2.5 V	Maximum voltage 240 mV Maximum duration 4.0 µS	

1/ For SEP test conditions, see 4.3.5.1.2.2 herein.

Case X





Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.105		2.68
A1	.030 REF		0.76 REF	
A2	.017	.027	0.43	0.69
A3		.012		0.30
b	.015	.019	0.38	0.48
c	.007	.009	0.18	0.23
D		.417		10.59
e	.050 BSC		1.27 BSC	
e1	.350 BSC		8.90 BSC	
E		.300		7.62
E1	.394	.419	10.01	10.64
E2	.346 REF		8.79 REF	

NOTE:
1. Location of the pin 1 marking. The ESD symbol may be used as the pin 1 marking.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. Package and lid are electrically isolated from signal pads.

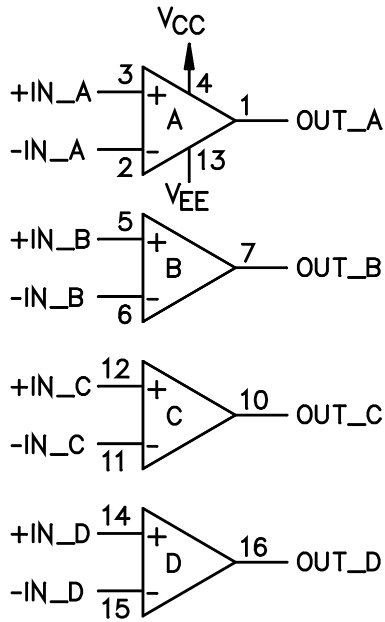
FIGURE 1. Case outline.

Device types	01	02 and 03
Case outline	X	
Terminal number	Terminal symbol	
1	OUT_A	OUT_A
2	-IN_A	-IN_A
3	+IN_A	+IN_A
4	V_{CC}	V_{CC}
5	+IN_B	+IN_B
6	-IN_B	-IN_B
7	OUT_B	OUT_B
8	NC_GND (See note 1)	EN_AB (See note 2)
9	NC_GND (See note 1)	EN_CD (See note 2)
10	OUT_C	OUT_C
11	-IN_C	-IN_C
12	+IN_C	+IN_C
13	V_{EE}	V_{EE}
14	+IN_D	+IN_D
15	-IN_D	-IN_D
16	OUT_D	OUT_D

NOTE:
1. NC_GND (pins 8 and 9) should be grounded to eliminate or minimize electrostatic discharge (ESD) or static buildup.
2. EN_AB enables amplifiers A and B, EN_CD enables amplifiers C and D.

FIGURE 2. Terminal connections.

DEVICE TYPE 01



DEVICE TYPES 02 AND 03

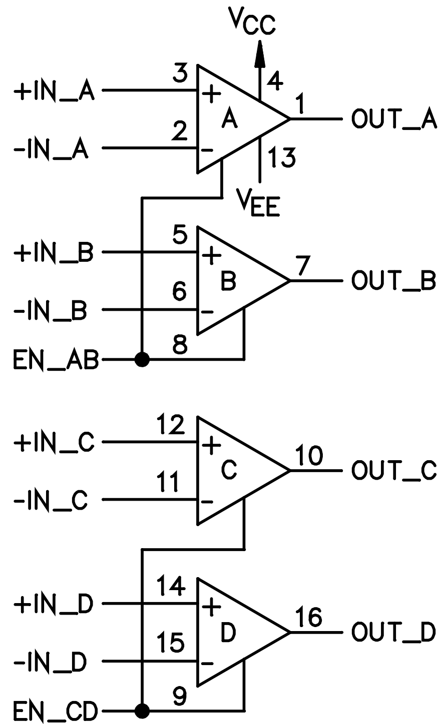


FIGURE 3. Logic diagram(s).

DEVICE TYPES 02 AND 03

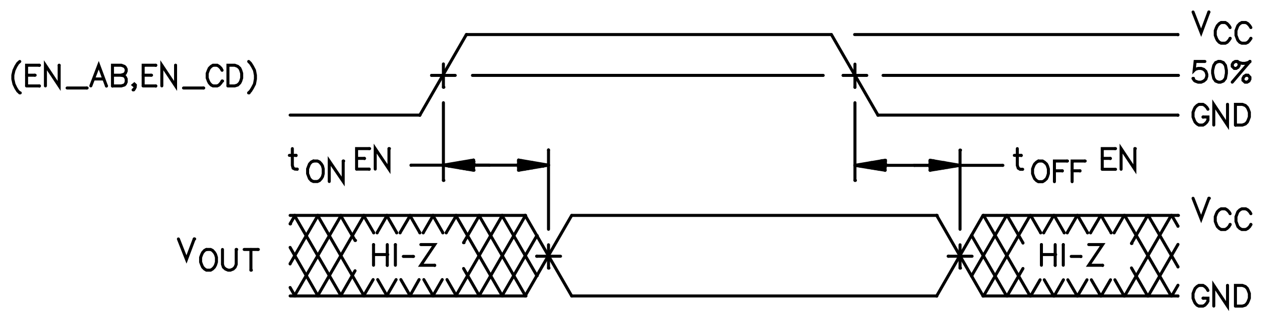


FIGURE 4. Switching diagrams.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,9
Final electrical parameters	1*2,3,4,5,6,9,10,11
Group A test requirements	1,2,3,4,5,6,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,9,10,11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	1,4,9

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8A , and 8B shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5. Radiation hardness assurance (RHA). RHA qualification is required only for those devices with the RHA designator as specified herein. See table IIIA and table IIIB.

Table IIIA. Radiation Hardness Assurance Method Table.

RHA method employed	**Testing at 2X rated total dose of (1 Mrad)**		**Worst Case Analysis Performed No**				**End point electricals after total dose**	
	Element Level	Hybrid Device Level	Includes temperature effects	Combines temperature and radiation effects	Combines total dose and displacement effects	End-of-life	Element Level T_C = +25°C	Hybrid device level T_C = +25°C
	Yes	Yes (See 4.3.5.1.1)	N/A	N/A	N/A	N/A	Yes	Yes

NOTES:
X = Radiation testing done (Level)
G = Guaranteed by design or process
(N) = Not yet tested
N/A = Not applicable for this SMD

Table IIIB. Hybrid level and element level test table.

	Radiation Test								
	Total Dose			**Heavy Ion**		**Proton**		**Neutron**	
	Low Dose Rate (LDR)	High Dose Rate (HDR)	ELDRS	SET (transient)	SEL (latch-up)	Low Energy	High Energy	SEE (upset)	Displacement Damage (DD)
CMOS IC	G	X (2 Mrad) (See 4.3.5.1.1)	G	X 59 MeV-cm^2/mg	X 100 MeV-cm^2/mg	(N)	(N)	(N)	G

NOTES:
X = Radiation testing done (Level)
G = Guaranteed by design or process
(N) = Not yet tested
N/A = Not applicable for this SMD

4.3.5.1 Radiation Hardness Assurance (RHA) inspection. RHA qualification is required for those devices with the RHA designator as specified herein. End-point electrical parameters for radiation hardness assurance (RHA) devices shall be specified in table II. Radiation testing will be in accordance with the qualifying activity (DLA Land and Maritime -VQ) approved plan and with MIL-PRF-38534, Appendix G.

a. The hybrid device manufacturer shall establish procedures controlling component radiation testing, and shall establish radiation test plans used to implement component lot qualification during procurement. Test plans and test reports shall be filed and controlled in accordance with the manufacturer's configuration management system.

b. The hybrid device manufacturer shall designate a RHA program manager to oversee component lot qualification, and to monitor design changes for continued compliance to RHA requirements.

4.3.5.1.1 Hybrid level RHA qualification. Hybrid level and element level testing are the same for the devices on this Standard Microcircuit Drawing (SMD) since the active element is accessible to the device leads for test.

4.3.5.1.1.1 Qualification by similarity. The devices on this (SMD) are considered similar for the purpose of RHA testing. Device type 5962H1024102KXC was RHA tested, therefore the other device types on this SMD are qualified by similarity.

4.3.5.1.2 Element level qualification.

4.3.5.1.2.1 Total ionizing dose irradiation testing. A minimum of 5 biased devices of the active element used will be tested every wafer lot. These active element will be tested at HDR in accordance with condition A of method 1019 of MIL-STD-883 to 2 Mrad(Si) to assure 1 Mrad(Si) for the device parameters as specified in table IA herein.

4.3.5.1.2.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.3.5.1.2.2 Single Event Phenomena (SEP). A minimum of one representative hybrid from this SMD shall be characterized for SEL and SET responses at initial qualification and after any design or process change which may affect the RHA response of the devices on this SMD. Testing shall be performed in accordance with ASTM F1192. Test conditions are as follows:

a. The ion beam angles of incidence for SEL shall be normal and 55 degrees to the die surface and for SET shall be normal. No shadowing of the ion beam due to fixturing is allowed.

b. The fluence shall be ≥ 1×10^7 particles/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 60 micron in silicon.

e. The transient test temperature shall be +25° ±10°C and the latchup test temperature shall be +125°C ±10°C.

f. For SEP test limits, see table IB herein.

4.3.5.2 RHA Lot Acceptance. Each wafer lot of the active element shall be evaluated for acceptance in accordance with MIL-PRF-38534 and herein.

4.3.5.2.1 Total Ionizing Dose (TID). See paragraph 4.3.5.1.2.1 and 4.3.5.1.2.1.1 herein.

4.3.5.2.2 Enhanced Element Evaluation. Enhanced Element Evaluation per Table IV herein including 45 devices subjected to Group C2, 1000 hours life testing, is required only for those devices with the RHA designator as specified herein.

Table IV. Enhanced Element Evaluation For Microcircuit Die.

Subgroup	Class K	Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity (accept number)	Reference Paragraph 1/
2	X	Element visual	2010		100 percent	C.3.3.2
		Assembled into package as specified in 1.2.4 herein.			100 percent	
1	X	Element electrical			100 percent	C.3.3.1
3	X	Internal visual	2017		100 percent	C.5.5
4	X	Temperature cycling	1010	C	100 percent	C.3.3.3
	X	Constant acceleration	2001	3000g's, Y1 direction		C.5.6
	X	Burn-in	1015	160 hours minimum at +125°C		
	X	Interim electrical				C.3.3.4.3
	X	Burn-in	1015	160 hours minimum at +125°C		
	X	Post burn-in Final Electrical, Group A				C.5.10
	X	Steady-state life	1005	1000 hours minimum at +125°C	45(0) 2/	
	X	Final electrical				C.3.3.4.3
5	X	Wire bond evaluation 3/	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018		See method 2018 of MIL-STD-883	C.3.3.6

1/ See MIL-PRF-38534.
2/ Die shall be traceable to the wafer and wafer lot. The sample size shall consist of a minimum of 3 die from each wafer and a minimum of 45 die from each wafer lot.
3/ The devices herein is manufactured with aluminum wires and aluminum bond sites on the IC. No bimetallic bonds.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of transients (SEP).

d. Occurance of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-03-26

Approved sources of supply for SMD 5962-10241 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1024101KXA	88379	RHD5900-201-2S
5962H1024101KXA	88379	RHD5900-901-2S
5962-1024101KXC	88379	RHD5900-201-1S
5962H1024101KXC	88379	RHD5900-901-1S
5962-1024102KXA	88379	RHD5901-201-2S
5962H1024102KXA	88379	RHD5901-901-2S
5962-1024102KXC	88379	RHD5901-201-1S
5962H1024102KXC	88379	RHD5901-901-1S
5962-1024103KXA	88379	RHD5902-201-2S
5962H1024103KXA	88379	RHD5902-901-2S
5962-1024103KXC	88379	RHD5902-201-1S
5962H1024103KXC	88379	RHD5902-901-1S

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
88379	Aeroflex Plainview Incorporated, (Aeroflex Microelectronic Solutions) 35 South Service Road Plainview, NY 11803-4193

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.