REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add radiation hardness assurance requirements. - ro	13-11-15	C. SAFFLE
B	Add footnote 1/ to paragraph 1.2.2. Add appendix A with update to paragraphs A.3.4 and A 4.2. -rrp	15-12-16	C. SAFFLE
C	Add device type 02. Add $T_A = T_J$ footnote 5/ to Table I.- ro	18-04-18	C. SAFFLE
D	Add RHA device type 02 and add die figure A-2 under Appendix A. - ro	18-06-20	C. SAFFLE
E	Make correction to the bond pad coordinates in figure A-2. -rrp	18-10-04	C. SAFFLE
F	Make change to the SYNC out high level threshold minimum test limit as specified under Table I. Delete the condition of the SYNC in frequency range test as specified under Table I. Make changes to EN, RT, SYNC, V_{IN}, P_{VIN}, and PH terminal symbol descriptions as specified under Figure 1. - ro	21-04-27	J. ESCHMEYER

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
13-06-14

REVISION LEVEL
F

MICROCIRCUIT, LINEAR, SYNCHRONOUS STEP DOWN CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-10221**

SHEET 1 OF 24

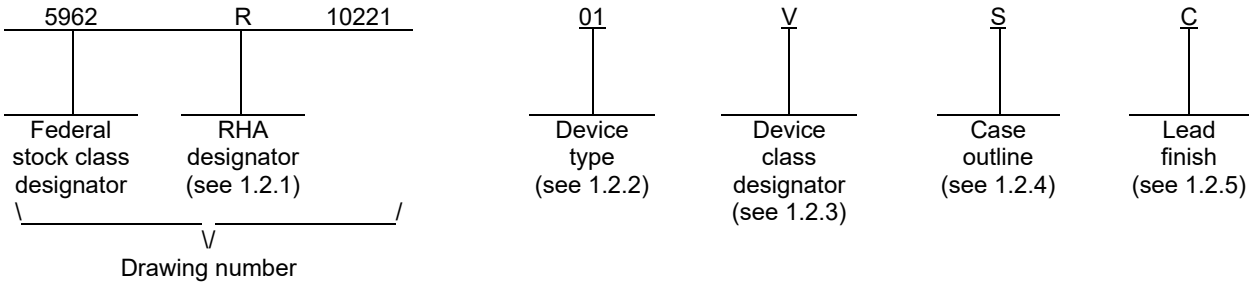
DSCC FORM 2233
APR 97

5962-E315-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	TPS50601-SP	6.3 V, 6 A synchronous step down converter
02	TPS50601A-SP	7.0 V, 6 A synchronous step down converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
S	CDFP3-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I. During package characterization of device type 01 die, manufacturer shall perform full temperature range test. However, wafer die probe test is performed at +25°C and +125°C for bare die.

1.3 Absolute maximum ratings. 2/

Input voltage (V_{IN}) :	
Input voltage (V_{IN}) :	
Device type 01	-0.3 V to 7 V
Device type 02	-0.3 V to 7.5 V
Power input voltage (P_{VIN}) :	
Device type 01	-0.3 V to 7 V
Device type 02	-0.3 V to 7.5 V
Enable (EN)	-0.3 V to 5.5 V
Bootstrap cap (BOOT) (device type 01 only)	-0.3 V to 14 V
Sense voltage (V_{SENSE})	-0.3 V to 3.3 V
Compensation (COMP)	-0.3 V to 3.3 V
Power good fault (PWRGD)	-0.3 V to 5.5 V
Slow start and tracking (SS/TR)	-0.3 V to 5.5 V
Resistor pin (RT) (device type 02 only)	-0.3 V to 5.5 V
Synchronization (SYNC) :	
Device type 01	-0.3 V to 7 V
Device type 02	-0.3 V to 7.5 V
Output voltage (V_{OUT}) :	
BOOT-PH (device type 01 only)	0 V to 7 V
REFCAP (device type 02 only)	-0.3 V to 3.3 V
Switch node (PH) :	
Device type 01	-1 V to 7 V
Device type 02	-1 V to 7.5 V
PH 10 ns transient :	
Device type 01	-3 V to 7 V
Device type 02	-3 V to 7.5 V
Output current (device type 01 only)	6 A
Differential voltage (V_{diff}), GND to exposed thermal pad	-0.2 V to 0.2 V
Source current:	
Device type 01:	
High side switch current limit (between V_{IN} and PH)	7.8 A
Low side switch current limit (between GND and PH)	6 A
Device type 02:	
PH	Current limit in amps
RT	$\pm$100 μA
Sink current:	
COMP	$\pm$200 μA
PWRGD	-0.1 mA to 5 mA
Device type 02:	
PH	Current limits in amps
PVIN	Current limits in amps

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

1.3 Absolute maximum ratings - continued. 2/

Electrostatic discharge (ESD):	
Human body model (HBM) :	
Device type 01	1 kV
Device type 02	750 V
Charged device model (CDM)	1 kV
Operating junction temperature (T_J)	-55°C to +150°C
Storage temperature	-65°C to +150°C
Thermal resistance, junction to case (θ_{JC}) with thermal pad	0.52°C/W 3/ 4/ 5/

1.4 Recommended operating conditions.

Input voltage (V_{IN})	3 V to 6.3 V
Power input voltage (P_{VIN}) :	
Device type 01	1.6 V to 6.3 V
Device type 02	3.0 V to 7.0 V
Operating temperature ($T_A = T_J$)	-55°C to +125°C

1.5 Radiation features.

For device type 01:	
Maximum total ionizing dose available (effective dose rate = 0.1 rad(Si)/s)	100 krad(Si) 6/
For device type 02:	
Maximum total ionizing dose available (high dose rate = 50 - 300 rad(Si)/s)	100 krad(Si) 7/
Maximum total ionizing dose available (low dose rate ≤ 10 mrad(Si)/s)	100 krad(Si) 7/

The manufacturer supplying RHA device type 02 on this drawing has performed characterization test to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1 at a dose level of 100 krad(Si).

_____

3/ Maximum power dissipation may be limited by overcurrent protection.

4/ Power rating at a specific ambient temperature (T_A) should be determined with a junction temperature (T_J) of 150°C. This is the point where distortion starts to substantially increases. Thermal management of the printed circuit board (PCB) should strive to keep the junction temperature at or below 150°C for best performance and long term reliability.

5/ Test board conditions:
a. 2.5 inches x 2.5 inches, four layers, thickness: 0.062 inch.
b. Two ounces copper traces located on the top of the PCB.
c. Two ounces copper ground planes on the two internal layers and bottom layer.
d. Four 0.010 inch thermal vias located under the device package.

6/ Device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate for device type 01 after extended room temperature anneal = 0.1 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower environment.

7/ The manufacturer supplying device type 02 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply voltage (V_{IN} and P_{VIN} pins).							
P_{VIN} operating input voltage			1,2,3	01	1.6	6.3	V
				02	3.0	7.0	
V_{IN} operating input voltage			1,2,3	01	3	6.3	V
				02	3	7.0	
V_{IN} internal under voltage lockout (UVLO) threshold		V_{IN} rising	1,2,3	01, 02		3	V
V_{IN} shutdown supply current		EN = 0 V	1,2,3	01		5.9	mA
				02		2.5	
V_{IN} operating – non switching supply current		V_{SENSE} = voltage bandgap (VBG) = 0.795 V	1,2,3	01, 02		10	mA
Enable and UVLO (EN pin).							
Enable threshold voltage		Rising	1,2,3	01, 02		1.18	V
Enable threshold voltage		Falling	1,2,3	01, 02	1.05		V
Voltage reference.							
Voltage reference		$0 A \le I_{OUT} \le 6 A$	1	01	0.785	0.804	V
			2		0.785	0.815	
			3		0.767	0.804	
			1,2,3	02	0.792	0.816	
Error amplifier							
Error amplifier 6/ transconductance	gm	$-2 \mu A < I_{COMP} < 2 \mu A$, $V_{(COMP)} = 1 V$	9,10,11	02	1000	2000	µS
Error amplifier source/sink 6/		$V_{(COMP)} = 1 V$, 100 mV input overdrive	1,2,3	02	-250	250	µA
Current limit.							
High side switch current limit threshold 7/		$V_{IN} = 6.3 V$	1,2,3	01	8		A
Low side switch sourcing current limit 7/		$V_{IN} = 6.3 V$	1,2,3	01	7		A

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal switching frequency.							
Internal set frequency		RT = open	4,5,6	01, 02	395	585	kHz
External set frequency.		RT = 100 kΩ (1%)	4,5,6	02	395	585	kHz
		RT = 487 kΩ (1%)			85	120	
		RT = 47 kΩ (1%)			900	1100	
External synchronization.							
SYNC out low-to-high rise time (10%/90%)		C_L = 25 pF	9,10,11	01, 02		111	ns
SYNC out high-to-low fall time (90%/10%)		C_L = 25 pF	9,10,11	01		15	ns
				02		15.5	
SYNC out high level threshold		I_{OH} = 50 μA	1,2,3	01	2		V
				02	V_{IN} – 0.3		
SYNC out low level threshold		I_{OL} = 50 μA	1,2,3	01, 02		600	mV
SYNC in low level threshold			1,2,3	01	800		mV
		PVIN = VIN =3.0 V		02		900	
		PVIN = VIN = 7.0 V				900	
SYNC in high level threshold			1,2,3	01		1.85	V
		PVIN = VIN =3.0 V		02	2.45		
		PVIN = VIN = 7.0 V			4.25		
SYNC in frequency range 8/			4,5,6	01	-5	5	%
					100	1000	kHz
PH (PH pin).							
Minimum on time		Measured at 90% to 90% of V_{IN}, I_{PH} = 2 A	9	01		175	ns
				02		235	
BOOT (BOOT pin).							
BOOT and PH pins UVLO			1,2,3	01		3	V
Slow start and tracking (SS/TR pin).							
SS charge current			1,2,3	02	1.5	3	μA
SS/TR to V_{SENSE} matching		$V_{(SS/TR)}$ = 0.4 V	1,2,3	01, 02		90	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power good (PWRGD pin).							
Output high leakage		V_{SENSE} = Vref, $V_{(PWRGD)}$ = 5 V	1,2,3	01, 02		181	nA
Output low voltage		$I_{(PWRGD)}$ = 2 mA	1,2,3	01, 02		0.3	V
Minimum V_{IN} for valid output		$V_{(PWRGD)} < 0.5$ V at 100 μA	1,2,3	01, 02		1	V
Minimum SS/TR voltage for PWRGD			1,2,3	01		1.4	V
				02		1.55	

1/ Unless otherwise specified, V_{IN} = 3 V to 6.3 V, for device type 01, P_{VIN} = 1.6 V to 6.3 V, and for device type 02, P_{VIN} = 3 V to 7.0 V.

2/ Device types 01 and 02 supplied to this drawing has been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

3/ Device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate for device type 01 after extended room temperature anneal = 0.1 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower environment.

4/ The manufacturer supplying device type 02 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).

5/ For production testing of these parameters to the limits in Table I herein, Ambient temperature (T_A) = Junction temperature (T_J).

6/ Ensured by design only. Not tested in production.

7/ For wafer probe only, specification is guaranteed by characterization and is not tested in production.

8/ For wafer probe only, specification is guaranteed by characterization and production tested at nominal voltage with $V_{IN} = P_{VIN} = 5$ V.

Device types	01	02
Case outline	S	
Terminal number	Terminal symbol	
1	GND	GND
2	EN	EN
3	RT	RT
4	SYNC	SYNC
5	V_{IN}	V_{IN}
6	P_{VIN}	P_{VIN}
7	P_{VIN}	P_{VIN}
8	PGND	PGND
9	PGND	PGND
10	PGND	PGND
11	PH	PH
12	PH	PH
13	PH	PH
14	PH	PH
15	PH	PH
16	BOOT	REFCAP
17	V_{SENSE}	V_{SENSE}
18	COMP	COMP
19	SS/TR	SS/TR
20	PWRGD	PWRGD

FIGURE 1. Terminal connections.

Terminal symbol	Description
GND	Return for control circuitry/thermal pad. See note 1.
EN	Enable pin. This pin is internally pulled up allowing for the pin to be floated to enable the device. Adjust the input undervoltage lockout with two resistors.
RT	In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency. Leaving this pin floating sets the internal switching frequency to 500 kHz.
SYNC	Optional 100 kHz to 1 MHz external system clock input.
V_{IN}	Input power for the control circuitry of the switching regulator.
P_{VIN}	Power input. Input power for the output stage of the switching regulator.
PGND	Return for low side power MOSFET.
PH	Switch phase node.
BOOT	A boot strap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high side MOSFET.
REFCAP	Required 470 nF external capacitor for internal reference.
V_{SENSE}	Inverting input of the transconductance (gm) error amplifier.
COMP	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	Slow start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
PWRGD	Power good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over voltage, EN shutdown or during slow start.

Note:
1. Thermal pad (analog ground) must be connected to PGND external to the package.

FIGURE 1. Terminal connections - continued.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5,6, 1/ 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6 2/
Group D end-point electrical parameters (see 4.4)	1,4	1,4
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and life test delta parameters. (T_A = +25°C). 1/

Parameters	Device types	Min	Max	Units
V_{IN} shutdown supply current	01, 02	-0.59	+0.59	mA
V_{IN} operating - non switching supply current	01, 02	-1.0	+1.0	mA

1/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and condition D as specified herein (see 1.5).

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

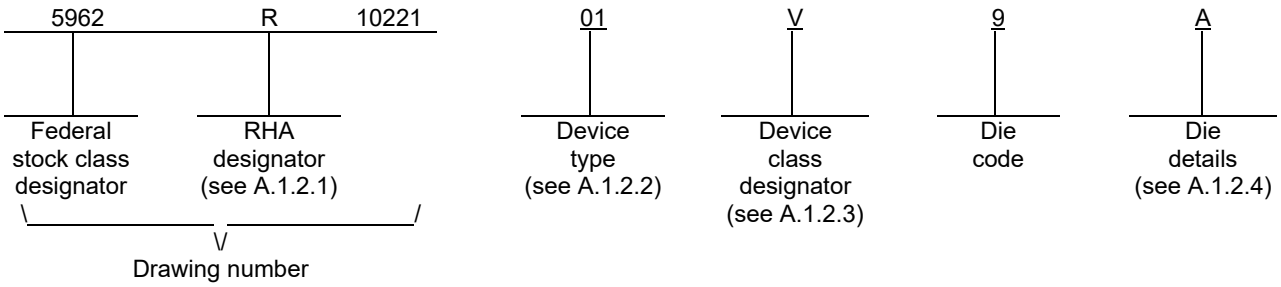
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-10221

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS50601-RHA KGD	6.3 V, 6 A synchronous step down converter
02	TPS50601A-SP	7.0 V, 6 A synchronous step down converter

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and A-2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1 and A-2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and A-2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figures A-1 and A-2.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.1.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

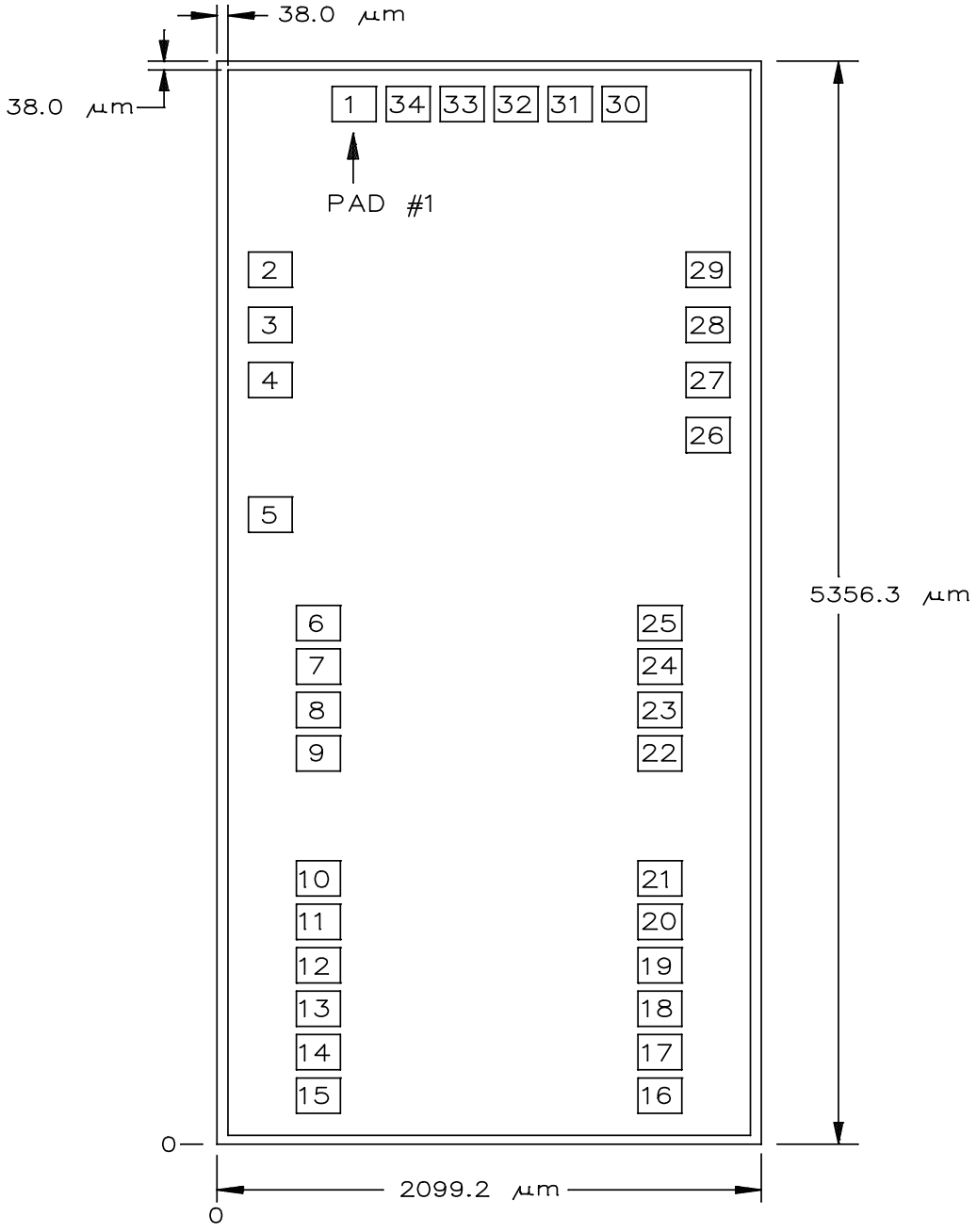


FIGURE A-1. Die bonding pad locations and electrical functions.

Description	Pad number	X min (μm)	Y min (μm)	X max (μm)	Y max (μm)
GND	1	400.77	5039.325	578.07	5216.625
EN	2	44.19	4169.79	221.49	4347.09
RT	3	44.19	3894.21	221.49	4071.51
SYNC	4	44.19	3618.63	221.49	3795.93
VIN	5	47.565	2952.27	224.865	3129.57
PVIN	6	280.215	2414.115	457.515	2591.415
PVIN	7	280.215	2170.665	457.515	2347.965
PVIN	8	280.215	1928.115	457.515	2105.415
PVIN	9	280.215	1684.665	457.515	1861.965
PGND	10	254.52	1236.285	431.82	1413.585
PGND	11	254.52	1008.315	431.82	1185.615
PGND	12	254.52	780.345	431.82	957.645
PGND	13	254.52	552.375	431.82	729.675
PGND	14	254.52	324.405	431.82	501.705
PGND	15	254.52	96.435	431.82	273.735
PH	16	1590.12	99.405	1767.42	276.705
PH	17	1590.12	321.435	1767.42	498.735
PH	18	1590.12	555.345	1767.42	732.645
PH	19	1590.12	777.375	1767.42	954.675
PH	20	1590.12	1011.285	1767.42	1188.585
PH	21	1590.12	1233.315	1767.42	1410.615
PH	22	1564.335	1684.665	1741.635	1861.965
PH	23	1564.335	1928.115	1741.635	2105.415
PH	24	1564.335	2170.665	1741.635	2347.965
PH	25	1564.335	2414.115	1741.635	2591.415
BOOT	26	1801.71	3352.14	1979.01	3529.44
VSENSE	27	1801.71	3644.145	1979.01	3821.445
COMP	28	1801.71	3940.92	1979.01	4118.22
SS/TR	29	1801.71	4216.5	1979.01	4393.8
PWRGD	30	1463.67	5039.325	1640.97	5216.625
GND	31	1251.09	5039.325	1428.39	5216.625
GND	32	1038.51	5039.325	1215.81	5216.625
GND	33	825.93	5039.325	1003.23	5216.625
GND	34	613.35	5039.325	790.65	5216.6
Substrate is not to be connected					

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Die physical dimensions.
Die size: 2100.00 µm x 5358.00 µm
Die thickness: 15 ± 1 mils

Interface materials.
Top metallization: Al5TiN (557.5 nm)
Backside metallization: Bare back

Glassivation.
Type: Oxide
Thickness: 11 kA

Substrate: Silicon

Assembly related information.
Substrate potential: Ground
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

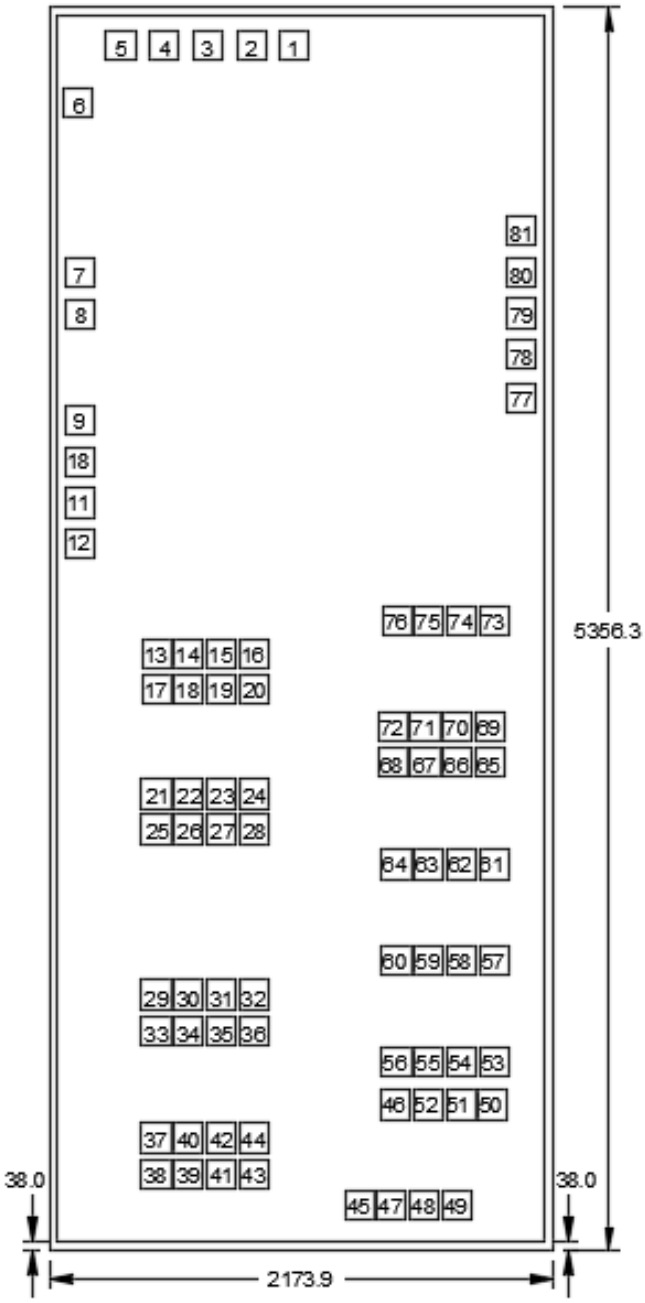


FIGURE A-2. Die bonding pad locations and electrical functions.

Description	Pad number	X min (μm)	Y min (μm)	X max (μm)	Y max (μm)
AVSS	1	938.16	5098.41	1064.16	5224.41
AVSS	2	759.06	5098.41	885.06	5224.41
NC	3	579.96	5098.41	705.96	5224.41
AVSS	4	400.86	5098.41	526.86	5224.41
AVSS	5	221.76	5098.41	347.76	5224.41
EN	6	38.7	4843.98	164.7	4969.98
RT	7	38.7	4115.43	164.7	4241.43
SYNC	8	38.7	3936.33	164.7	4062.33
VIN	9	55.89	3473.865	181.89	3599.865
VIN	10	55.89	3285.765	181.89	3411.765
VIN	11	55.89	3097.665	181.89	3223.665
VIN	12	55.89	2909.565	181.89	3035.565
PVIN	13	360.045	2468.025	486.045	2594.025
PVIN	14	500.805	2468.025	626.805	2594.025
PVIN	15	643.905	2468.025	769.905	2594.025
PVIN	16	782.505	2468.025	908.505	2594.025
PVIN	17	360.045	2312.595	486.045	2438.595
PVIN	18	500.805	2312.595	626.805	2438.595
PVIN	19	643.905	2312.595	769.905	2438.595
PVIN	20	782.505	2312.595	908.505	2438.595
PVIN	21	360.045	1868.265	486.045	1994.265
PVIN	22	500.805	1868.265	626.805	1994.265
PVIN	23	643.905	1868.265	769.905	1994.265
PVIN	24	782.505	1868.265	908.505	1994.265
PVIN	25	360.045	1712.265	486.045	1838.835
PVIN	26	500.805	1712.265	626.805	1838.835
PVIN	27	643.905	1712.265	769.905	1838.835
PVIN	28	782.505	1712.265	908.505	1838.835
PGND	29	360	1004.625	486	1130.625
PGND	30	498.6	1004.625	624.6	1130.625
PGND	31	637.2	1004.625	763.2	1130.625
PGND	32	775.8	1004.625	901.8	1130.625
PGND	33	360	863.955	486	989.955
PGND	34	498.6	863.955	624.6	989.955
PGND	35	637.2	863.955	763.2	989.955
PGND	36	775.8	863.955	901.8	989.955
PGND	37	360	384.525	486	510.525
PGND	38	360	243.855	486	369.855
PGND	39	503.1	243.855	629.1	369.855
PGND	40	503.1	384.525	629.1	510.525

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

Description	Pad number	X min (μm)	Y min (μm)	X max (μm)	Y max (μm)
PGND	41	641.7	243.855	767.7	369.855
PGND	42	641.7	384.525	767.7	510.525
PGND	43	775.8	243.855	901.8	369.855
PGND	44	775.8	384.525	901.8	510.525
PH	45	1239.66	97.425	1365.66	223.425
PH	46	1374.66	529.965	1500.66	655.965
PH	47	1378.26	97.425	1504.26	223.425
PH	48	1516.86	97.425	1642.86	223.425
PH	49	1657.26	97.425	1783.26	223.425
PH	50	1790.46	529.965	1916.46	655.965
PH	51	1651.86	529.965	1777.86	655.965
PH	52	1513.26	529.965	1639.26	655.965
PH	53	1790.46	718.515	1916.46	844.515
PH	54	1651.86	718.515	1777.86	844.515
PH	55	1513.26	718.515	1639.26	844.515
PH	56	1374.66	718.515	1500.66	844.515
PH	57	1790.46	1150.065	1916.46	1276.065
PH	58	1651.86	1150.065	1777.86	1276.065
PH	59	1513.26	1150.065	1639.26	1276.065
PH	60	1374.66	1150.065	1500.66	1276.065
PH	61	1795.365	1565.1	1921.365	1691.1
PH	62	1655.865	1565.1	1781.865	1691.1
PH	63	1515,465	1565.1	1641.465	1691.1
PH	64	1376.865	1565.1	1502.865	1691.1
PH	65	1795.365	2016	1921.365	2142
PH	66	1655.865	2016	1781.865	2142
PH	67	1515.465	2016	1641.465	2142
PH	68	1376.865	2016	1502.865	2142
PH	69	1795.365	2164.86	1921.365	2290.86
PH	70	1655.865	2164.86	1781.865	2290.86
PH	71	1515.465	2164.86	1641.465	2290.86
PH	72	1376.865	2164.86	1502.865	2290.86
PH	73	1795.365	2615.76	1921.365	2741.76
PH	74	1655.865	2615.76	1781.865	2741.76
PH	75	1515.465	2615.76	1641.465	2741.76
PH	76	1376.865	2615.76	1502.865	2741.76
REFCAP_NU	77	1933.245	3572.46	2059.245	3698.46
VSENSE	78	1933.245	3770.415	2059.245	3896.415
COMP	79	1933.245	3949.515	2059.245	4075.515
SS	80	1933.2	4149.135	2059.2	4275.135
PWRGD	81	1933.2	4292.325	2059.2	4418.325

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

Die physical dimensions.
Die size: 2174.00 µm x 5358.00 µm
Die thickness: 15 ± 1 mils

Interface materials.
Top metallization: ALCU (1050 nm)
Backside metallization: Bare back

Glassivation.
Type: OXYNITRIDE
Thickness: 11 kA

Substrate: Silicon

Assembly related information.
Substrate potential: Ground
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-04-27

Approved sources of supply for SMD 5962-10221 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1022101VSC	01295	TPS50601-SP
5962R1022101VSC	01295	TPS50601-RHA
5962R1022101V9A	01295	TPS50601-RHA KGD
5962-1022102VSC	01295	TPS50601A-SP
5962R1022102VSC	01295	TPS50601A-RHA
5962R1022102V9A	01295	TPS50601A-RHA-KGD

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243