| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Boilerplate update. Corrections to sections 1.3, 1.5 and Table IB. Corrections to Figure 2 terminal connections table. Removed class M references to meet current boilerplate requirements. – glg | 13-04-03 | Charles F. Saffle |
| B | Added D4/E4 dimension to FIGURE 1 case outline and dimensions table. - glg | 14-11-05 | Charles F. Saffle |
| C | Add device type 03. Update voltages in section 1.3. Add $V_{IH1}$, $V_{IH2}$, $V_{IL1}$, $V_{IL2}$, $t_{AVSK}$, and $t_{AVET2}$; and add footnotes 9 and 10 to table IA. Update figure 1 to change A dimensions and add A5 dimensions. Update Figure 5 to add $t_{AVSK}$ and $t_{AVET2}$. Update boilerplate to reflect current MIL-PRF-38535 requirements. - llb | 19-04-18 | Charles F. Saffle |
| D | Vendor corrections to table I. – llb | 21-03-10 | James R. Eschmeyer |

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | D | D | D | D | D | D | D | D | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | | | | | | | | | | | | |

| REV STATUS | REV | D | D | D | D | D | D | D | D | D | D | D | D | D | D |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Gary L. Gross

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Laura Leeper

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
12-02-15

REVISION LEVEL
D

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2MEG X 39-BIT (80M), RADIATION-HARDENED, DUAL VOLTAGE SRAM, MULTICHIP MODULE

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-10206** |

SHEET 1 OF 22

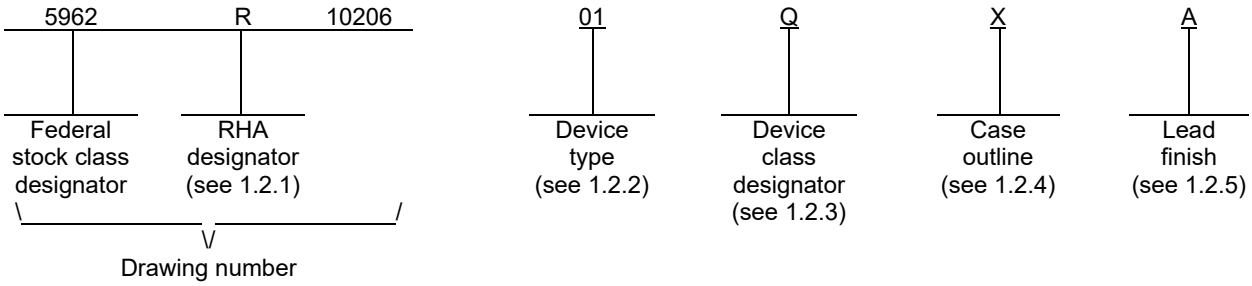
DSCC FORM 2233
APR 97

5962-E172-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

| Device type | Generic number | Circuit function | Access time | Case Operating Temp. Range |
|---|---|---|---|---|
| 01 | UT8R2M39 | 2M X 39-bit rad-hard SRAM | 22 ns | -55ºC to +105ºC |
| 02 | UT8R2M39 | 2M X 39-bit rad-hard SRAM with additional screening 1/ | 22 ns | -55ºC to +105ºC |
| 03 | UT8R2M39 | 2M X 39-bit rad-hard SRAM | 22 ns | -55ºC to +105ºC |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | See figure 1 | 132 | dual cavity quad flat pack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Device type 02 provides QML Q product with additional testing as specified in paragraph 4.2.1d.

1.3 Absolute maximum ratings. 2/ 3/

| | |
|---|---|
| Supply voltage range, ($V_{DD1}$) | -0.3 V dc to +2.4 V dc |
| Supply voltage range, ($V_{DD2}$) | -0.3 V dc to +4.5 V dc |
| Voltage range on any pin | -0.3 V dc to +4.5 V dc |
| Input current, dc | ± 10 mA |
| Power dissipation $P_D$ @ $T_C$ = 105ºC | 2.0 W 4/ |
| Case temperature range, ($T_C$) | -55ºC to +105ºC |
| Storage temperature range, ($T_{STG}$) | -65ºC to +150ºC |
| Junction temperature, ($T_J$) | +150ºC |
| Thermal resistance, junction-to-case, ($\theta_{JC}$): Case X | 10ºC/W |

1.4 Recommended operating conditions. 3/

| | |
|---|---|
| Supply voltage range, ($V_{DD1}$) | +1.7 V dc to +2.0 V dc |
| Supply voltage range, ($V_{DD2}$) | +2.3 V dc to +3.6 V dc |
| Supply voltage, ($V_{SS}$) | 0 V dc |
| Input voltage, dc | 0 V dc to $V_{DD2}$ |
| Case operating temperature range, ($T_C$) | -55ºC to +105ºC |
| Lead temperature, (per lead, 5 seconds) | +300ºC |

1.5 Radiation features

| | |
|---|---|
| Maximum total dose available (effective dose rate = 1 rads(Si)/s) | 100 K rads(Si) 5/ |
| Single event phenomenon (SEP): | |
| Effective linear energy transfer (LET) with no upsets (see 4.4.4.3) | 0.8 MeV-cm$^2$/mg 6/ |
| Effective LET with no latch-up (see 4.4.4.2) | ≤ 110 MeV-cm$^2$/mg |
| Single event upset (SEU) error rate (Adam's 90% worst environment) | 7.5 x $10^{-8}$ errors/bit-day |
| Neutron irradiation test (Displacement damage test) | 3.0 x $10^{14}$ n/cm$^2$ 7/ |

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltage values in this drawing are with respect to $V_{SS}$.

4/ Per MIL-STD-883, method 1012, section 3.4.1, $P_D = \frac{(+125ºC - +105ºC)}{\Theta_{JC}}$

5/ Devices are irradiated at a dose rate = 50 – 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and are guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to a low dose rate environment.

6/ 0.8 MeV-cm$^2$/mg is the estimated onset LET with no errors based on SEU testing where the minimum heavy ion LET available at the test facility was 0.9 MeV-cm$^2$/mg. At 0.9 MeV-cm$^2$/mg the cross-section is three orders of magnitude lower than the saturated cross-section and will therefore be close to the onset LET with no upsets.

7/ Parameter is guaranteed to the limit shown but not specifically tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation test circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_C \le +105°C$<br>$+1.7\ V \le V_{DD1} \le +2.0\ V$<br>$+2.3\ V \le V_{DD2} \le +3.6\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High-level input voltage | $V_{IH}$ | | 1, 2, 3 | 1, 2 | 2.2 | | V |
| Low-level input voltage | $V_{IL}$ | | 1, 2, 3 | 1, 2 | | 0.8 | V |
| High-level input voltage | $V_{IH1}$ | $V_{DD1}$ = 2.0 V, $V_{DD2}$ = 3.6 V<br>$V_{DD1}$ = 1.7 V, $V_{DD2}$ = 3.0 V | 1, 2, 3 | 3 | 2.2 | | V |
| Low-level input voltage | $V_{IL1}$ | $V_{DD1}$ = 2.0 V, $V_{DD2}$ = 3.6 V<br>$V_{DD1}$ = 1.7 V, $V_{DD2}$ = 3.0 V | 1, 2, 3 | 3 | | 0.8 | V |
| High-level input voltage | $V_{IH2}$ | $V_{DD1}$ = 2.0 V, $V_{DD2}$ = 2.7 V | 1, 2, 3 | 3 | 1.6 | | V |
| Low-level input voltage | $V_{IL2}$ | $V_{DD1}$ = 1.7 V, $V_{DD2}$ = 2.3 V | 1, 2, 3 | 3 | | 0.7 | V |
| High-level output voltage | $V_{OH1}$ | $I_{OH}$ = -4mA, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V | 1, 2, 3 | All | 0.8* $V_{DD2}$ | | V |
| High-level output voltage | $V_{OH2}$ | $I_{OH}$ = -2mA, 2.3 V ≤ $V_{DD2}$ ≤ 2.7 V | 1, 2, 3 | All | 0.8* $V_{DD2}$ | | V |
| Low-level output voltage | $V_{OL1}$ | $I_{OL}$ = 8 mA, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V | 1, 2, 3 | All | | 0.4 | V |
| Low-level output voltage | $V_{OL2}$ | $I_{OH}$ = 6 mA, 2.3 V ≤ $V_{DD2}$ ≤ 2.7 V | 1, 2, 3 | All | | 0.2* $V_{DD2}$ | V |
| Input capacitance 2/ | $C_{IN}$ | f = 1 MHz @ 0 V see 4.4.1e | 4 | All | | 29 | pF |
| Bidirectional I/O capacitance 2/ | $C_{IO}$ | | 4 | All | | 27 | pF |
| Input capacitance, device enables 2/ | $C_{EN}$ | | 4 | All | | 10 | pF |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{DD2}$ and $V_{SS}$ | 1, 2, 3 | All | -2 | 2 | µA |
| Three state output leakage current | $I_{OZ}$ | $V_O$ = $V_{DD2}$ and $V_{SS}$,<br>$V_{DD2}$ = $V_{DD2}$ (max);<br>$\overline{G}$ = $V_{DD2}$ (max) | 1, 2, 3 | All | -2 | 2 | µA |
| Short-circuit output current 3/ 4/ | $I_{OS}$ | $V_{DD2}$ = $V_{DD2}$ (max), $V_O$ = $V_{DD2}$,<br>$V_O$ = $V_{SS}$ | 1, 2, 3 | All | -100 | 100 | mA |
| Supply current operating @ 1 MHz 5/ | $I_{DD1}$ (OP1) | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2 V<br>$V_{IH}$ = $V_{DD2}$ - 0.2 V, $I_{OUT}$ = 0 mA<br>$V_{DD1}$ = 1.9 V, $V_{DD2}$ = $V_{DD2}$ (max) | 1, 2, 3 | All | | 10 | mA |
| | | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2 V<br>$V_{IH}$ = $V_{DD2}$ - 0.2 V, $I_{OUT}$ = 0 mA<br>$V_{DD1}$ = 2.0 V, $V_{DD2}$ = $V_{DD2}$ (max) | | | | 14 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_C \le +105°C$<br>$+1.7\ V \le V_{DD1} \le +2.0\ V$<br>$+2.3\ V \le V_{DD2} \le +3.6\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Supply current operating @ 45 MHz 5/ | $I_{DD1}$ (OP2) | Inputs: $V_{IL} = V_{SS} + 0.2\ V$<br>$V_{IH} = V_{DD2} - 0.2\ V$, $I_{OUT} = 0\ mA$<br>$V_{DD1} = 1.9\ V$, $V_{DD2} = V_{DD2}$(max) | 1, 2, 3 | All | | 210 | mA |
| | | Inputs: $V_{IL} = V_{SS} + 0.2\ V$<br>$V_{IH} = V_{DD2} - 0.2\ V$, $I_{OUT} = 0\ mA$<br>$V_{DD1} = 2.0\ V$, $V_{DD2} = V_{DD2}$ (max) | | | | 225 | |
| Supply current operating @ 1 MHz 5/ | $I_{DD2}$(OP1) | Inputs: $V_{IL} = V_{SS} + 0.2\ V$<br>$V_{IH} = V_{DD2} - 0.2\ V$, $I_{OUT} = 0\ mA$<br>$V_{DD1} = V_{DD1}$(max), $V_{DD2} = V_{DD2}$(max) | 1, 2, 3 | All | | 2 | mA |
| Supply current operating @ 45 MHz | $I_{DD2}$(OP2) | Inputs: $V_{IL} = V_{SS} + 0.2\ V$<br>$V_{IH} = V_{DD2} - 0.2\ V$, $I_{OUT} = 0\ mA$<br>$V_{DD1} = V_{DD1}$(max), $V_{DD2} = V_{DD2}$(max) | 1, 2, 3 | All | | 5 | mA |
| Functional test | | See 4.4.1c, $T_C = 25°C$ | 7, 8A, 8B | All | | | |
| Supply current standby @ 0 MHz (per die) | $I_{DD1}$(SB) | CMOS inputs, $I_{OUT} = 0$,<br>$\overline{E} = V_{DD2} - 0.2\ V$, | 1, 3 | All | | 15 | mA |
| | | $V_{DD1} = V_{DD1}$(max), M, D, P, L, R | 1 | | | 35 | |
| | | $V_{DD2} = V_{DD2}$(max) | 2 | | | 35 | |
| | $I_{DD2}$(SB) | | 1, 2, 3 | | | 3 | |
| Supply current standby A (18:0) @ 45 MHz (per die) | $I_{DD1}$(SB) | CMOS inputs, $I_{OUT} = 0$,<br>$\overline{E} = V_{DD2} - 0.2\ V$, | 1, 3 | All | | 15 | |
| | | $V_{DD1} = V_{DD1}$(max), M, D, P, L, R | 1 | | | 35 | |
| | | $V_{DD2} = V_{DD2}$(max) | 2 | | | 35 | |
| | $I_{DD2}$(SB) | | 1, 2, 3 | | | 3 | |
| Data retention current (per die) | $I_{DDR}$ | See figure 5 as applicable | 1 | All | | 3 | |
| | | $V_{DD2} = 2.3\ V$ M, D, P, L, R | 1 | | | 23.5 | |
| | | $\overline{E}$n as shown in figure 5, | 2 | | | 23.5 | |
| | | all other inputs = $V_{DD2}$ or $V_{SS}$ | 3 | | | 3 | |
| $V_{DD1}$ for data retention | $V_{DR}$ | | 1, 2, 3 | All | 1 | | V |
| Chip deselect to data retention time 6/ | $t_{EFR}$ | | 9, 10, 11 | All | 0 | | ns |
| Operation recovery time 6/ | $t_R$ | | 9, 10, 11 | All | $t_{AVAV1}$<br>$t_{AVAV2}$ | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_C \le +105°C$<br>$+1.7\ V \le V_{DD1} \le +2.0\ V$<br>$+2.3\ V \le V_{DD2} \le +3.6\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Read cycle time 2/ 10/ | $t_{AVAV1}$ | See figures 4 and 5 as applicable | 9, 10, 11 | All | 22 | | ns |
| Address valid to address valid skew time 9/ | $t_{AVSK}$ | | 9, 10, 11 | All | | 4 | |
| Read access time | $t_{AVQV}$ | | 9, 10, 11 | All | | 22 | |
| Output hold time 7/ | $t_{AXQX}$ | | 9, 10, 11 | All | 3 | | |
| $\overline{G}$-controlled output enable time 2/ 7/ | $t_{GLQX}$ | | 9, 10, 11 | All | 2 | | |
| $\overline{G}$-controlled read access time | $t_{GLQV}$ | | 9, 10, 11 | All | | 8 | |
| $\overline{G}$-controlled output three-state time 7/ | $t_{GHQZ}$ | | 9, 10, 11 | All | 2 | 6 | |
| Address setup time for read (E-controlled) 9/ | $t_{AVET2}$ | | 9, 10, 11 | All | -4 | | |
| $\overline{E}$-controlled output enable time 7/ | $t_{ETQX}$ | | 9, 10, 11 | All | 5 | | |
| $\overline{E}$-controlled access time | $t_{ETQV}$ | | 9, 10, 11 | All | | 22 | |
| $\overline{E}$-controlled output three-state time 7/ | $t_{EFQZ}$ | | 9, 10, 11 | All | 2 | 7 | |
| Write cycle time 8/ | $t_{AVAV2}$ | | 9, 10, 11 | All | 10 | | |
| Device enable to end of write | $t_{ETWH}$ | | 9, 10, 11 | All | 10 | | |
| Address set-up time for write ($\overline{E}$-controlled) | $t_{AVET}$ | | 9, 10, 11 | All | 0 | | |
| Address set-up time for write ($\overline{W}$-controlled) | $t_{AVWL}$ | | 9, 10, 11 | All | 0 | | |
| Write pulse width 8/ | $t_{WLWH}$ | | 9, 10, 11 | All | 8 | | |
| Address hold time for write ($\overline{W}$-controlled) | $t_{WHAX}$ | | 9, 10, 11 | All | 0 | | |
| Address hold time for device enable ($\overline{E}$-controlled) | $t_{EFAX}$ | | 9, 10, 11 | All | 0 | | |
| $\overline{W}$-controlled three-state time 7/ | $t_{WLQZ}$ | | 9, 10, 11 | All | | 7 | |
| $\overline{W}$-controlled output enable time 7/ | $t_{WHQX}$ | | 9, 10, 11 | All | 0 | | |
| Device enable pulse width ($\overline{E}$-controlled) | $t_{ETEF}$ | | 9, 10, 11 | All | 10 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_C \le +105°C$<br>$+1.7\ V \le V_{DD1} \le +2.0\ V$<br>$+2.3\ V \le V_{DD2} \le +3.6\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Data set-up time | $t_{DVWH}$ | See figures 4 and 5 as applicable | 9, 10, 11 | All | 5 | | ns |
| Data hold time | $t_{WHDX}$ | | 9, 10, 11 | All | 0 | | |
| Device enable controlled write pulse width 8/ | $t_{WLEF}$ | | 9, 10, 11 | All | 8 | | |
| Data set-up time | $t_{DVEF}$ | | 9, 10, 11 | All | 5 | | |
| Data hold time | $t_{EFDX}$ | | 9, 10, 11 | All | 0 | | |
| Address valid to end of write | $t_{AVWH}$ | | 9, 10, 11 | All | 10 | | |
| Write disable time 8/ | $t_{WHWL}$ | | 9, 10, 11 | All | 2 | | |

1/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C. Devices are irradiated at a dose rate = 50 – 300 rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and are guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to a low dose rate, environment.

2/ Measured only for initial qualification and after any design or process changes which may affect this parameter.

3/ Supplied as a design limit but not guaranteed or tested.

4/ Not more than one output may be shorted at a time, for a maximum duration of one second.

5/ Operating current limit does not include standby current.

6/ This parameter is guaranteed by design, but is neither characterized nor tested.

7/ Three-state is defined as a change from steady-state output voltage.

8/ $\overline{G} = V_{DD2}$.

9/ Guaranteed by design.

10/ Address changes prior to satisfying $t_{AVAV}$ minimum is an invalid operation.

Table IB. SEP test limits 1/ 2/

| Device type | Memory pattern | Single Event Upset 3/ 4/ Bias $V_{DD1}$ = 1.7 V, $V_{DD2}$ = 3.0 V | | Single Event Latch-up 5/ Bias $V_{DD1}$ = 2.0 V, $V_{DD2}$ = 3.6 V |
|---|---|---|---|---|
| | | Effective LET No upsets [MeV/(mg/cm$^2$)] | Maximum device Cross section (LET = 80) (cm$^2$) | Effective LET No latch-up [MeV/(mg/cm$^2$)] |
| All | 6/ | 0.8 7/ | $7.5 \times 10^{-8}$ | ≤110 |

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature $T_A$ = +25°C ±10°C.
4/ Soft error rate = $7.3 \times 10^{-8}$ error/bit-day assuming Adam's 90% worst case environment, geosynchronous orbit, and 100 mil aluminum shielding. Contact the device manufacturer for detailed information.
5/ Worst case test temperature $T_A$ = +125°C ±10°C.
6/ Memory patterns are as specified in Appendix A, Algorithm A herein.
7/ 0.8 MeV-cm$^2$/mg is the estimated onset LET with no errors based on SEU testing where the minimum heavy ion LET available at the test facility was 0.9 MeV-cm$^2$/mg. At 0.9 MeV-cm$^2$/mg the cross-section is three orders of magnitude lower than the saturated cross-section and will therefore be close to the onset LET with no upsets.

Case outline X

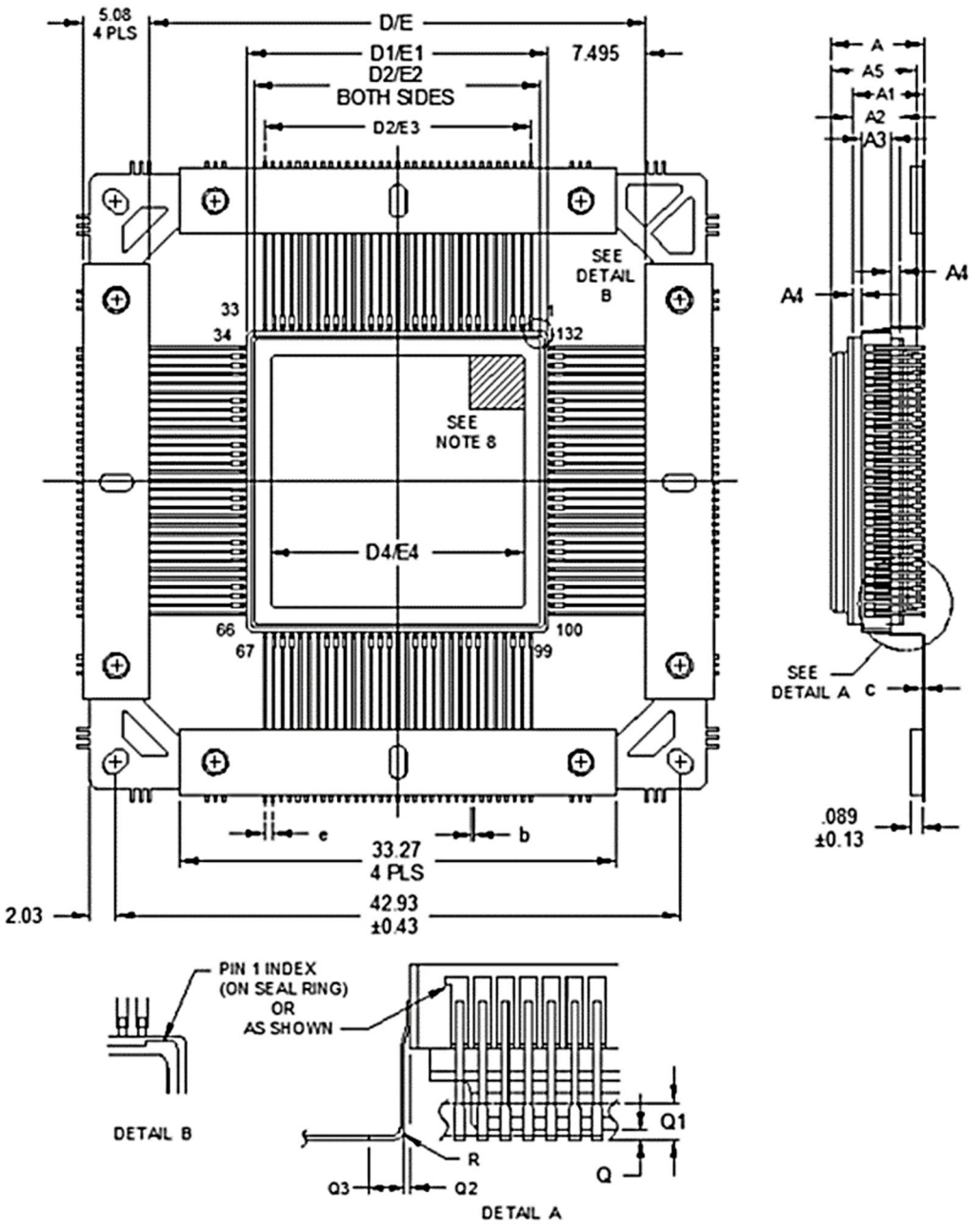



FIGURE 1. Case outline.

Case outline X

| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 7.71 | | .304 |
| A1 | | 6.02 | | .237 |
| A2 | | 3.61 | | .142 |
| A3 | 2.14 | 2.54 | .084 | .100 |
| A4 | 0.59 | 0.69 | .023 | .027 |
| A5 | | 7.28 | | .287 |
| b | 0.150 | 0.250 | .006 | .010 |
| c | 0.125 | 0.200 | .005 | .008 |
| e | 0.635 | | 0.025 | |
| D/E | 37.34 | 38.36 | 1.47 | 1.51 |
| D1/E1 | 22.63 | 23.09 | .891 | .909 |
| D2/E2 | 21.64 | 22.04 | .852 | .868 |
| D3/E3 | 20.12 | 20.52 | .792 | .808 |
| D4/E4 | 20.07 | 20.57 | .790 | .810 |
| Q | 0.205 | 0.405 | 0.008 | 0.016 |
| Q1 | 1.0 | | 0.039 | |
| Q2 | 0.25 | | 0.009 | |
| Q3 | 1.0 | | 0.039 | |
| R | 0.25 | | 0.009 | |

NOTES:
1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The seal ring and lids are electrically connected to $V_{SS}$.
4. Dogleg geometries optional within dimensions shown.
5. Lead finish is in accordance with MIL-PRF-38535.
6. Tie bar may have excise slots of various configurations and are vendor option. Tie bar dimensions are for reference only.
7. Package material: opaque 90% minimum Alumina ceramic.
8. ESD classification mark or dot is located in the pin 1 corner within area shown.
9. Q provides the clearance of the bottom lid and the circuit board.

FIGURE 1. Case outline – Continued.

| Case X, all device types. | | | | | | | |
|---|---|---|---|---|---|---|---|
| Terminal number | Terminal symbol | Terminal number | Terminal symbol | Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | TOP_DQ38 | 35 | A11 | 69 | DQ31 | 103 | A9 |
| 2 | BOT_DQ38 | 36 | A12 | 70 | DQ30 | 104 | A8 |
| 3 | DQ0 | 37 | A13 | 71 | DQ29 | 105 | A7 |
| 4 | DQ1 | 38 | VSS | 72 | DQ28 | 106 | VDD1 |
| 5 | DQ2 | 39 | NC | 73 | VDD2 | 107 | VSS |
| 6 | DQ3 | 40 | NC | 74 | VSS | 108 | A6 |
| 7 | VDD2 | 41 | NC | 75 | DQ27 | 109 | $\overline{W}$ |
| 8 | VSS | 42 | VDD2 | 76 | DQ26 | 110 | A18 |
| 9 | DQ4 | 43 | NC | 77 | DQ25 | 111 | NC |
| 10 | DQ5 | 44 | VDD1 | 78 | DQ24 | 112 | VDD1 |
| 11 | DQ6 | 45 | NC | 79 | VDD1 | 113 | NC |
| 12 | DQ7 | 46 | NC | 80 | VSS | 114 | NC |
| 13 | VDD1 | 47 | $\overline{E3}$ | 81 | NC | 115 | VDD1 |
| 14 | VSS | 48 | $\overline{E1}$ | 82 | VDD2 | 116 | NC |
| 15 | NC | 49 | VDD1 | 83 | NC | 117 | VSS |
| 16 | VDD2 | 50 | $\overline{G}$ | 84 | VDD2 | 118 | NC |
| 17 | NC | 51 | VSS | 85 | NC | 119 | NC |
| 18 | VDD2 | 52 | $\overline{E2}$ | 86 | VSS | 120 | VDD1 |
| 19 | NC | 53 | $\overline{E4}$ | 87 | VDD1 | 121 | NC |
| 20 | VSS | 54 | NC | 88 | DQ23 | 122 | A17 |
| 21 | VDD1 | 55 | NC | 89 | DQ22 | 123 | A5 |
| 22 | DQ8 | 56 | VDD1 | 90 | DQ21 | 124 | A4 |
| 23 | DQ9 | 57 | VDD2 | 91 | DQ20 | 125 | VSS |
| 24 | DQ10 | 58 | VSS | 92 | VSS | 126 | VDD1 |
| 25 | DQ11 | 59 | VSS | 93 | VDD2 | 127 | A3 |
| 26 | VSS | 60 | NC | 94 | DQ19 | 128 | A2 |
| 27 | VDD2 | 61 | NC | 95 | DQ18 | 129 | A1 |
| 28 | DQ12 | 62 | VSS | 96 | DQ17 | 130 | A0 |
| 29 | DQ13 | 63 | A14 | 97 | DQ16 | 131 | TOP_DQ37 |
| 30 | DQ14 | 64 | A15 | 98 | BOT_DQ35 | 132 | BOT_DQ37 |
| 31 | DQ15 | 65 | A16 | 99 | TOP_DQ35 | | |
| 32 | TOP_DQ32 | 66 | BOT_DQ34 | 100 | BOT_DQ36 | | |
| 33 | TOP_DQ33 | 67 | BOT_DQ33 | 101 | TOP_DQ36 | | |
| 34 | TOP_DQ34 | 68 | BOT_DQ32 | 102 | A10 | | |

FIGURE 2. Terminal connections.

| G | W | $\overline{E1}$ or $\overline{E2}$ or $\overline{E3}$ or $\overline{E4}$ 1/ | I/O Mode | Mode |
|---|---|---|---|---|
| X | X | H | Three-state | Standby |
| X | L | L | Data in | Write |
| H | H | L | Three-state | Read (device active, outputs disabled) |

1/ Only one enable may be active at any given time; L = low, H = high, X = don't care, Z = high impedance.

FIGURE 3. Truth table.

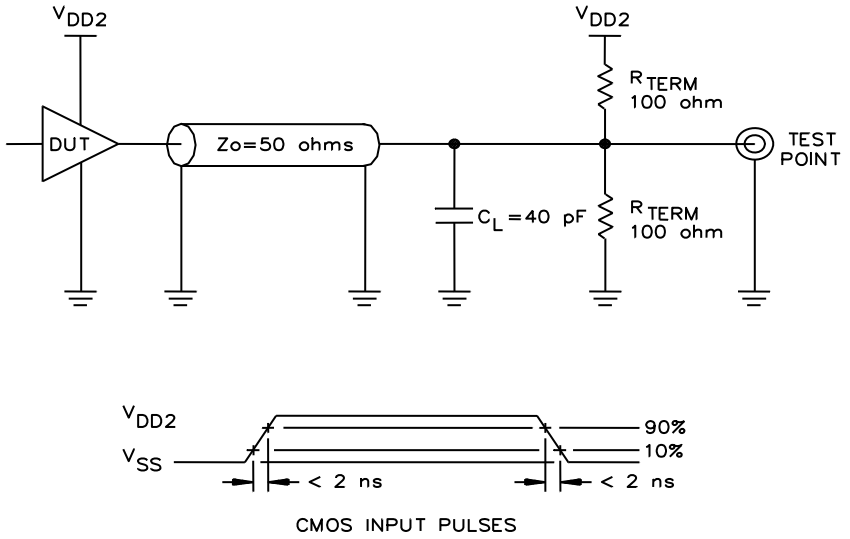
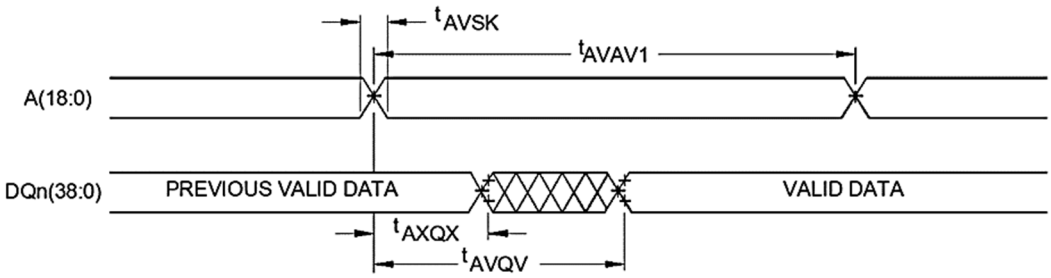
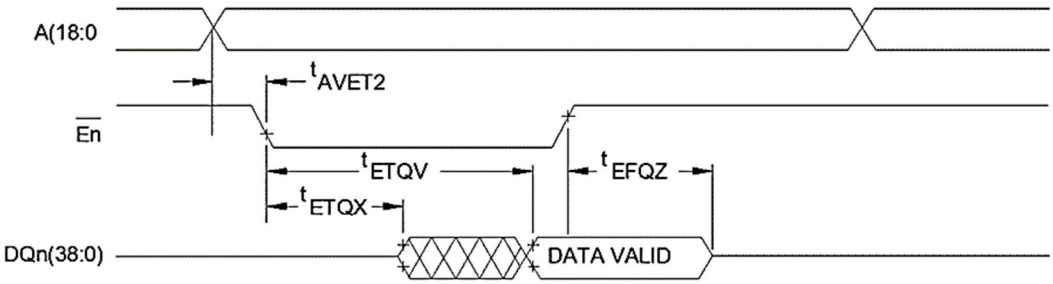



FIGURE 4. Output load circuit




SRAM READ CYCLE 1: ADDRESS ACCESS

Note: $\overline{En}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min), only one $\overline{En}$ may be active at any given time.

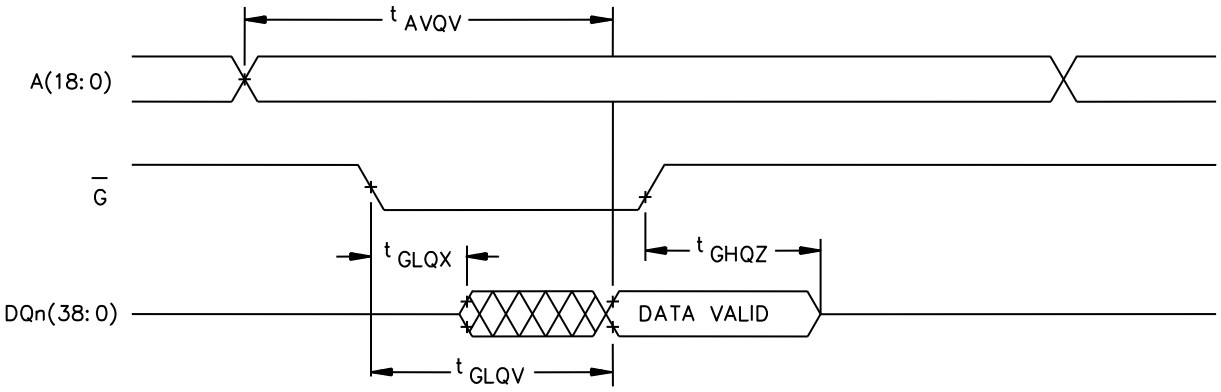



SRAM READ CYCLE 2: CHIP ENABLE-CONTROLLED ACCESS

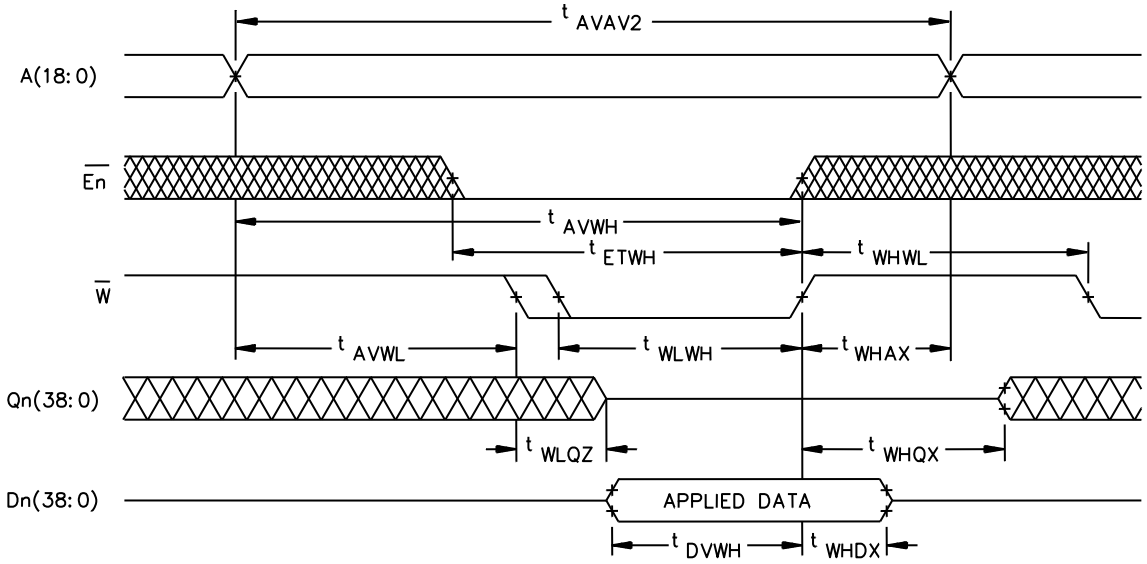
Note: $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min), only one $\overline{En}$ may be active at any given time.

FIGURE 5. Timing waveforms.

Note: $\overline{E} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min), only one $\overline{En}$ may be active at any given time.



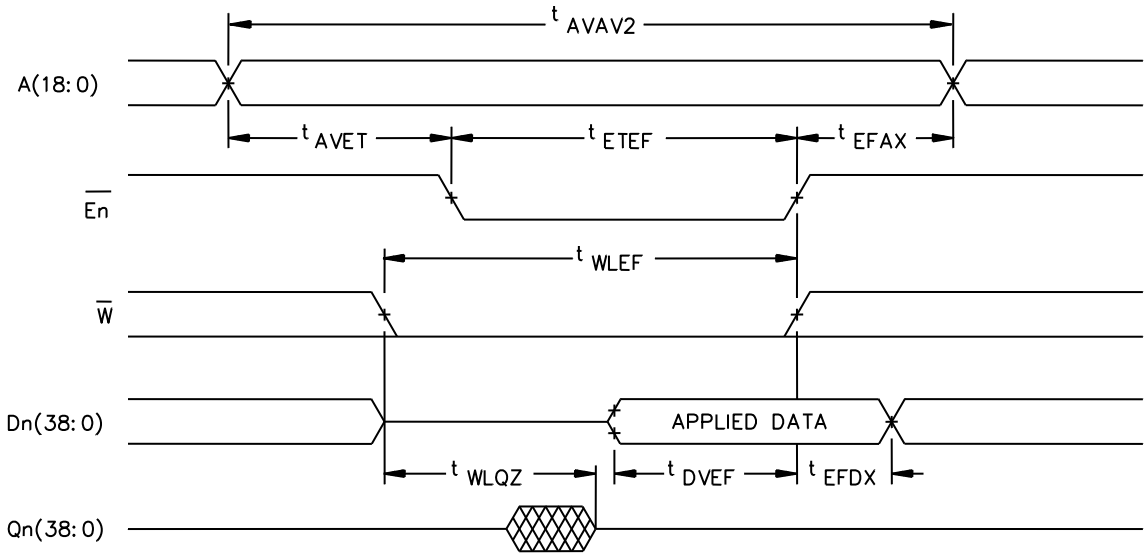

SRAM READ CYCLE 3: OUTPUT ENABLE-CONTROLLED ACCESS




SRAM WRITE CYCLE 1: WRITE ENABLE-CONTROLLED ACCESS

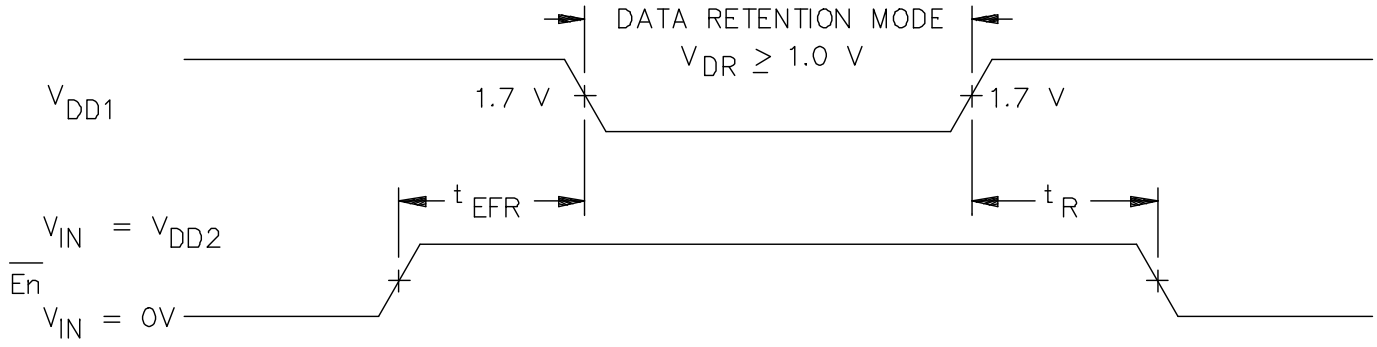
Note: $\overline{G} \le V_{IL}$ (max). If $\overline{G} \ge V_{IH}$ (min) then Qn(38:0) will be in three-state for the entire cycle. Only one $\overline{En}$ may be active at any given time.

FIGURE 5. Timing waveforms – Continued.




SRAM WRITE CYCLE 2: CHIP ENABLE-CONTROLLED ACCESS

Note: $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(38:0) will be in three-state for the entire cycle. Only one $\overline{En}$ may be active at any given time.




DATA RETENTION WAVEFORM

FIGURE 5. Timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 02.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883.

(2) 100% PIND (Single pass).

(3) Serialization.

(4) 100% X-ray (Top view only).

(5) Group A.

(6) Accelerated dynamic burn-in, deltas, PDA (3%) for Functional Test only, and PDA (5%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

| Line Number | Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | - - - | 1, 7, 9 |
| 2 | Static burn-in I and II (method 1015) | Not required | Required |
| 3 | Same as line 1 | - - - | 1*, 7* Δ |
| 4 | Dynamic burn-in (method 1015) | Required | Required |
| 5 | Same as line 1 | - - - | 1*, 7* Δ |
| 6 | Final electrical parameters | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| 7 | Group A test requirements | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| 8 | Group C end-point electrical parameters | 2, 3, 7, 8A, 8B | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ |
| 9 | Group D end-point electrical parameters | 2, 3, 8A, 8B | 2, 3, 8A, 8B |
| 10 | Group E end-point electrical parameters | 1, 7, 9 | 1, 7, 9 |

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan..
7/ See 4.4.1d.

Table IIB. Delta limits at +25ºC.

| Parameter 1/ | Limit | Unit |
|---|---|---|
| Supply current standby at 0 MHz $I_{DD2}$ | ± 10% of specified value in Table IA | mA |

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD78 may be used for reference.

e. Subgroup 4 ($C_{IN}$ and $C_{IO}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C +5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º $\leq$ angle $\leq$ 60º). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq$ $10^6$ ions/$cm^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/$cm^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature $\pm$10ºC for single event latch-up testing.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and 0this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Occurrence of latch-up (SEP).

APPENDIX A
Appendix A forms a part of SMD 5962-10206

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-03-10

Approved sources of supply for SMD 5962-10206 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962R1020601QXC | 65342 | UT8R2M39-22XFC |
| 5962R1020601VXC | 65342 | UT8R2M39-22XFC |
| 5962R1020602QXC | 65342 | UT8R2M39-22XFC |
| 5962R1020603QXC | 65342 | UT8R2M39-22XFC |
| 5962R1020603VXC | 65342 | UT8R2M39-22XFC |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 65342 | Cobham Colorado Springs, Inc.<br>4350 Centennial Blvd.<br>Colorado Springs, CO 80907-7370 |