REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added D4/E4 dimension to FIGURE 1 case outline and dimensions table. – glg	14-11-05	Charles F. Saffle
B	Update drawing to latest MIL-PRF-38535 requirements. – jt	21-08-17	James R. Eschmeyer
C	VEN add device types 05 and 06, increased abs. max. voltage ratings in ¶1.3, add V_{IH1}, V_{IH2}, V_{IL1}, V_{IL}, t_{AVSK}, and t_{AVET2} to table I, update table I footnotes, update Figure 1 for Case X to add A5 dimension, update Figures 2, 5, and 6. Update boilerplate to current Section 508 Compliance and MIL-PRF-38535 requirements. - llb	24-03-14	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	C	C	C	C	C	C	C	C	C	C											
SHEET	23	24	25	26	27	28	29	30	31	32											
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
12-09-24

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

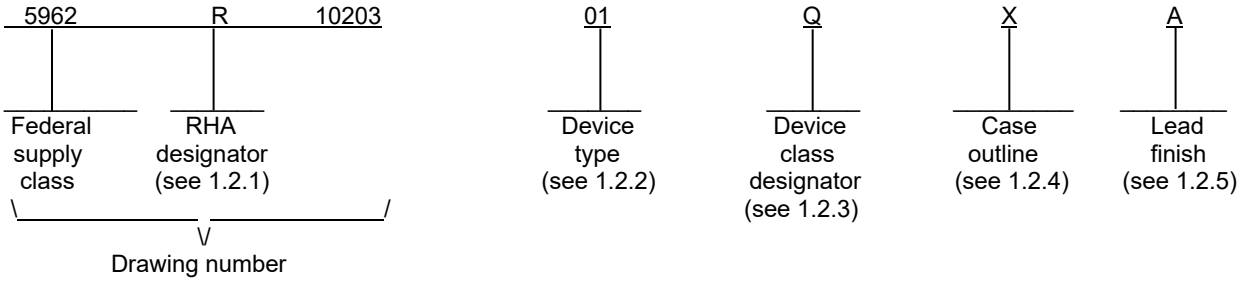
MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2MEG X 32-BIT (64M), RADIATION-HARDENED, DUAL VOLTAGE SRAM with embedded EDAC, MULTICHIP MODULE

AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **67268**	**5962-10203**
		SHEET	1 OF 32	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	UT8ER2M32M	2M X 32-bit rad-hard SRAM master	22 ns
02	UT8ER2M32S	2M X 32-bit rad-hard SRAM slave	22 ns
03	UT8ER2M32M	2M X 32-bit rad-hard SRAM master, with additional screening 1/	22 ns
04	UT8ER2M32S	2M X 32-bit rad-hard SRAM slave, with additional screening 1/	22 ns
05	UT8ER2M32M	2M X 32-bit rad-hard SRAM master	22 ns
06	UT8ER2M32S	2M X 32-bit rad-hard SRAM slave	22 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	132	dual cavity quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Device types 03 and 04 provides QML Q product with additional testing as specified in paragraph 4.2.1d.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{DD1})	-0.3 V dc to +2.4 V dc
Supply voltage range, (V_{DD2})	-0.3 V dc to +4.5 V dc
Voltage range on any pin	-0.3 V dc to +4.5 V dc
Input current, dc	± 10 mA
Power dissipation permitted, P_D @ T_C = 105ºC	2.0 W 4/
Case temperature range, (T_C)	-55ºC to +105ºC
Storage temperature range, (T_{STG})	-65ºC to +150ºC
Junction temperature, (T_J)	+150ºC
Thermal resistance, junction-to-case, (θ_{JC}): Case X	10ºC/W

1.4 Recommended operating conditions. 3/

Supply voltage range, (V_{DD1})	+1.7 V dc to +2.0 V dc
Supply voltage range, (V_{DD2})	+2.3 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to V_{DD2}
Case operating temperature range, (T_C)	-55ºC to +105ºC

1.5 Radiation features.

Maximum total dose available (effective dose rate = 1 rads(Si)/s)	10.0×10^4 rads(Si) 5/
Single event phenomenon (SEP) effective	
linear energy threshold (LET) with no upsets	N/A 6/
with no latch-up	≤ 110 MeV-cm^2/mg
Single event upset	8.1×10^{-16} errors/bit-day 6/ 7/
Neutron irradiation	3.0×10^{14} n/cm^2

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltage values in this drawing are with respect to V_{SS}.

4/ Per MIL-STD-883, Method 1012.1, section 3.4.1, Pd = (125°C – 105°C)/θ_{JC}.

5/ Device is irradiated at a dose rate = 50 – 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to a low dose rate environment.

6/ Single event upsets are driven by charged particle flux, rather than 'LET', due to embedded error detection and correction.

7/ Assuming geosynchronous orbit, Adam's 90% worst environment and 152 KHz default scrub rate (97.0% SRAM availability).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 EDAC configuration. EDAC configuration tables and definitions are specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in the appendix (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +105°C$ $+1.7\ V \le V_{DD1} \le +2.0\ V$ $+2.3\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}		1, 2, 3	All	2.2		V
Low-level input voltage	V_{IL}		1, 2, 3	All		0.8	V
High-level input voltage	V_{IH1}	V_{DD1} = 2.0 V, V_{DD2} = 3.6 V, V_{DD1} = 1.7 V, V_{DD2} = 3.0 V	1, 2, 3	5, 6	2.2		V
High-level input voltage	V_{IH2}	V_{DD1} = 2.0 V, V_{DD2} = 2.7 V,	1, 2, 3	5, 6	1.6		V
Low-level input voltage	V_{IL1}	V_{DD1} = 2.0 V, V_{DD2} = 3.6 V, V_{DD1} = 1.7 V, V_{DD2} = 3.0 V	1, 2, 3	5, 6		0.8	V
Low-level input voltage	V_{IL2}	V_{DD1} = 1.7 V, V_{DD2} = 2.3 V	1, 2, 3	5, 6		0.7	V
High-level output voltage	V_{OH1}	I_{OH} = -4mA, 3.0 V ≤ V_{DD2} ≤ 3.6 V	1, 2, 3	All	0.8*V_{DD2}		V
High-level output voltage	V_{OH2}	I_{OH} = -2mA, 2.3 V ≤ V_{DD2} ≤ 2.7 V	1, 2, 3	All	0.8*V_{DD2}		V
Low-level output voltage 2/	V_{OL1}	I_{OL} = 8 mA, 3.0 V ≤ V_{DD2} ≤ 3.6 V	1, 2, 3	All		0.4	V
Low-level output voltage 2/	V_{OL2}	I_{OL} = 6 mA, 2.3 V ≤ V_{DD2} ≤ 2.7 V	1, 2, 3	All		0.2*V_{DD2}	V
Input capacitance 3/ (Device Enables)	C_{EN}	f = 1 MHz @ 0 V see 4.4.1e	4	All		10	pF
Input capacitance 3/	C_{IN}	f = 1 MHz @ 0 V see 4.4.1e	4	All		29	pF
Bidirectional I/O capacitance 3/	C_{IO}		4	All		27	pF
Input leakage current	I_{IN}	V_{IN} = V_{DD2} and V_{SS}	1, 2, 3	All	-2	2	µA
Three state output leakage current 4/	I_{OZ}	V_O = V_{DD2} and V_{SS}, V_{DD2} = V_{DD2} (max); $\overline{G}$ = V_{DD2} (max)	1, 2, 3	All	-2	2	µA
Short-circuit output current 5/ 6/	I_{OS}	V_{DD2} = V_{DD2} (max), V_O = V_{DD2}, V_O = V_{SS}	1, 2, 3	All	-100	100	mA
Supply current operating @ 1 MHz 7/ 8/	$I_{DD1}^{(OP1)}$	Inputs: V_{IL} = V_{SS} +0.2 V V_{IH} = V_{DD2} -0.2 V, I_{OUT} = 0 mA V_{DD1} = 1.9 V, V_{DD2} = V_{DD2} (max)	1, 2, 3	All		10 9/	mA
		Inputs: V_{IL} = V_{SS} +0.2 V V_{IH} = V_{DD2} -0.2 V, I_{OUT} = 0 mA V_{DD1} = 2.0 V, V_{DD2} = V_{DD2} (max)				14 9/	
Supply current operating @ 50 MHz 7/ 8/	$I_{DD1}^{(OP2)}$	Inputs: V_{IL} = V_{SS} +0.2 V V_{IH} = V_{DD2} -0.2 V, I_{OUT} = 0 mA V_{DD1} = 1.9 V, V_{DD2} = V_{DD2} (max)	1, 2, 3	All		210 9/	mA
		Inputs: V_{IL} = V_{SS} +0.2 V V_{IH} = V_{DD2} -0.2 V, I_{OUT} = 0 mA V_{DD1} = 2.0 V, V_{DD2} = V_{DD2} (max)				225 9/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +105°C$ $+1.7\ V \le V_{DD1} \le +2.0\ V$ $+2.3\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply current operating @ 1 MHz 7/ 8/	$I_{DD2}^{(OP1)}$	Inputs: $V_{IL} = V_{SS} +0.2\ V$ $V_{IH} = V_{DD2} -0.2\ V$, $I_{OUT} = 0\ mA$ $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		1, 2, 3	All		2	mA
Supply current operating @ 50 MHz 7/ 8/	$I_{DD2}^{(OP2)}$	Inputs: $V_{IL} = V_{SS} +0.2\ V$ $V_{IH} = V_{DD2} -0.2\ V$, $I_{OUT} = 0\ mA$ $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		1, 2, 3	All		5	mA
Functional test		See 4.4.1c, $T_C = 25°C$		7, 8A, 8B	All			
Supply current standby @ 0 MHz EDAC bypassed (per die)	$I_{DD1}^{(SB)}$	CMOS inputs, $I_{OUT} = 0\ mA$, $V_{IL} = 0\ V$, $V_{IH} = V_{DD2}$(max), $\overline{E} = V_{DD2} -0.2\ V$,		1, 3	All		15	mA
		$V_{DD1} = V_{DD1}$(max),	**R**	1			35	
				2			35	
	$I_{DD2}^{(SB)}$	$V_{DD2} = V_{DD2}$ (max)		1, 2, 3			3	mA
Supply current standby A(18:0) @ 50 MHz EDAC bypassed (per die)	$I_{DD1}^{(SB)}$	CMOS inputs, $I_{OUT} = 0\ mA$, $V_{IL} = 0\ V$, $V_{IH} = V_{DD2}$(max), $\overline{E} = V_{DD2} -0.2\ V$,		1, 3	All		15	mA
		$V_{DD1} = V_{DD1}$(max),	**R**	1			35	
				2			35	
	$I_{DD2}^{(SB)}$	$V_{DD2} = V_{DD2}$ (max)		1, 2, 3			3	mA
Read cycle time 3/ 10/	t_{AVAV1}	See figures 4 and 5 as applicable		9, 10, 11	All	22		ns
Address valid to address valid skew time 11/	t_{AVSK}			9, 10, 11	All		4	ns
Address setup time for read ($\overline{E}$-controlled) 11/	t_{AVET2}			9, 10, 11	All	-4		ns
Read access time	t_{AVQV1}			9, 10, 11	All		22	ns
Output hold time 9/	t_{AXQX}			9, 10, 11	All	1.5		ns
$\overline{G}$-controlled output enable time 3/ 9/	t_{GLQX}			9, 10, 11	All	1		ns
$\overline{G}$-controlled read access time	t_{GLQV}			9, 10, 11	All		10	ns
$\overline{G}$-controlled output three-state time 9/	t_{GHQZ}			9, 10, 11	All	1	8	ns
$\overline{E}$-controlled output enable time 9/	t_{ETQX}			9, 10, 11	All	4		ns
$\overline{E}$-controlled access time	t_{ETQV}			9, 10, 11	All		22	ns
$\overline{E}$-controlled output three-state time 9/	t_{EFQZ}			9, 10, 11	All	2	9	ns
Address to error flag valid	t_{AVMV}			9, 10, 11	All		22	ns
Address to error flag hold time from address change 9/	t_{AXMX}			9, 10, 11	All	1.5		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +105°C$ $+1.7\ V \le V_{DD1} \le +2.0\ V$ $+2.3\ V \le V_{DD2} \le +3.6\ V$ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{G}$-controlled error flag enabled time 9/	t_{GLMX}	See figures 4 and 5 as applicable	9, 10,11	All	0		ns
$\overline{G}$-controlled error flag valid	t_{GLMV}		9, 10,11	All		8	ns
$\overline{E}$-controlled error flag enable time 9/	t_{ETMX}		9, 10, 11	All	4		ns
$\overline{E}$-controlled error flag time	t_{ETMV}		9, 10, 11	All		22	ns
$\overline{G}$-controlled error flag three-state time 9/	t_{GHMZ}		9, 10, 11	All	1	9	ns
Write cycle time 12/	t_{AVAV2}	See figures 4 and 5 as applicable, $\overline{G} = V_{DD2}$	9, 10, 11	All	10		ns
Device enable to end of write	t_{ETWH}	See figures 4 and 5 as applicable	9, 10, 11	All	10		ns
Address set-up time for write ($\overline{E}$-controlled)	t_{AVET}		9, 10, 11	All	0		ns
Address set-up time for write ($\overline{W}$-controlled)	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width 12/	t_{WLWH}		9, 10, 11	All	8		ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	All	0		ns
Address hold time for device enable ($\overline{E}$-controlled)	t_{EFAX}		9, 10, 11	All	0		ns
$\overline{W}$-controlled three-state time 9/	t_{WLQZ}		9, 10, 11	All		9	ns
$\overline{W}$-controlled output enable time 9/	t_{WHQX}		9, 10, 11	All	0		ns
Device enable pulse width ($\overline{E}$-controlled)	t_{ETEF}		9, 10, 11	All	10		ns
Data set-up time	t_{DVWH}		9, 10, 11	All	5		ns
Data hold time	t_{WHDX}		9, 10, 11	All	0		ns
Device enable controlled write pulse width 12/	t_{WLEF}		9, 10, 11	All	8		ns
Data set-up time	t_{DVEF}		9, 10, 11	All	5		ns
Data hold time	t_{EFDX}		9, 10, 11	All	0		ns
Address valid to end of write	t_{AVWH}		9, 10, 11	All	10		ns
Write disable time 12/	t_{WHWL}	See figures 4 and 5 as applicable, $\overline{G} = V_{DD2}$	9, 10, 11	All	2		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}C \le T_C \le +105^{\circ}C$ $+1.7\ V \le V_{DD1} \le +2.0\ V$ $+2.3\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master mode AC characteristics							
User programmable $\overline{BUSY}$ low to $\overline{SCRUB}$ low 13/	t_{BLSL}	See figures 4 and 5 as applicable	9, 10, 11	All	50n	90n+1	ns
$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	t_{SLSH1}		9, 10, 11	All	200	350	ns
$\overline{SCRUB}$ high to $\overline{BUSY}$ high	t_{SHBH}		9, 10, 11	All	50	85	ns
Scrub rate period 14/	t_{SCRT}		9, 10, 11	All	2^n50 +200	2^n90 +350	ns
Slave mode AC characteristics							
$\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave)	t_{SLSH2}	See figures 4 and 5 as applicable	9, 10, 11	All	200		ns
$\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave) 15/	t_{SHSL}		9, 10, 11	All	400		ns
EDAC control register AC characteristics							
Address valid to address valid for control register cycle	t_{AVAV3}	See figures 4 and 5 as applicable	9, 10, 11	All	200		ns
Address valid to control low	t_{AVCL}		9, 10, 11	All	400		ns
Address valid to enable valid	t_{AVEX}		9, 10, 11	All	200		ns
Address to data valid control register read	t_{AVQV3}		9, 10, 11	All		400	ns
MBE control EDAC disable time 9/	t_{MLQX}		9, 10, 11	All	3		ns
Output tri-state time 9/	t_{GHQZ3}		9, 10, 11	All	2	9	ns
MBE low to output enable 15/	t_{MLGL}		9, 10, 11	All	85		ns
MBE high to address valid	t_{CHAV}		9, 10, 11	All	0		ns
MBE low to address invalid	t_{CLAX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

1/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are only characterized at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.
2/ The $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ pins for the master device (device types 01, 03, and 05) are tested functionally for V_{OL} specification.
3/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in Table IA.
4/ The $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ pins for the master device (device types 01, 03, and 05) are guaranteed by design, but neither tested nor characterized.
5/ Supplied as a design limit but not guaranteed or tested.
6/ Not more than one output may be shorted at a time, for a maximum duration of one second.
7/ EDAC enabled. Default Scrub Rate Period applicable to master device (device types 01, 03, and 05) only.
8/ Operating current limit includes standby current.
9/ Three-state is defined as a 300 mV change from steady-state output voltage.
10/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation.
11/ Guaranteed by design.
12/ Test performed with $\overline{G}$ high.
13/ The value n is decimal equivalent of hexadecimal value 0x0 through 0xF programmed into control register address bits A_4-A_7 by user. Default value for n = 10.
14/ The value n is decimal equivalent of hexadecimal value 0x3 through 0xF programmed into control register address bits A_0-A_3 by user. Default value for n = 7.
15/ Guaranteed by design, neither tested nor characterized.

Table IB. SEP test limits 1/ 2/

Device type	Single Event Upset 3/ V_{DD1} = 1.7 V, V_{DD2} = 3.0 V		Single Event Latch-up 4/ Bias V_{DD1} = 2.0 V, V_{DD2} = 3.6 V
	Onset LET No upsets [MeV/(mg/cm^2)]	Maximum device Cross section (LET = 80) (cm2)	Effective LET No latch-up [MeV/(mg/cm^2)]
All	5/	5/	≤ 110

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature T_A = +25°C ±10°C.
4/ Worst case test temperature T_A = +125°C ±10°C.
5/ Soft error rate = 8.1 x 10^{-16} error/bit-day assuming Adam's 90% worst case environment, geosynchronous orbit, 100 mil aluminum shielding. Contact the device manufacturer for detailed information.

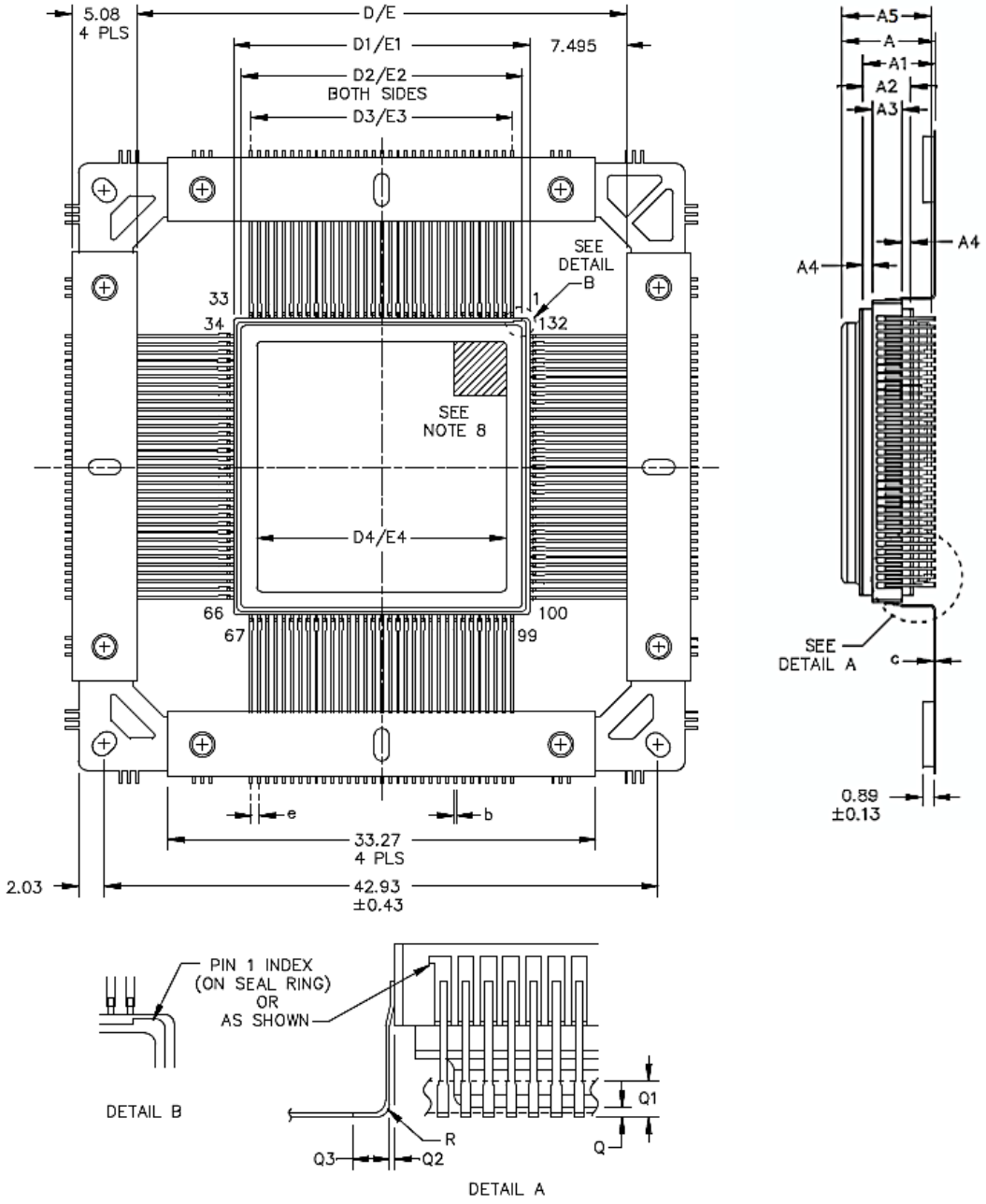


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-10203**
		REVISION LEVEL C	SHEET **11**

Case outline X

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		7.71		.304
A1		6.02		.237
A2		3.61		.142
A3	2.14	2.54	.084	.100
A4	0.59	0.69	.023	.027
A5		7.28		.287
b	0.150	0.250	.006	.010
c	0.125	0.200	.005	.008
e	0.635		0.025	
D/E	37.34	38.36	1.47	1.51
D1/E1	22.63	23.09	.891	.909
D2/E2	21.64	22.04	.852	.868
D3/E3	20.12	20.52	.792	.808
D4/E4	20.07	20.57	.790	.810
Q	0.205	0.405	0.008	0.016
Q1	1.0		0.039	
Q2	0.25		0.009	
Q3	1.0		0.039	
R	0.25		0.009	

NOTES:
1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The seal ring and lids are electrically connected to VSS.
4. Dogleg geometries optional within dimensions shown.
5. Lead finish is in accordance with MIL-PRF-38535.
6. Tie bar may have excise slots of various configurations and are vendor option. Tie bar dimensions are for reference only.
7. Package material: opaque 90% minimum Alumina ceramic.
8. ESD classification mark or dot is located in the pin 1 corner within area shown.
9. Q provides the clearance of the bottom lid and the circuit board.

FIGURE 1. Case outline – Continued.

Case X

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VSS	35	A11
2	VSS	36	A12
3	DQ0	37	A13
4	DQ1	38	VSS
5	DQ2	39	NC
6	DQ3	40	NC
7	VDD2	41	NC
8	VSS	42	$\overline{\text{VSS}}$
9	DQ4	43	$\overline{\text{BUSY}}$ 1/
10	DQ5	44	VDD1
11	DQ6	45	NC
12	DQ7	46	$\overline{\text{NC}}$
13	VDD1	47	$\overline{\text{E3}}$
14	VSS	48	$\overline{\text{E1}}$
15	NC	49	VDD1
16	VDD2	50	$\overline{\text{G}}$
17	NC	51	VSS
18	VDD2	52	$\overline{\text{E2}}$
19	NC	53	$\overline{\text{E4}}$
20	VSS	54	NC
21	VDD1	55	NC
22	DQ8	56	VDD1
23	DQ9	57	$\overline{\text{SCRUB}}$
24	DQ10	58	MBE
25	DQ11	59	VDD2
26	VSS	60	NC
27	VDD2	61	NC
28	DQ12	62	VSS
29	DQ13	63	A14
30	DQ14	64	A15
31	DQ15	65	A16
32	VSS	66	VSS
33	VSS	67	VSS
34	VSS	68	VSS

FIGURE 2. Terminal connections.

Case X – Continued.

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
69	DQ31	102	A10
70	DQ30	103	A9
71	DQ29	104	A8
72	DQ28	105	A7
73	VDD2	106	VDD1
74	VSS	107	VSS
75	DQ27	108	$\overline{A6}$
76	DQ26	109	$\overline{W}$
77	DQ25	110	A18
78	DQ24	111	NC
79	VDD1	112	VDD1
80	VSS	113	NC
81	NC	114	NC
82	VDD2	115	VDD1
83	NC	116	NC
84	VDD2	117	VSS
85	NC	118	NC
86	VSS	119	NC
87	VDD1	120	VDD1
88	DQ23	121	NC
89	DQ22	122	A17
90	DQ21	123	A5
91	DQ20	124	A4
92	VSS	125	VSS
93	VDD2	126	VDD1
94	DQ19	127	A3
95	DQ18	128	A2
96	DQ17	129	A1
97	DQ16	130	A0
98	VSS	131	VSS
99	VSS	132	VSS
100	VSS		
101	VSS		

1/ Device types 01, 03, and 05 = $\overline{BUSY}$. Device types 02, 04, and 06 = NC

FIGURE 2. Terminal connections – Continued.

SRAM Device Control Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E1}$, $\overline{E2}$, $\overline{E3}$, or $\overline{E4}$ 1/	I/O Mode	Mode
X	X	H	DQ(31:0) Three-state	Standby
X	L	L	DQ(31:0) Data in	Write
H	H	L	DQ(31:0) Three-state	Word Read (device active, outputs disabled)
L	H	L	DQ(31:0) Data out	Word Read

1/ Only one enable may be active at any given time.

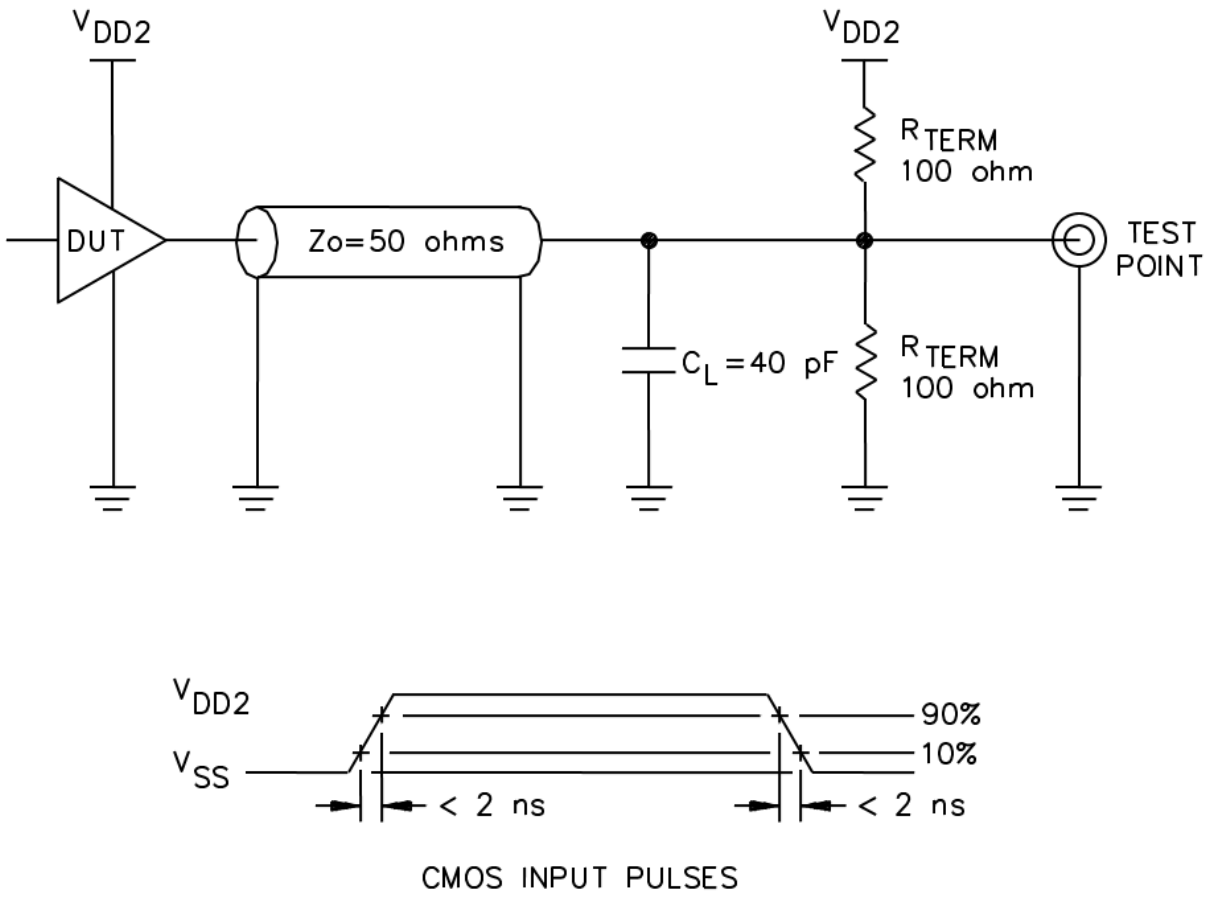
Note : L = low, H = high, X = don't care, Z = high impedance

EDAC Control Pin Operation Truth Table

MBE	$\overline{SCRUB}$	$\overline{BUSY}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

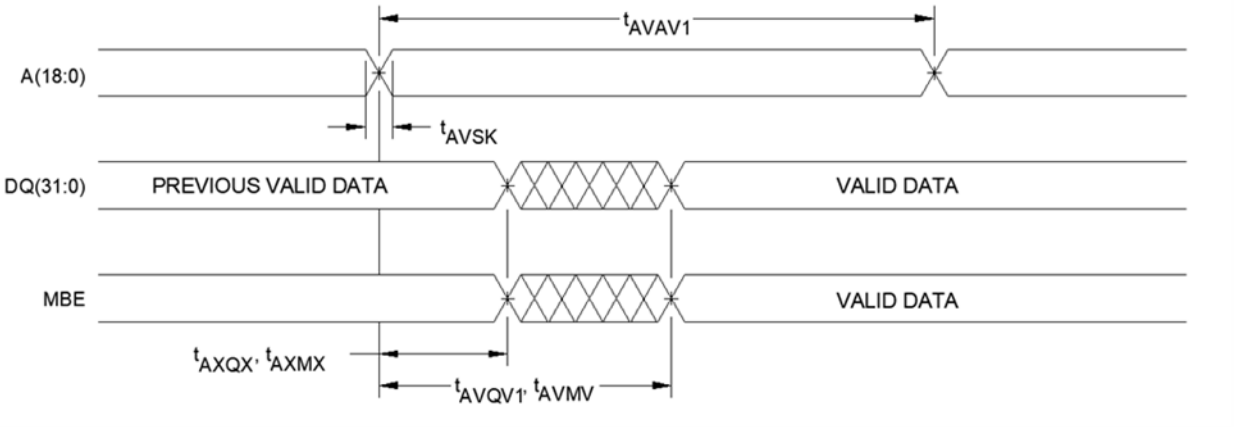
Note : L = low, H = high, X = don't care, Z = high impedance

FIGURE 3. Truth table.



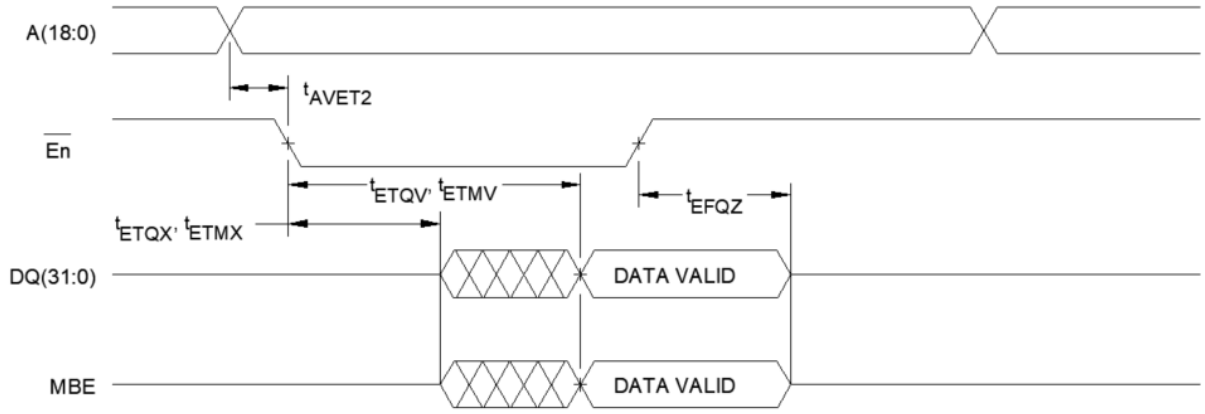
Note: 50 pF including scope probe and test socket.

FIGURE 4. Output load circuit.



Note: $\overline{En}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min), only one $\overline{En}$ may be active at any given time.

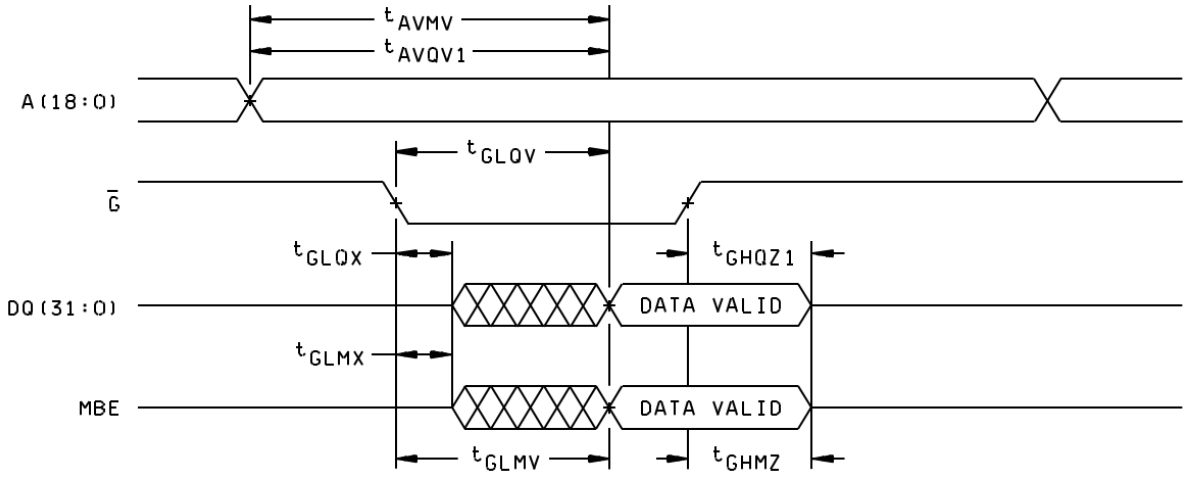
SRAM read cycle 1: Address Access



Notes:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min), only one $\overline{En}$ may be active at any given time.
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

SRAM read cycle 2: Chip Enable Access

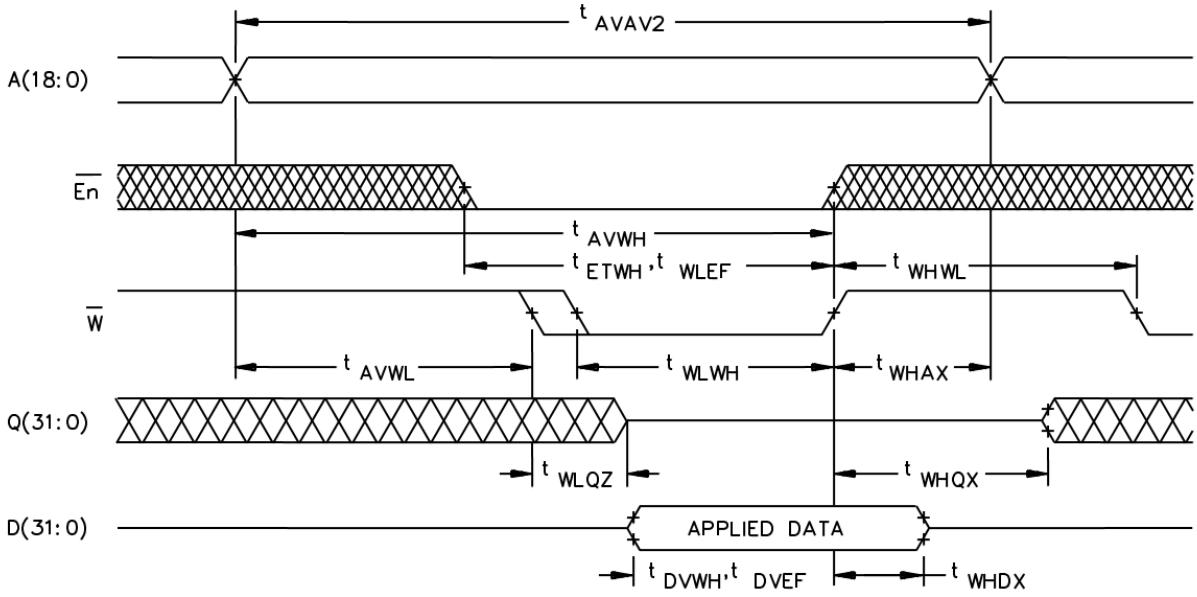
FIGURE 5. Timing waveforms.



Notes:
1. $\overline{En} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)
2. $\overline{SCRUB} \ge V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

SRAM read cycle 3: Output Enable Access

FIGURE 5. Timing waveforms – Continued.

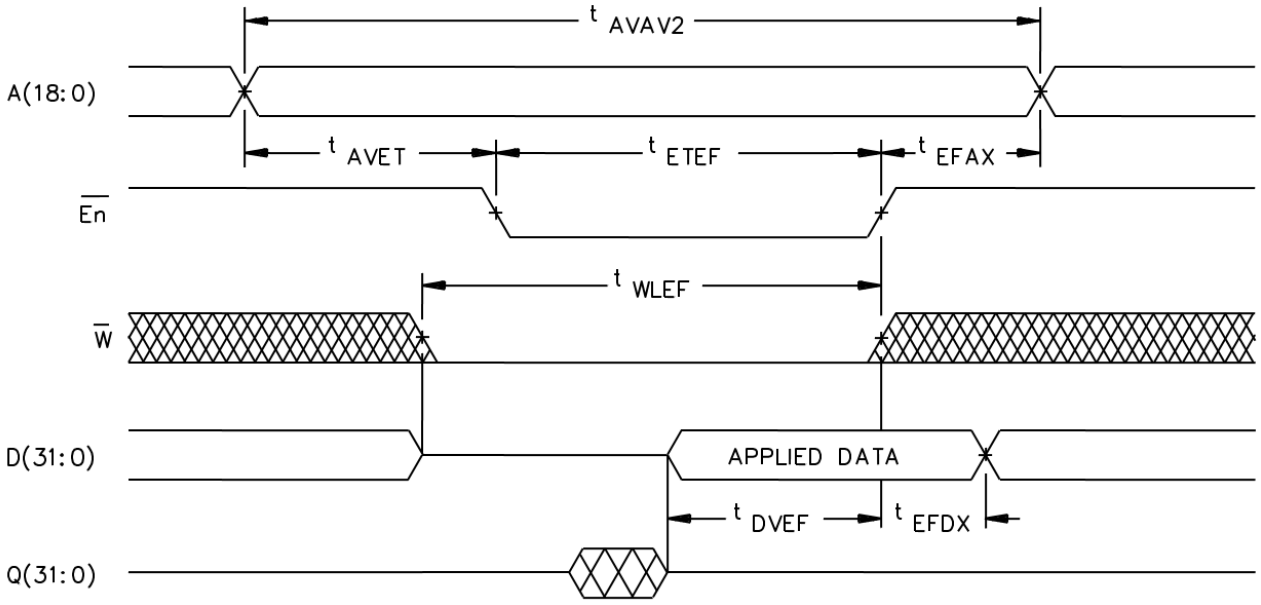


Notes:

1. $\overline{G} \leq V_{IL}$(max) [If $\overline{G} \geq V_{IH}$(min) then Q(31:0) and MBE will be three-state for the entire cycle]
2. $\overline{SCRUB} \geq V_{OH}$(min)

SRAM write cycle 1: $\overline{W}$-controlled Access

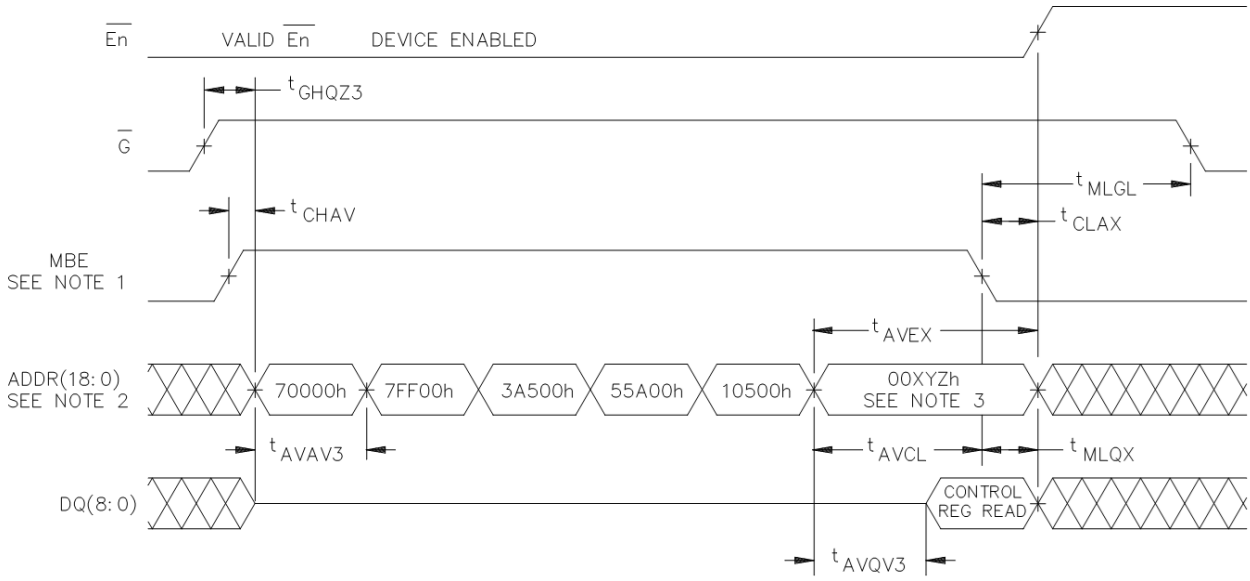
FIGURE 5. Timing waveforms – Continued.



Notes:
1. $\overline{G} \leq V_{IL}$ (max) [If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be three-state for the entire cycle]
2. $\overline{SCRUB} \geq V_{OH}$ (min)

SRAM write cycle 2: Enabled-Controlled Access

FIGURE 5. Timing waveforms – Continued.

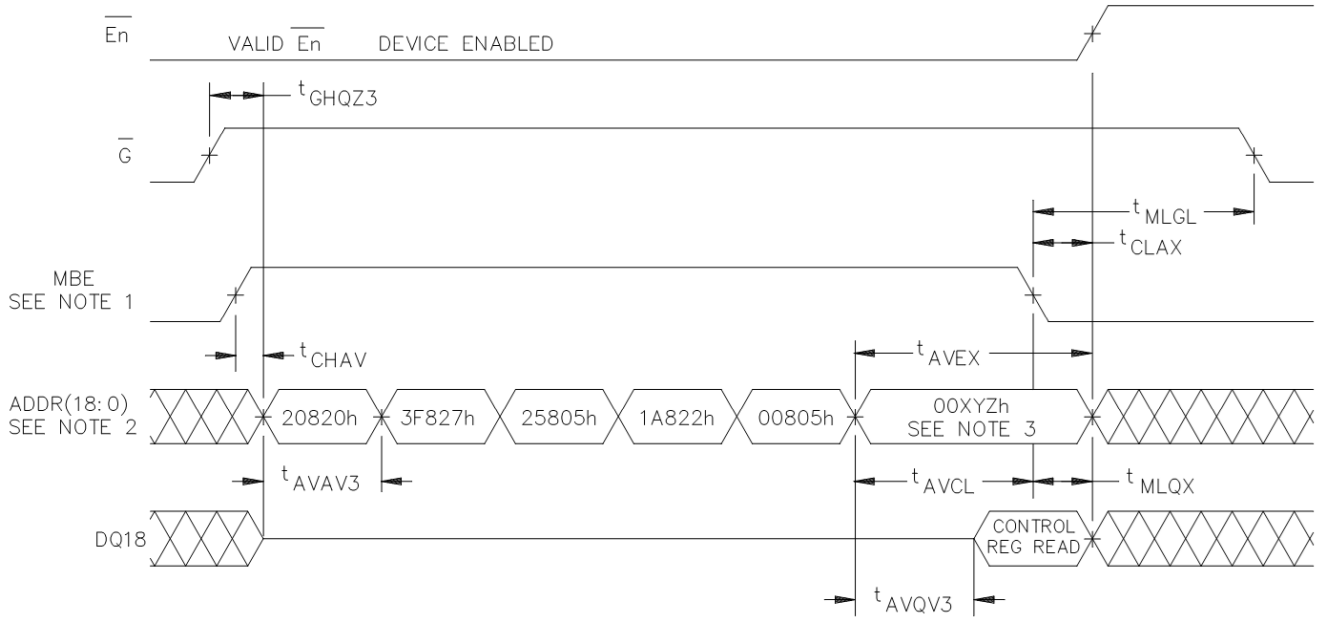


Notes:

1. MBE is driven high by the user.
2. An address transition to 70000h must occur coincident with, or subsequent to, MBE assertion.
3. Lower 10 bits of the last address are used to read or configure the control register.
4. $\overline{\text{SCRUB}} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{\text{SCRUB}}$ during configuration cycle.

EDAC Control register cycle (Odd die numbers)

FIGURE 5. Timing waveforms – Continued.

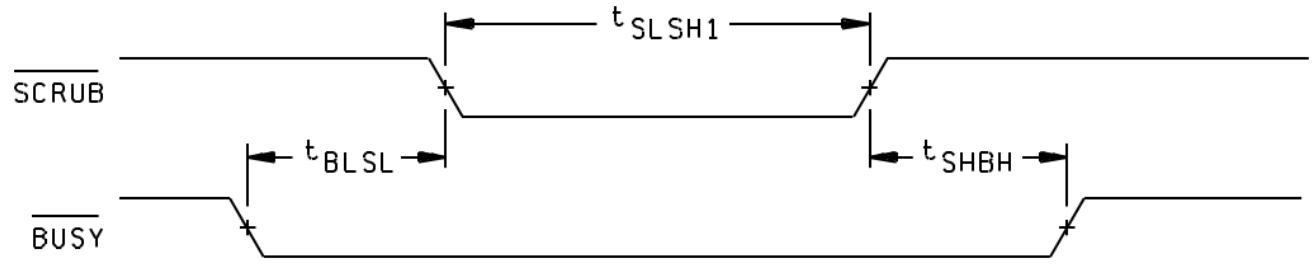


Notes:

1. MBE is driven high by the user.
2. An address transition to 20820h must occur coincident with, or subsequent to, MBE assertion.
3. Bits A2 and A1 are used to read or configure the control register.
4. $\overline{\text{SCRUB}} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{\text{SCRUB}}$ during configuration cycle.

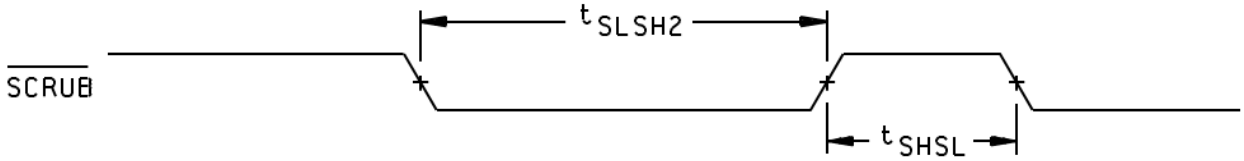
EDAC Control register cycle (Even die numbers)

FIGURE 5. Timing waveforms – Continued.



Note: The conditions pertain to both Read or Write.

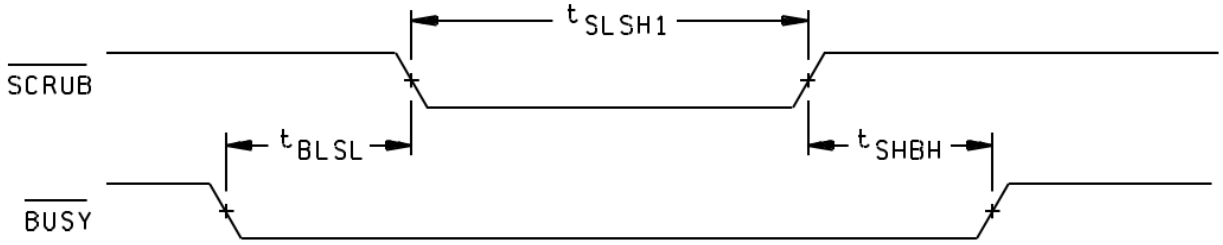
Master mode SCRUB cycle



Note: The conditions pertain to both Read or Write.

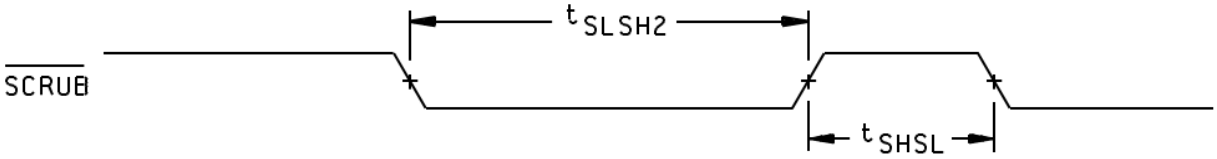
Slave mode SCRUB cycle

FIGURE 5. Timing waveforms – Continued.



Note: The conditions pertain to both Read or Write.

Master mode SCRUB cycle

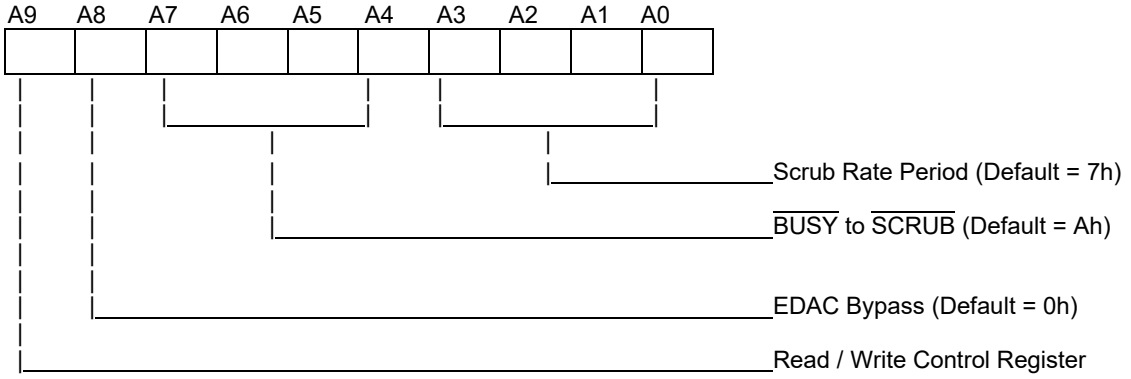


Note: The conditions pertain to both Read or Write.

Slave mode SCRUB cycle

FIGURE 5. Timing waveforms – Continued.

$\overline{E1}$ and $\overline{E3}$ Chip Enabled EDAC Control Register



$\overline{E1}$ and $\overline{E3}$ Chip Enabled EDAC Programming Configuration Table

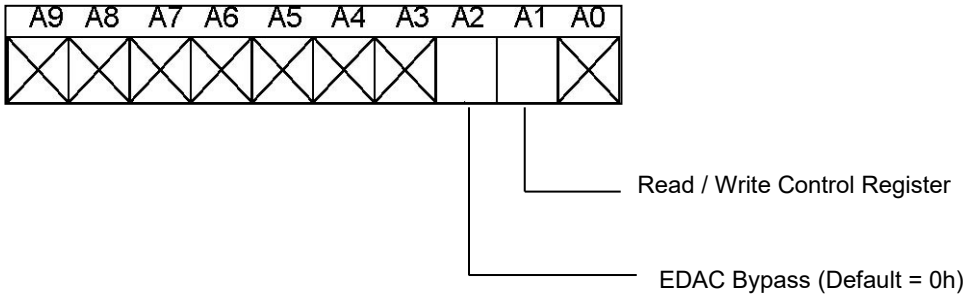
ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 – 3)	Scrub Rate Period [1, 2, 3]	3 – 15 Note: 0 -2 reserved	As SCRUB rate changes from 0 – 15, then the interval between SCRUB cycles will change as follows: 3 = 0.6 µs 8 = 13.0 µs 12 = 205 µs 4 = 1.0 µs 9 = 25.8 µs 13 = 410 µs (see note 4) 5 = 1.8 µs 10 = 51.4 µs 14 = 819 µs (see note 4) 6 = 3.4 µs 11 = 102.6 µs 15 = 1.64 ms (see note 4) 7 = 6.6 µs
A (4 – 7)	$\overline{BUSY}$ to $\overline{SCRUB}$ [2, 3, 5]	0 - 15	If $\overline{BUSY}$ changes from 0 – 15, then the interval t_{BLSL} between $\overline{SCRUB}$ and BUSY will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250 ns
A (8)	Bypass EDAC Bit [6]	0, 1	If 0, then normal EDAC operation will occur If 1, then EDAC will be bypassed
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

Notes:

1. Default Scrub Rate Period is 6.6 µs.
2. Values based on minimum specification limits. For guaranteed ranges of Scrub Rate Period (t_{SCRT}) and $\overline{BUSY}$ to $\overline{SCRUB}$ t_{BLSL} reference the Master mode AC characteristic tables.
3. Scrub Rate Period and $\overline{BUSY}$ to $\overline{SCRUB}$, applicable to master device types 01, 03, and 05, $\overline{E1}$ chip enable only.
4. Period below test capability.
5. The default for t_{BLSL} is 500 ns.
6. The default state for A8 is 0.

FIGURE 6. EDAC Configuration.

$\overline{E2}$ and $\overline{E4}$ Chip Enabled EDAC Control Register



Notes:
X = Not applicable for even die.
See table below for Control Register Definitions

E2 and E4 Chip Enable EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (2)	Bypass EDAC Bit, 1/	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed and no memory scrubbing will occur.
A (1)	Read / Write Control Register	0, 1	0 = A2 will be written to the control register 1 = Control register will be asserted to the data bus DQ18

Notes:

1/ The default state for A2 is 0.

FIGURE 6. EDAC Configuration – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 03 and 04.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883.

(2) 100% PIND (Single pass).

(3) Serialization.

(4) 100% X-ray (Top view only).

(5) Group A.

(6) Dynamic burn-in, deltas, PDA (3%) for Functional Test only, and PDA (10%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	- - -	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	- - -	1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

Table IIB. Delta limits at +25ºC.

Parameter 1/	Limit	Unit
Supply current standby at 0 MHz I_{DD2}	± 10% of specified value in Table IA	mA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º ≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature ±10ºC for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

APPENDIX A
Appendix A forms a part of SMD 5962-10203

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-03-14

Approved sources of supply for SMD 5962-10203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1020301QXC	65342	UT8ER2M32M-22XFC
5962R1020301VXC	65342	UT8ER2M32M-22XFC
5962R1020302QXC	65342	UT8ER2M32S-22XFC
5962R1020302VXC	65342	UT8ER2M32S-22XFC
5962R1020303QXC	65342	UT8ER2M32M-22XFC
5962R1020304QXC	65342	UT8ER2M32S-22XFC
5962R1020305QXC	65342	UT8ER2M32M-22FC
5962R1020305VXC	65342	UT8ER2M32M-22FC
5962R1020306QXC	65342	UT8ER2M32S-22FC
5962R1020306VXC	65342	UT8ER2M32S-22FC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Frontgrade Colorado Springs LLC 4350 Centennial Blvd. Colorado Springs, CO 80907-7370