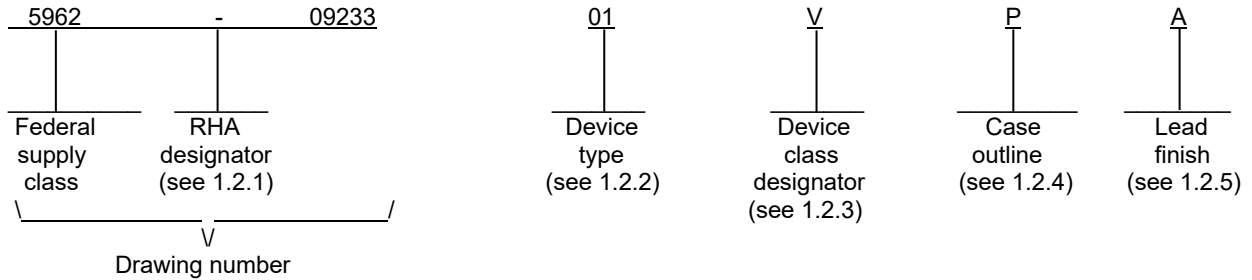




1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	UC19432	Adjustable analog controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. <sup>1/</sup>

Supply voltage (VCC) .....	24 V
Collector regulated output voltage (V <sub>COLL</sub> ) .....	24 V
Non-inverting input to error amplifier (+EA) .....	6 V
Inverting input to error amplifier input (SENSE) .....	6 V
Error amplifier compensation (COMP) .....	6 V
Reference output (REF) .....	6 V
Output sink current of COLL pin (continuous or time average) (I <sub>COLL</sub> ) .....	125 mA
Output source current of ISET pin (continuous or time average) (ISET) .....	-125 mA
Power dissipation (PD) at T <sub>A</sub> ≤ 25°C .....	1 W <sup>2/</sup>
Storage temperature range .....	-65°C to +150°C
Junction temperature (T <sub>J</sub> ) .....	-55°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ) .....	125°C/W

1.4 Recommended operating conditions.

Supply voltage (VCC) .....	2.4 V to 24 V
Ambient operating temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<sup>2/</sup> Derate 8 mW/°C for T<sub>A</sub> > 25°C.

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference voltage tolerance	V <sub>T</sub>	V <sub>COLL</sub> = 5 V, T <sub>A</sub> = +25°C	1	01	1.295	1.305	V
Reference temperature tolerance	V <sub>TT</sub>	V <sub>COLL</sub> = 5 V	1,2,3	01	1.291	1.309	V
Reference line regulation	V <sub>LN</sub>	V <sub>CC</sub> = 2.4 V to 24 V, V <sub>COLL</sub> = 5 V	1,2,3	01		38	mV
Reference load regulation	V <sub>LD</sub>	I <sub>COLL</sub> = 10 mA to 50 mA, V <sub>COLL</sub> = 5 V	1,2,3	01		38	mV
Reference sink current	I <sub>SK</sub>		1,2,3	01	10		μA
Reference source current	I <sub>SC</sub>		1,2,3	01		-10	μA
Error amplifier (EA) input bias current	I <sub>IB</sub>		1,2,3	01	-0.5		μA
Error amplifier (EA) input offset voltage	V <sub>OS</sub>		1,2,3	01	-4	4	mV
Non-inverting input to the error amplifier (+EA) operational voltage limitations	V <sub>+EA</sub>		1,2,3	01	0.9	1.6	V
Error amplifier (EA) output current sink (internally limited)	I <sub>OSK</sub>		1,2,3	01	16		μA
Error amplifier (EA) output current source	I <sub>OS</sub>		1,2,3	01		-0.8	mA
Minimum operating current	I <sub>CC</sub>	V <sub>CC</sub> = 24 V, V <sub>COLL</sub> = 5 V	1,2,3	01		0.8	mA
Collector current limit <sup>2/</sup>	I <sub>L</sub>	V <sub>COLL</sub> = V <sub>CC</sub> = 24 V, Ref = 1.3 V, I <sub>SET</sub> = GND	1,2,3	01		155	mA
Collector saturation voltage	V <sub>SAT</sub>	I <sub>COLL</sub> = 20 mA	1,2,3	01	0.7	1.5	V
Transconductance <sup>2/ 3/</sup>	g <sub>m</sub>	V <sub>CC</sub> = 2.4 V to 24 V, V <sub>COLL</sub> = 3 V, I <sub>SET</sub> = GND	4,5,6	01	-170	-110	mS
Error amplifier open loop voltage gain	A <sub>VOL</sub>		4,5,6	01	60		dB
Error amplifier gain bandwidth	GBW		4,5,6,	01	1.5		MHz

<sup>1/</sup> Unless otherwise specified, T<sub>A</sub> = T<sub>J</sub>, V<sub>CC</sub> = 15 V, COLL pin output = 2.4 V to 24 V, and I<sub>COLL</sub> = 10 mA.

<sup>2/</sup> Programmed transconductance and collector current limit equations are specified in the I<sub>SET</sub> pin description.

<sup>3/</sup> Measured as ΔI<sub>COLL</sub> / ΔV<sub>COMP</sub> for I<sub>COLL</sub> = 5 mA to 20 mA.

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Device type	01	
Case outline	P	
Terminal number	Terminal symbol	Description
1	COLL	The collector of the output transistor with a maximum voltage of 24 V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is $(g_m \times R_L)$ , where $g_m$ is designed to be $-140 \text{ mS} \pm 30 \text{ mS}$ and $R_L$ represents the output load.
2	COMP	The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2 V.
3	VCC	The power connection for the device. The minimum to maximum operating voltage is 2.4 V to 24 V. The quiescent current is usually 0.5 mA.
4	+EA	The non-inverting input to the error amplifier.
5	REF	The output of the trimmed precision reference. It can source or sink $10 \mu\text{A}$ and still maintain less than $\pm 1\%$ output variation.
6	SENSE	The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3 V on chip reference. The SENSE pin is also used as the under voltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1 V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier.  To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole. The error amplifier must slew 2 V to drive the transconductance amplifier initially on.
7	GND	The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.
8	ISET	The current set pin for the transconductance amplifier. The transconductance will be $-140 \text{ mS}$ as specified in the electrical table if this pin is grounded. If a resistance, $R_L$ , is added to the ISET pin, the resulting new transconductance ( $g_m$ ) is calculated using equation :  $g_m = -0.714 / ( 5.1 \Omega + R_L ).$  The maximum current will be approximated by using equation:  $I_{MAX} = 0.65 \text{ V} / ( 5.1 \Omega + R_L ).$

FIGURE 1. Terminal connections.

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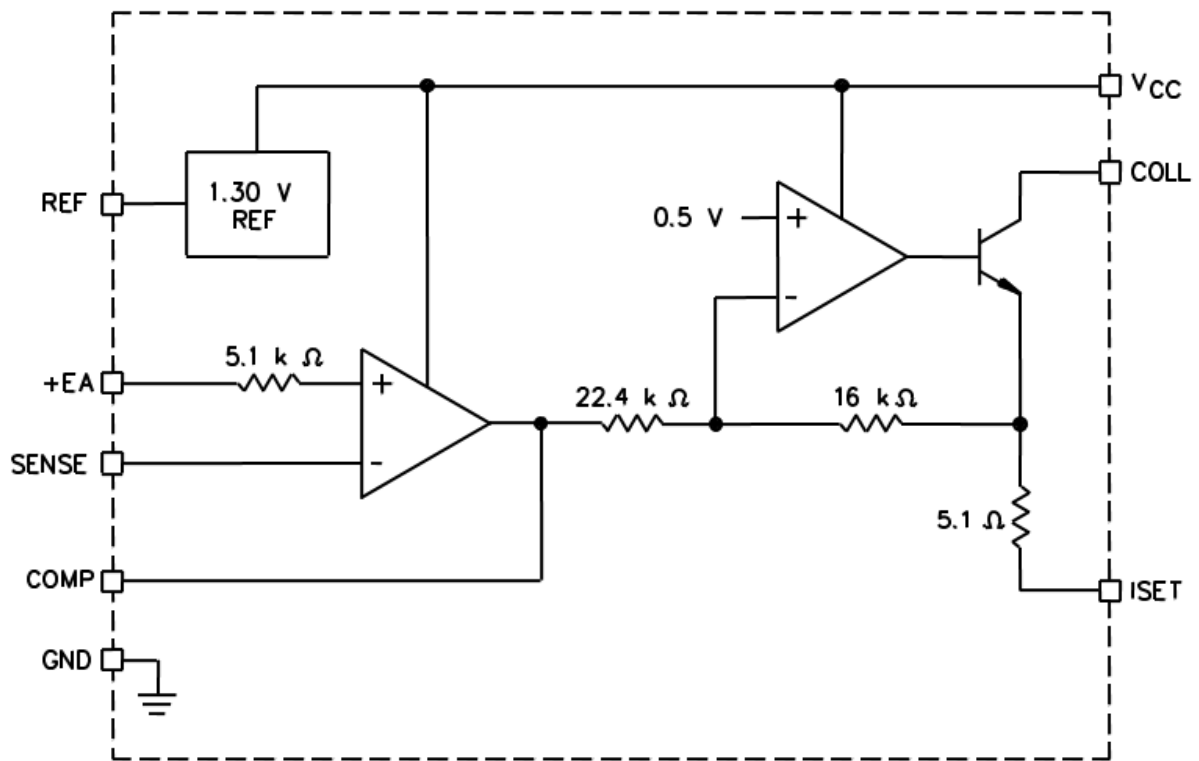


FIGURE 2. Block diagram.

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#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

##### 4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

##### 4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

##### 4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 <u>1/</u>	1,2,3, <u>1/</u> <u>2/</u> 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3, <u>2/</u> 4,5,6
Group D end-point electrical parameters (see 4.4)	1,4	1,4
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. TA = +25°C. 1/

Parameters	Symbol	Delta limits
Minimum operating current	ICC	±0.05 mA
Error amplifier (EA) input offset voltage	VOS	±0.4 mV
Error amplifier (EA) input bias current	IIB	±0.02 µA

1/ Deltas are performed at room temperature.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at TA = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-06-23

Approved sources of supply for SMD 5962-09233 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0923301VPA	01295	UC19432-SP

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln.  
PO Box 660199  
Dallas, TX 75243

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