

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Removed all Class M references and updated boilerplate to current MIL-PRF-38535 requirements. Revised Table IA: added checkerboard pattern to I _{DD4} , added "(WP only)" to I _{IH} , removed I _{IL} . Added "Optional" to line 3 of Table IIA. - lhl	13-10-21	Charles F. Saffle

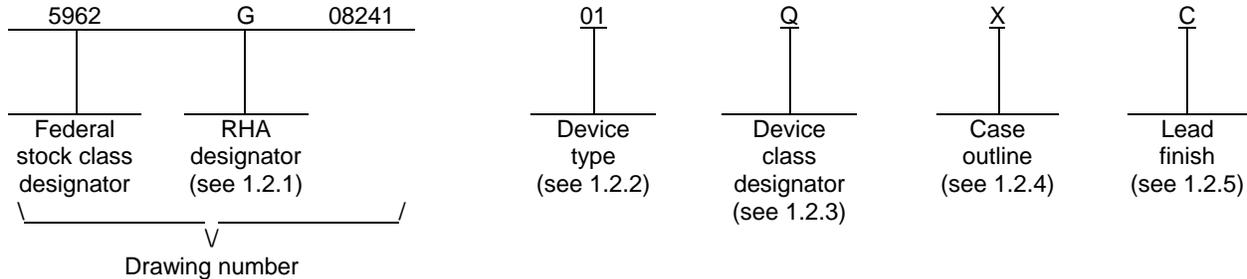
REV																				
SHEET																				
REV	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20														
REV STATUS OF SHEETS	REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Kenneth Rice	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Rajesh Pithadia																			
	APPROVED BY Charles F. Saffle	<p align="center">MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K X 8, 3.3 VOLT, RADIATION HARDENED, Nonvolatile RANDOM ACCESS MEMORY (NVRAM), MONOLITHIC SILICON</p>																		
	DRAWING APPROVAL DATE 10-09-17																			
	REVISION LEVEL A		<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-08241</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-08241														
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access Time</u>	<u>Endurance</u>
01	8406746-155	512K X 8, 3.3 Volt, Radiation Hardened, NVRAM (requires external ECC),	1000 ns	1 x 10 ⁵ cycles
02	8406746-154 1/	512K X 8, 3.3 Volt, Radiation Hardened, NVRAM (requires external ECC),	1000 ns	1 x 10 ⁵ cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	40	Ceramic flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Device type 02 is device type 01 with additional testing (see 4.2.2.d).

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1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V _{DD})	-0.5 V dc to +4.12 V dc
Programming voltage range (V _{PP}).....	-0.5 V dc to +4.12 V dc
DC input voltage range (V _{IN})	-0.5 V dc to V _{DD} + 0.5 V dc 4/
DC output voltage range (V _{OUT})	-0.5 V dc to V _{DD} + 0.5 V dc 4/
Storage temperature range	-65°C to +150°C
Case operating free-air temperature range, (T _C)	-40°C to +110°C
Lead temperature (soldering 5 seconds)	+250°C
Thermal resistance, junction to case (Θ _{JC})	2.9 °C/W
Maximum power dissipation	0.05 W @ 1MHz 5/
Maximum junction temperature (T _J)	140°C
Data retention:	
T _C = 90°C	0.1 years
T _C = 85°C	0.3 years
T _C = 80°C	0.9 years
T _C = 75°C	3.1 years
T _C = 70°C	11.6 years
Write cycle endurance	1 x 10 ⁵ cycles 6/

1.4 Recommended operating conditions. 3/ 4/ 7/

Supply voltage range (V _{DD})	2.97 V dc to 3.63 V dc
Programming voltage range (V _{PP}).....	2.97 V dc to 3.63 V dc
Supply voltage reference (GND)	0.0 V dc
High level input voltage range (V _{IH})	2.0 V to V _{DD}
Low level input voltage range (V _{IL})	0.0 V dc to 0.80 V dc
Case operating free-air temperature range (T _C)	-40°C to +110°C

1.5 Radiation features

Maximum total dose available (dose rate = 50 - 300 rads(Si)/s)	≥ 500 krad (Si)
Single event phenomenon (SEP) effective linear energy threshold (LET) with no latchup (SEL) (see 4.4.4.4)	≥ 120 MeV-cm ² /mg 8/
Single event upset (SEU)	≤ 1 x 10 ⁻¹¹ upsets/bit-day 8/
Neutron irradiation	1 x 10 ¹³ neutrons/cm ² 8/
Dose rate upset	≥ 1 x 10 ¹² rad(Si)/sec 8/
Dose rate survivability (RS).....	≥ 1 x 10 ¹² rad(Si)/sec 8/

- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum or minimum levels may degrade performance and affect reliability.
- 3/ All voltages are referenced to GND.
- 4/ Maximum applied voltage shall not exceed +4.12 V.
- 5/ Guaranteed by design; not tested.
- 6/ Endurance assumes a 50% write "1"s and 50% write "0"s.
- 7/ Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents.
- a. Power-up sequence: GND, V_{DD}, Inputs, V_{PP}.
 - b. Power-down sequence: V_{PP}, Inputs, V_{DD}, GND.
- 8/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract. Users needing additional radiation information should contact the supplier for the detailed radiation report.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; <http://www.astm.org>.)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC JESD78 - IC Latch-Up Test.
 JEDEC JESD22-A117 - Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test.
 JEDEC JESD47 - Stress-Test-Driven Qualification of Integrated Circuits.

(Applications for copies should be addressed to the JEDEC Solid State Technology Association 2011, 3103 North 10th Street, Suite 240 South, Arlington, VA 22201-2107; <http://www.jedec.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Timing waveforms. The read and write cycle timing waveforms shall be as specified on figure 4.

3.2.5 Irradiation bias circuit for total dose. The irradiation bias circuit for total dose shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Functional tests. Various functional tests used to test this device are contained in the appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Write cycle endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 here in over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data. Testing may be done per JESD22-A117 and JESD47.

3.9 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data. Testing may be done per JESD22-A117 and JESD47.

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3.10 Write protection. A write protection test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the operation in PROM mode. The methods and procedures may be vendor specific, but shall guarantee that when V_{PP} is 0 V and / or the write protect signal is low, the memory is disabled for write operations while maintaining the read operation availability over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Test Conditions -40°C ≤ T _C ≤ +110°C 2.97 V ≤ V _{DD} ≤ 3.63 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Supply Current (cycling selected)	I _{DD1}	F = Fmax 3/ CS = V _{IL} = GND No output load, checkerboard pattern, access = read	All	1, 2, 3		75	mA
		F = Fmax 3/ CS = V _{IL} = GND No output load, checkerboard pattern, access = write	All	1, 2, 3		35	mA
Supply Current (cycling de-selected)	I _{DD2}	F = Fmax 3/ CS = V _{IH} = V _{DD}	All	1, 2, 3		25	mA
Supply Current (Standby)	I _{DD3}	F = 0 MHz, CS = V _{IH} = V _{DD}	All	1, 2, 3		25	mA
Programming Current (cycling selected)	I _{DD4}	F = Fmax 3/ CS = V _{IL} = GND No output load, checkerboard pattern, access = write	All	1, 2, 3		15	mA
Low level output voltage	V _{OL}	I _{OL} = 4 mA	All	1, 2, 3		0.4	V
		I _{OL} = 200 μA				0.1	
High level output voltage	V _{OH}	I _{OH} = -4 mA	All	1, 2, 3	2.4		V
		I _{OH} = -200 μA			V _{DD} - 0.1V		
High level input voltage	V _{IH}		All	1, 2, 3	2.0		V
Low level input voltage	V _{IL}		All	1, 2, 3		0.8	V
Input leakage current	I _{ILK}	0 V ≤ V _{IN} ≤ 3.63 V	All	1, 2, 3	-10	10	μA
Output leakage current	I _{OLK}	0 V ≤ V _{OUT} ≤ 3.63 V	All	1, 2, 3	-10	10	μA
Input capacitance	C _{IN}	See 4.4.1e	All	4		10	pF
Output capacitance	C _{OUT}		All	4		10	pF
Functional tests		See 4.4.1.c	All	7, 8A, 8B			
Input pull down current	I _{IH}	V _{PIN} = V _{DD} (WP only)	All	1, 2, 3		2.0	mA

See footnotes at the end of the table.

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TABLE IA. Electrical performance characteristics - continued. 1/2/

Test	Symbol	Test Conditions -40°C ≤ T _C ≤ +110°C 2.97 V ≤ V _{DD} ≤ 3.63 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Read Cycle AC Specifications <u>4/</u>							
Read cycle time	t _{AVAV}		All	9, 10, 11	100		ns
Address access time	t _{AVQV}		All	9, 10, 11		70	ns
Chip select access time	t _{SLQV}		All	9, 10, 11		80	ns
Output enable access time	t _{GLQV}		All	9, 10, 11		12	ns
Chip select to output active	t _{SLQX}		All	9, 10, 11	5		ns
Output enable to output active	t _{GLQX}		All	9, 10, 11	0		ns
Output hold after address change	t _{AXQX}		All	9, 10, 11	2		ns
Chip select to output disable	t _{SHQZ}		All	9, 10, 11		10	ns
Output enable to output disable	t _{GHQZ}		All	9, 10, 11		10	ns
Write Latency <u>5/</u>		The delay required prior to reading an address after writing to that same address.	All	9, 10, 11	10		ms
Write Cycle AC Specifications							
Write cycle time	t _{AVAV}		All	9, 10, 11	1000		ns
Address setup to end of write	t _{AVWH}		All	9, 10, 11	855		ns
Chip select to end of write	t _{SLWH}		All	9, 10, 11	860		ns
Write pulse width access time	t _{WLWH}		All	9, 10, 11	850		ns
Data-in setup time	t _{WDS}		All	9, 10, 11	5		ns
Data hold after end of write	t _{SHDX}		All	9, 10, 11	5		ns
Address setup to start of write	t _{AVWL}		All	9, 10, 11	5		ns
Address hold after end of write	t _{SHAX}		All	9, 10, 11	5		ns
Write disable pulse width	t _{WHWL}		All	9, 10, 11	10		ns

See footnotes at the end of the table.

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TABLE IA. Electrical performance characteristics - continued.

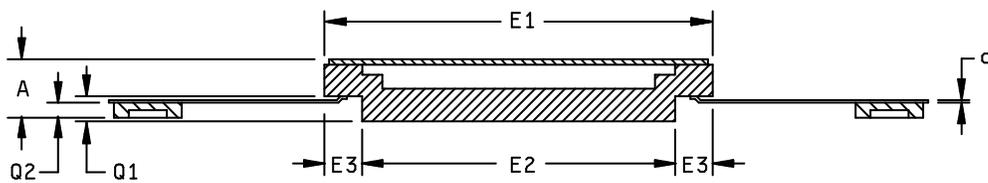
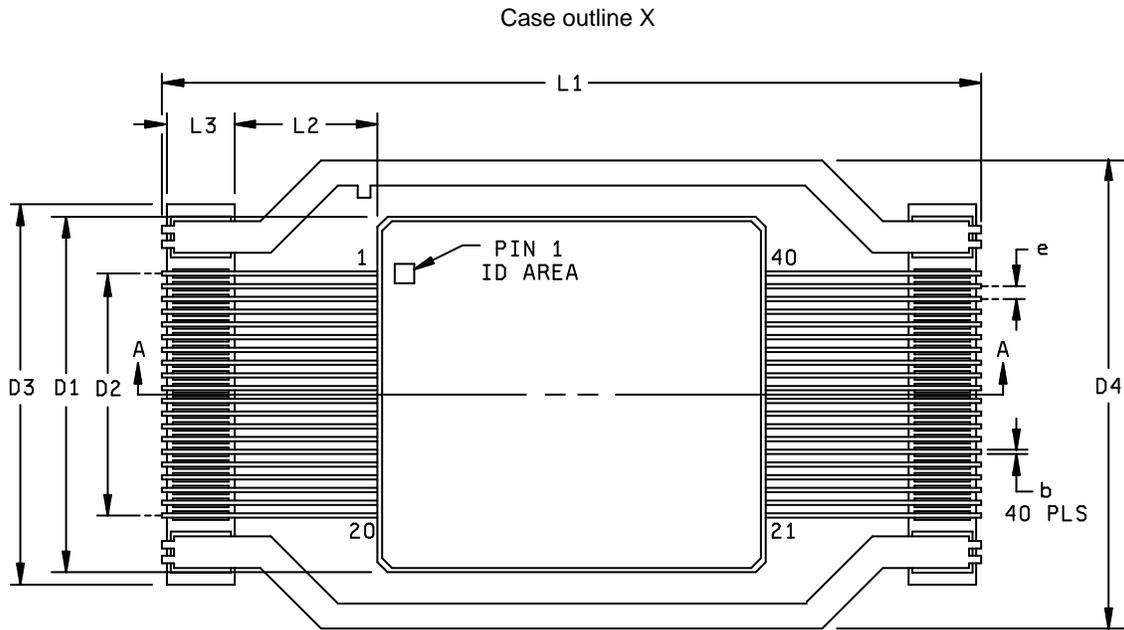
- 1/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F and G of irradiation. However, this device is only tested at the "G" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25^\circ\text{C}$.
- 2/ Test conditions are defined at inception of test. The device is first stabilized at the desired temperature in an unpowered state to ensure that the module is at the desired case temperature (T_{case}) before parameters are measured. The case temperature (T_{case}) is maintained during testing at the specified temperature by a forced air test environment.
 Test conditions for AC measurements are listed below.
 Input Levels: 0 V to V_{DD}
 Input rise and fall time: < 2.0 ns/Volt
 Input and output timing reference levels (except for tristate parameters): 1.5 V
 Input and output timing reference levels for tristate parameters: $V_{\text{OL}} = 1.23 \text{ V}$, $V_{\text{OH}} = 2.23 \text{ V}$
 Read Cycle timing diagram is shown in Figure 4.
 Write Cycle timing diagram is shown in Figure 4.
- 3/ $F_{\text{max}} = 1 / t_{\text{AVAV}(\text{min})}$. Also, the value of F_{MAX} is different for read vs. write accesses.
- 4/ The worst case timing sequence of $t_{\text{WLWH}} + t_{\text{WHWL}} = t_{\text{AVAV}}$ (write cycle time).
- 5/ This applies only to this specific address, reading and/or writing to other addresses during this period is permitted assuming the specified latency is observed for each written address.

TABLE IB. SEP test limits. 1/ 2/

Device type	$T_A =$ Temperature $\pm 10^\circ\text{C}$	Memory pattern	$V_{\text{DD}} = 2.97 \text{ V}$		Bias for latch-up test $V_{\text{DD}} = 3.63 \text{ V}$ no latch-up LET = 5/ 6/
			SER CRÈME 96 Solar Min environment	Maximum device cross section (LET = 120 MeV- cm^2/mg)	
All	+25°C	3/	$\leq 1 \times 10^{-11}$ upsets/bit-day 4/	$4.3 \times 10^{-11} \text{ cm}^2/\text{bit}$	$\geq 120 \text{ MeV}\cdot\text{cm}^2/\text{mg}$

- 1/ For SEP test conditions, see 4.4.4.4 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
- 4/ CRÈME 96 with Weibull parameters. Calculation performed assuming 35000km CREME96 Solar Minimum Heavy Ion Spectrum with 0.100 inch of aluminum shielding with an absorption depth of 2 μm . Testing performed to ASTM Standard F1192.
- 5/ Worst case temperature is $T_A = +110^\circ\text{C}$.
- 6/ Tested to an LET of $\geq 120 \text{ MeV}/(\text{cm}^2/\text{mg})$, with no latch-up (SEL).

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SECTION A-A

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	3.40	3.80	E1	19.44	19.94
b	.15	.25	E2	15.88	16.38
c	.112	.175	E3	1.58	1.98
D1	16.26	16.76	L1	41.53 REF	
D2	11.87	12.27	L2	7.24 REF	
D3	19.10	19.50	L3	3.3	3.56
D4	23.25	24.25	Q1	1.07	1.47
e	.535	.735	Q2	.76 REF	

- Notes: 1. Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface.
 2. Terminal identification numbers need not appear on the package.

FIGURE 1. Case outline.

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Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	DQ4
2	GND
3	VDD
4	DQ6
5	AREF <u>1/</u>
6	A7
7	A6
8	A5
9	A4
10	$\overline{\text{OE}}$
11	$\overline{\text{WE}}$
12	A8
13	A9
14	A10
15	A13
16	A14
17	DQ2
18	VPP <u>2/</u>
19	GND
20	DQ0
21	DQ1
22	GND
23	VDD
24	DQ3
25	A15
26	A18
27	A11
28	A12
29	A17
30	A16
31	CS
32	A0
33	A1
34	A2
35	A3
36	$\overline{\text{WP}}$
37	DQ7
38	VDD
39	GND
40	DQ5

Notes:

1/ AREF = should be tied to GND.

2/ VPP = Programming Power Supply. Tied to GND (post-programming) for Read Only applications.

FIGURE 2. Terminal connections.

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Truth Table when $V_{PP} = V_{DD}$

Mode	Inputs <u>1/</u> , <u>2/</u>					Power
	\overline{CS}	\overline{WE}	\overline{OE}	\overline{WP}	I/O	
WRITE	LOW	LOW	X	<u>4/</u>	DATA-IN	ACTIVE
READ	LOW	HIGH	LOW	<u>4/</u>	DATA-OUT	ACTIVE
STANDBY <u>3/</u>	HIGH	X	X	X	HIGH-Z	STANDBY

Truth Table when $V_{PP} = 0\text{ V}$

Mode	Inputs <u>1/</u> , <u>2/</u>					Power
	\overline{CS}	\overline{WE}	\overline{OE}	\overline{WP}	I/O	
WRITE	Prohibited					
READ	LOW	HIGH	LOW	<u>4/</u>	DATA-OUT	ACTIVE
STANDBY <u>3/</u>	HIGH	X	X	X	HIGH-Z	STANDBY

Notes:

1/ V_{IN} for Don't Care (X) inputs = V_{IL} or V_{IH} .

2/ When $\overline{OE} = \text{HIGH}$, I/O is High-Z.

3/ To dissipate the minimum amount of standby power when in standby mode: $\overline{CS} = V_{DD}$. All other input levels may float.

4/ Not a switching signal. \overline{WP} tied high for NVRAM applications (default). Tied low for "Read Only" applications.

FIGURE 3. Truth tables.

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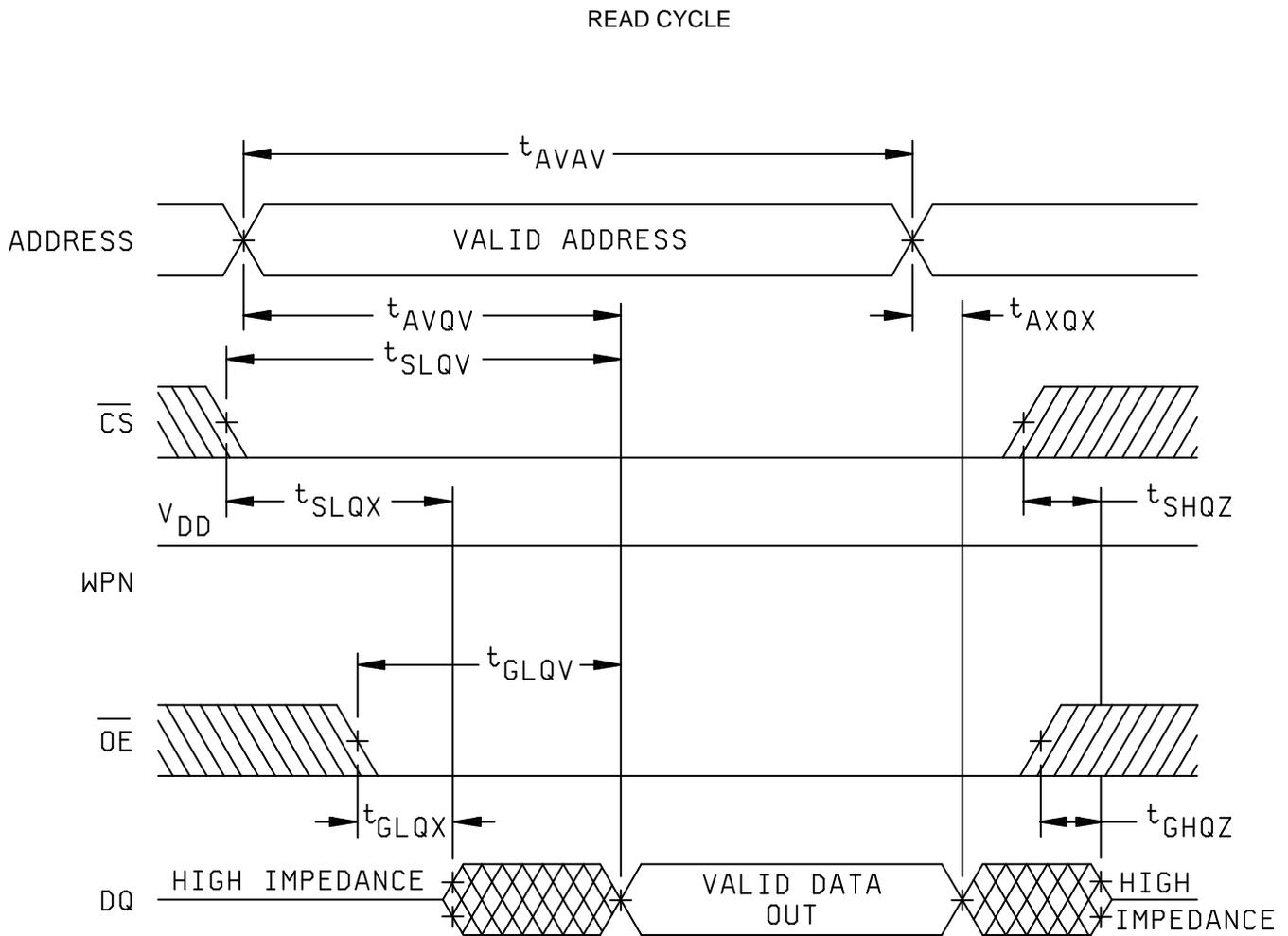


FIGURE 4. Timing waveforms.

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WRITE CYCLE (WE CONTROLLED)

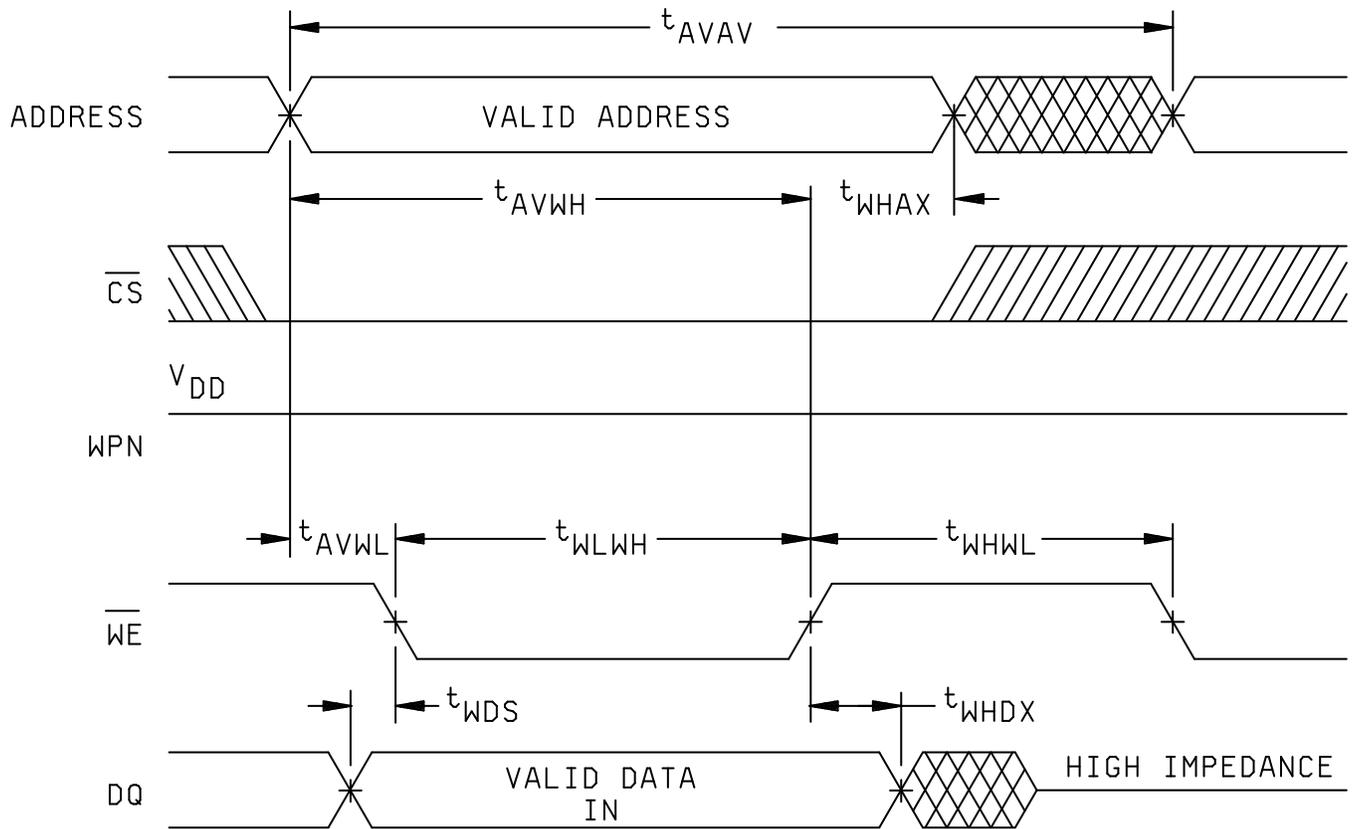


FIGURE 4. Timing waveforms – continued.

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WRITE CYCLE (CS CONTROLLED)

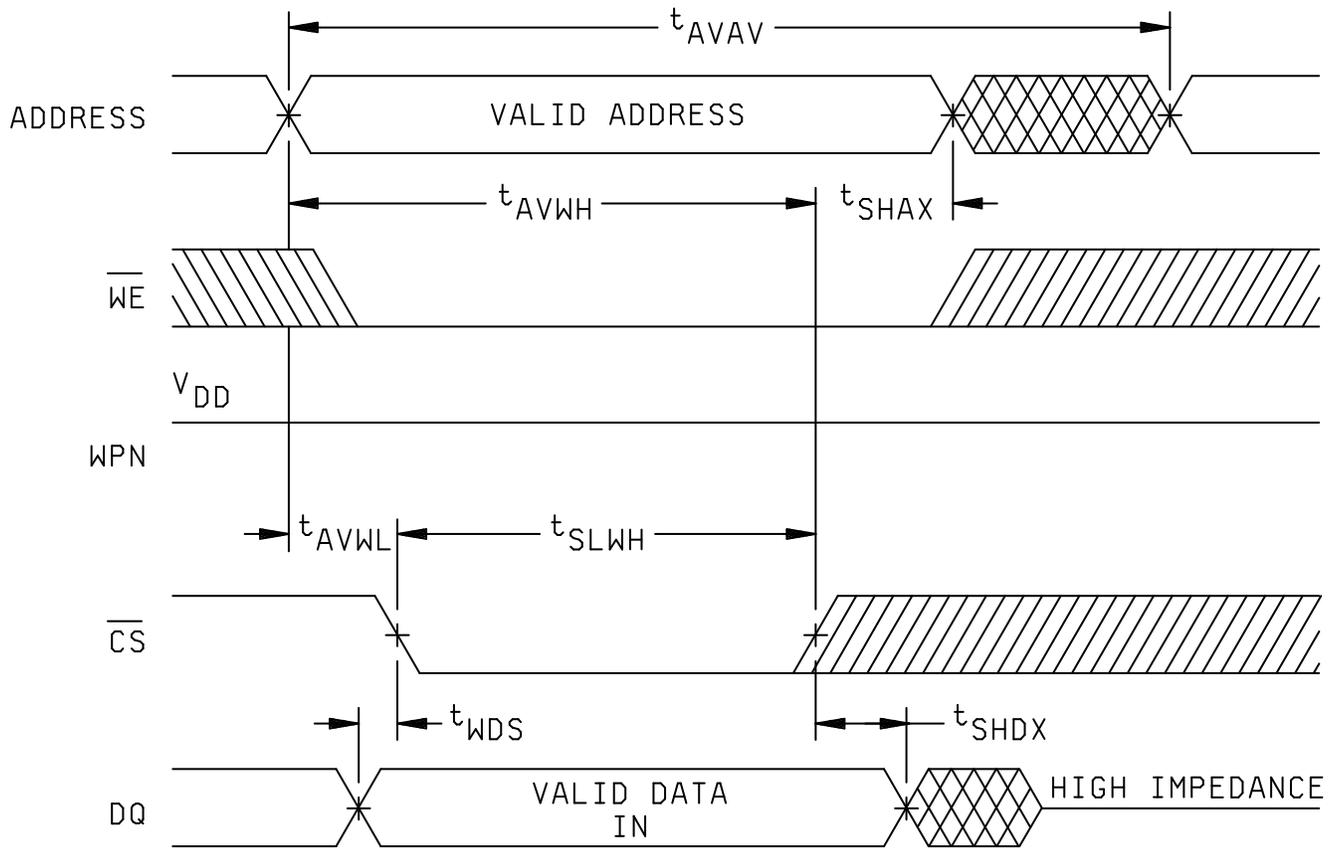


FIGURE 4. Timing waveforms – continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- d. Additional screening for device O2 shall include:
 - (1) 100% X-ray per MIL-STD-883, method 2012
 - (2) Increased burn-in (240 hours) dynamic burn-in
 - (3) Optional interim room temperature electrical test
 - (4) 144 hours static burn-in with tightened class V PDA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. In addition, special test structures may be used for latch-up characterization in place of using product. If test structures are used, testing shall be on five wafers. Information contained in JEDEC JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1*, 7*, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		Optional 1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
6	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter <u>1/</u>	Limits	Units
I _{DD3} (standby)	± 10% of specified value in Table IA or 35 μA whichever is greater <u>2/</u>	mA
I _{ILK}	± 10% of specified value in Table IA or 35 μA whichever is greater <u>2/</u>	μA
I _{OLK}	± 10% of specified value in Table IA or 35 μA whichever is greater <u>2/</u>	μA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ If device is tested at or below 35 μA, no deltas are required.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$. The latchup test temperature shall be at $110^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
- f. Bias conditions shall be V_{DD} maximum = 2.97 V dc for the upset measurements and V_{DD} minimum = 3.63 V dc for the latchup measurements.
- g. For SEP test limits, see table IB herein.

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4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$ after an exposure of 2×10^{12} neutrons/cm² (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Occurrence of latchup (SEP).

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APPENDIX A

Appendix A forms a part of SMD 5962-08241

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 1.4 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.

- Step 1. Increment address from minimum to maximum writing each address with alternating data pattern (x55).
- Step 2. Increment address from minimum to maximum while performing 2a and 2b.
 - Step 2a. Read and verify an address.
 - Step 2b. Write the address with complement data.
- Step 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d.
 - Step 3a. Read and verify an address.
 - Step 3b. Write the address with complement data.
 - Step 3c. Read and verify the address.
 - Step 3d. Write the address with complement data.
- Step 4. Decrement address from maximum to minimum while performing 4a and 4b.
 - Step 4a. Read and verify the address.
 - Step 4b. Write the address with complement data.
- Step 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d.
 - Step 5a. Read and verify the address.
 - Step 5b. Write the address with complement data.
 - Step 5c. Read and verify the address.
 - Step 5d. Write the address with complement data.
- Step 6. Decrement address from maximum to minimum while performing 6a.
 - Step 6a. Read and verify the address.

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APPENDIX A – Continued.

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FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

- Step 1. Write x55 data pattern to all addresses from minimum to maximum.
- Step 2. Read and verify x55 data pattern at all addresses.
- Step 3. Write xAA data pattern to all addresses from minimum to maximum.
- Step 4. Read and verify xAA data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verification.

Each test performed independently.

- NOE Functional test: Read with NOE = VIH and confirm high-Z outputs.
- NCS Functional test: Read with NCS = VIH and verify high-Z outputs.
- NSL Functional test: Read with NSL = VIL and verify high-Z outputs.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-10-21

Approved sources of supply for SMD 5962-08241 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962G0824101QXC	1RU44	8406746-155
5962G0824001VXC	<u>3/</u>	8406746-151
5962G0824102QXC	1RU44	8406746-154

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply. The last known source is listed below.

Vendor CAGE
number

1RU44

Vendor name
and address

BAE Systems
9300 Wellington Road
Manassas, VA 20110-4122

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