

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to meet current MIL-PRF-38535 requirements. – glg	16-06-28	Charles Saffle



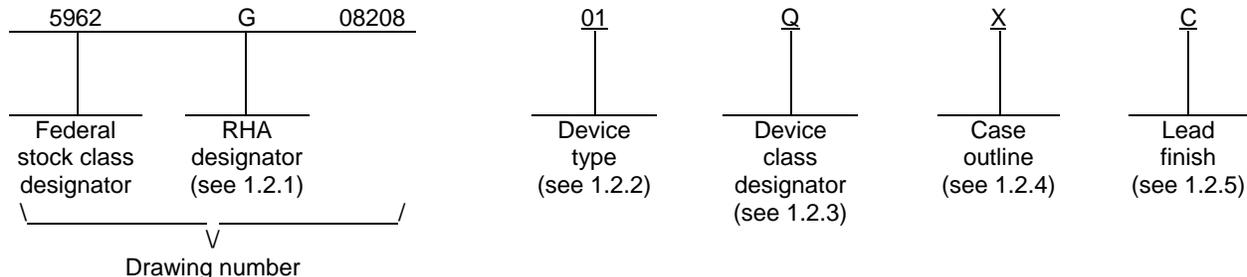
REV																				
SHEET																				
REV	A	A	A	A	A	A	A													
SHEET	15	16	17	18	19	20	21													
REV STATUS OF SHEETS				REV SHEET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
					1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Cheri Rida	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p>MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 1K X 36 CLOCKED FIFO, 3.3 VOLT, RADIATION-HARDENED, MONOLITHIC SILICON</p>																			
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Ken Rice																				
	APPROVED BY Robert M. Heber																				
	DRAWING APPROVAL DATE 08-10-22																				
AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE 67268	5962-08208																	
		SHEET		1 OF 21																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	8407971	1K X 36 Clocked FIFO Rad-Hard

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	132	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.3 V dc to +4.5 V dc
Input voltage range (V_{IN})	-0.3 V dc to $V_{DD} + 0.3$ V dc 3/ 5/
Output voltage range (V_{OUT})	-0.3 V dc to $V_{DD} + 0.3$ V dc 3/ 5/
Storage temperature range (T_A)	-65°C to +150°C
Case operating temperature range (T_C)	-55°C to +125°C
Lead temperature (soldering, 5 seconds)	+250°C
Thermal resistance, junction-to-case (θ_{JC})	3.0°C/W
Maximum power dissipation (P_D)	1.8 W 4/
Maximum junction temperature (T_J)	150°C
5 V tolerant CMOS and TTL (V_{5Vtol}) (V_{DD} applied)	-0.3 V to +5.5 V 5/ 7/
All I/O types (V_{ColdSp}) ($V_{DD} = 0.0$ V, Cold Spare condition)	-0.3 V to +3.63 V 5/ 7/
DC I/O clamp current (I_{IK}) ($V_{IN} < 0.0$ V, $T_J = +125^\circ\text{C}$)	-5.0 mA 6/

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 2

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V _{DD})	+2.97 V dc to +3.63 V dc
Ground voltage (GND)	0.0 V dc
Input logic low voltage (V _{IL})	0.0 V dc to +0.8 V dc
Input logic high voltage (V _{IH})	+2.0 V to V _{DD}
Case operating temperature range (T _c)	-55°C to +125°C
Maximum clock frequency (F _{max})	50 MHz

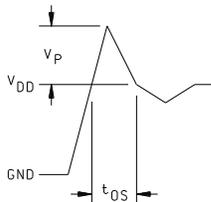
1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012)	99.3 percent
--	--------------

1.6 Radiation features

Maximum total dose available (dose rate = 50-300 rads (Si)/s)	500K Rad (Si) <u>8/</u>
Prompt dose upset/latch-up	1 x 10 ⁹ rad(Si)/sec <u>4/</u>
Dose rate survivability (DRS)	1 x 10 ¹² rad(Si)/sec <u>4/</u>
Single event upset error rate (SER)	1 x 10 ⁻⁹ upsets/bit-day <u>9/</u> <u>4/</u>
Single event phenomenon (SEP):	
No SEL occurs at effective (LET)	> 120 MeV-cm ² /mg <u>4/</u> <u>10/</u>
Neutron irradiation	2 x 10 ¹³ neutrons/cm ² <u>11/</u> <u>4/</u>

- 1/ Stresses at or above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum or minimum levels may degrade performance and affect reliability.
- 2/ All voltages are referenced to GND.
- 3/ Maximum applied voltage shall not exceed + 4.5 V for V_{DD}.
- 4/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.
- 5/ External signals applied to I/O pins assume that drivers are in high impedance state.
- 6/ Clamp current is equivalent to I_{DC} current at V_{IN} < 0 with respect to the module ground leads
- 7/ Overshoot area (V_P x t_{OS}) / 2 ≤ 1.2 V – ns as shown below:



- 8/ Irradiation performed according to MIL-STD-883, method 1019, condition A.
- 9/ 90% worst case particle environment, Geosynchronous orbit, 0.025 inch of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 μm-epi thickness.
- 10/ See Table IB for information on SEP test limits.
- 11/ Testing performed on technology characterization vehicle.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; <http://www.astm.org>.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing waveforms. The read and write cycle waveforms shall be as specified on figure 3.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
4

3.2.4 Irradiation bias circuit for total dose. The irradiation bias circuit for total dose shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
5

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C +2.97 V ≤ V _{DD} ≤ +3.63 V unless otherwise specified	Device types	Group A Subgroups 3/	Limits		Unit
					Min	Max	
Static Supply Current	I _{DDSB} 4/ 5/	-55°C ≤ T _C ≤ +25°C	All	1, 3		0.1	mA
		T _C = +125°C	All	2		3.5	mA
Idle Supply Current	I _{DDI} 6/	f _{CLK} = 50 MHz, T _C = -55°C	All	3		90	mA
		f _{CLK} = 50 MHz, T _C = +25°C to +125°C	All	1, 2		76	mA
Dynamic Current	I _{DDOP} 7/	f _{CLK} = 50 MHz, C _{load} = 50 pf	All	1, 2, 3		360	mA
		f _{CLK} = 50 MHz, C _{load} = 85 pf	All	1, 2, 3		500	mA
Output High Voltage	V _{OH1}	I _{OH1} = -6.0 mA	All	1, 2, 3	2.40		V
Output High Voltage	V _{OH2}	I _{OH2} = -100 μA	All	1, 2, 3	V _{DD} -0.20		V
Output Low Voltage	V _{OL1}	I _{OL1} = 4.0 mA	All	1, 2, 3		0.40	V
Output Low Voltage	V _{OL2}	I _{OL2} = 100 μA	All	1, 2, 3		0.20	V
Input High Voltage	V _{IH}		All	1, 2, 3	2.0		V
Input Low Voltage	V _{IL}			1, 2, 3		0.8	V
Input Leakage Current	I _{IL}	V _{IN} = 0.0 V, V _{DD} = 3.63 V	All	1, 2, 3	-10		μA
Input Leakage Current	I _{IH}	V _{IN} = 3.63 V, V _{DD} = 3.63 V	All	1, 2, 3		10	μA
I/O High Tri-state Current	I _{OZH1}	V _{PIN} = V _{DD} = 3.63 V	All	1, 2, 3	0	10	μA
I/O Low Tri-state Current	I _{OZL1}	V _{PIN} = 0.0 V	All	1, 2, 3	-10		μA
I/O 5 V High Tri-state Current	I _{OZH2}	V _{PIN} = 5.50 V, V _{DD} = 2.97 V	All	1, 2, 3		300	μA
I/O Pin Capacitance	C _{IN} 3/	0 V < V _{IN} ≤ V _{DD}	All	4		10	pF
I/O Pin Capacitance	C _{OUT} 3/		All	4		10	pF
Manufacturing Tests			All	7, 8A, 8B			
AC Performance Tests	8/		All	9, 10, 11	50		MHz

See footnotes at the end of the table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
6

TABLE IA. Electrical performance characteristics - continued. 1/ 2/

Test	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C +2.97 V ≤ V _{DD} ≤ +3.63 V unless otherwise specified	Device types	Group A Subgroups 3/	Limits		Unit
					Min	Max	
Read clock cycle time	t _{CKR}		All	9, 10, 11	13.0		ns
Clock high time	t _{CKH}		All	9, 10, 11	6.0		ns
Clock low time	t _{CKL}		All	9, 10, 11	6.0		ns
Enable setup time	t _{SEN}		All	9, 10, 11	6.0		ns
Enable hold time	t _{HEN}		All	9, 10, 11	1.0		ns
Q hold after CLKRD	t _{QH}		All	9, 10, 11	1.5		ns
Q propagation	t _{QP}	C _{load} = 25 pf	All	9, 10, 11		11.0	ns
		C _{load} = 50 pf	All	9, 10, 11		12.5	ns
		C _{load} = 85 pf	All	9, 10, 11		15.0	ns
Flag hold after CLKRD	t _{FH}		All	9, 10, 11	1.5		ns
Flag propagation	t _{FP}	C _{load} = 25 pf	All	9, 10, 11		8.0	ns
		C _{load} = 50 pf	All	9, 10, 11		10.0	ns
		C _{load} = 85 pf	All	9, 10, 11		12.0	ns
Write clock cycle time	t _{CKW}		All	9, 10, 11	13.0		ns
D setup	t _{SD}		All	9, 10, 11	4.0		ns
D hold	t _{HD}		All	9, 10, 11	1.0		ns
Flag hold after CLKWR	t _{FH}		All	9, 10, 11	1.5		ns
MR pulse width low	t _{PMR}		All	9, 10, 11	2 ClkWr rising edges		
Clock setup to MR	t _{SCMR}		All	9, 10, 11	1.0		ns
MR recovery	t _{MRR}		All	9, 10, 11	2.0		ns
Data hold from MR	t _{QHMR}		All	9, 10, 11	0.0		ns
MR assert to Q low	t _{MRQL}		All	9, 10, 11		18.0	ns
MR high to flags valid	t _{MRF}		All	9, 10, 11		N/A	ns
MR high to data valid	t _{AMR}		All	9, 10, 11		N/A	ns

See footnotes at the end of the table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
7

TABLE IA. Electrical performance characteristics - continued. 1/ 2/

Test	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C +2.97 V ≤ V _{DD} ≤ +3.63 V unless otherwise specified	Device types	Group A Subgroups 3/	Limits		Unit
					Min	Max	
MR exit time after deassert	t _{MRDW}		All	9, 10, 11	2 ClkWr rising edges		
MR exit time after deassert	t _{MRDR}		All	9, 10, 11	2 ClkRd rising edges		
OE to output low Z	t _{QLZ}		All	9, 10, 11	0.0		ns
OE to output high Z	t _{OHZ}		All	9, 10, 11		6.0	ns
OE low to Q valid	t _{OE}	C _{load} = 25 pf	All	9, 10, 11		8.0	ns
		C _{load} = 50 pf	All	9, 10, 11		9.0	ns
		C _{load} = 85 pf	All	9, 10, 11		12.0	ns
CLKWR cycle			All	9, 10, 11	13.0		ns
CLKRD cycle			All	9, 10, 11	13.0		ns
Tskew2 falling edge of opposite clock	t _{SKREW2} 9/		All	9, 10, 11	3.5		ns

- 1/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F, and G of irradiation. However, this device is only tested at the "G" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 2/ At inception of test, the part is first stabilized at the desired temperature in an un-powered state to ensure that the module is at the desired T_C before parameters are measured. The case temperature (T_C) is maintained during testing at the specified temperature by a forced air test environment. Test is performed at -55°C, 25°C, and 125°C to ensure the above performance parameters across the voltage and temperature ranges specified in Section 1.4.
- 3/ Design value validated by characterization, not measured by electrical test.
- 4/ All clocks and enable signals are disabled and the data inputs are static.
- 5/ Post total dose irradiation static supply current, I_{DDSB}, tested at T_C = +25°C, is guaranteed against the 125°C specified value (3.5 mA) shown here in Table IA.
- 6/ Idle current condition for the FIFO includes only the Read Clock (CLKRD) and Write Clock (CLKWR) signals. The Read Enable (ENRD) and the Write Enable (ENWR) signals are both disabled and the data inputs are static.
- 7/ Guaranteed by design, not measured by electrical test.
- 8/ Timing waveforms shown in Figure 3 shall meet the electrical performance characteristics specified in here. All timing parameters are tested except t_{ckr}, t_{ckh} (Read), t_{ckw}, t_{ckh} (Write), t_{pmr}, t_{mrr} which are guaranteed by design. Timing parameters in Figure 3 are tested with an equivalent load of 25pf.
- 9/ Tskew2 dictates on which cycle the flags will de-assert. If the falling edge of opposite clock is greater than Tskew2, then de-assert will happen on Cycle A, otherwise it could happen on Cycle A or Cycle B.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
8

TABLE IB. SEP test limits. 1/ 2/

Device type	T _A = Temperature ±10°C	Memory pattern	V _{DD} = 2.97 V		Bias V _{DD} = 3.63 V for Single event latch-up (SEL) test No SEL occurs at effective LET <u>5/</u> <u>6/</u>
			SER Adam 90% environment	Maximum device cross section	
01	+25°C	<u>3/</u>	SER = 1 x 10 ⁻⁹ upsets/bit-day <u>4/</u>	1 x 10 ⁻⁸ cm ² /bit	LET ≤ 120 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

4/ CREME 96 with Weibull parameters.

5/ Worst case temperature is T_A = +125°C ±10°C.

6/ Tested to an effective LET of ≥ 120 MeV/(mg/cm²), with no latch-up (SEL).

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

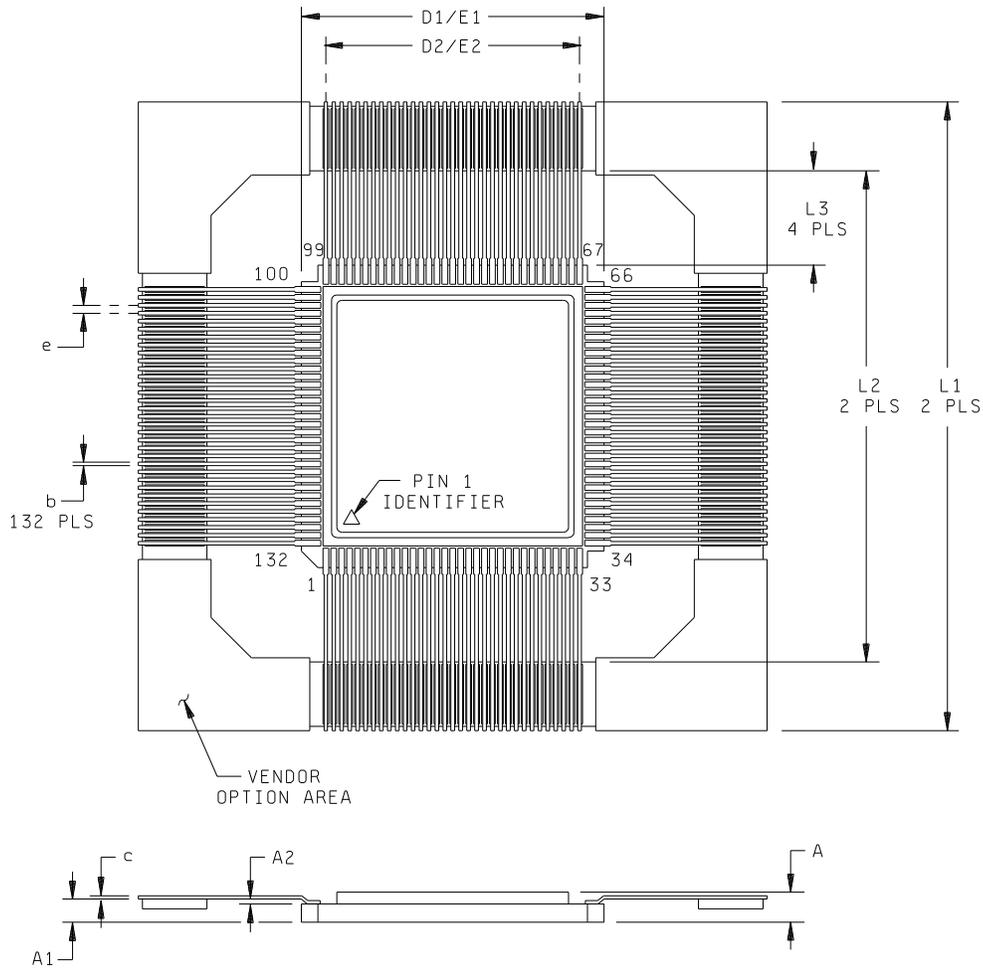
SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
9

Case outline X (see notes 1, 2, and 3)



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.084	.106	2.13	2.7	D1/E1	.94	.96	23.88	24.38
A1	.056	.076	1.42	1.93	D2/E2	.796	.804	20.22	20.42
A2	.005	.011	.13	.28	e	.023	.027	.584	.686
b	.008	REF	.2	REF	L1	1.49	1.98	37.85	49.4
c	.004	.0065	.1	.17	L2	1.49	1.57	37.85	39.88
					L3	.275	.305	6.99	7.75

- Notes: 1. Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.
 2. Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface.
 3. Terminal identification numbers need not appear on the package.

FIGURE 1. Case outline.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
10

Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	GND
2	Q6
3	Q7
4	Q8
5	Q9
6	Q10
7	GND1
8	Q11
9	Q12
10	Q13
11	Q14
12	GND1
13	Q15
14	Q16
15	Q17
16	Q18
17	V _{DD}
18	GND
19	Q19
20	Q20
21	Q21
22	Q22
23	GND1
24	Q23
25	Q24
26	Q25
27	Q26
28	GND1
29	Q27
30	Q28
31	Q29
32	Q30
33	GND
34	GND
35	V _{DD}
36	V _{DD}
37	Q31
38	Q32
39	Q33

Device types	All
Case outlines	X
Terminal number	Terminal symbol
40	Q34
41	GND1
42	Q35
43	ENRD
44	CLKRD
45	E
46	QF_TQF
47	E_F_FAULT
48	MR
49	OE
50	GND
51	GND1
52	GND1
53	E_F
54	HF
55	F
56	CLKWR
57	ENWR
58	D35
59	GND1
60	D34
61	D33
62	D32
63	D31
64	V _{DD}
65	V _{DD}
66	GND
67	GND
68	D30
69	D29
70	D28
71	D27
72	D26
73	GND1
74	D25
75	D24
76	D23
77	D22
78	GND1

FIGURE 2. Terminal connections.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
11

Device types	All
Case outlines	X
Terminal number	Terminal symbol
79	D21
80	D20
81	D19
82	D18
83	V _{DD}
84	GND
85	D17
86	D16
87	D15
88	D14
89	GND1
90	D13
91	D12
92	D11
93	D10
94	GND1
95	D9
96	D8
97	D7
98	D6
99	GND
100	GND
101	V _{DD}
102	V _{DD}
103	D5
104	D4
105	D3

Device types	All
Case outlines	X
Terminal number	Terminal symbol
106	D2
107	GND1
108	D1
109	D0
110	GND1
111	GND1
112	GND1
113	GND1
114	GND1
115	GND1
116	GND
117	GND1
118	GND1
119	GND1
120	GND1
121	GND1
122	GND1
123	Q0
124	Q1
125	GND1
126	Q2
127	Q3
128	Q4
129	Q5
130	V _{DD}
131	V _{DD}
132	GND

FIGURE 2. Terminal connections - continued.

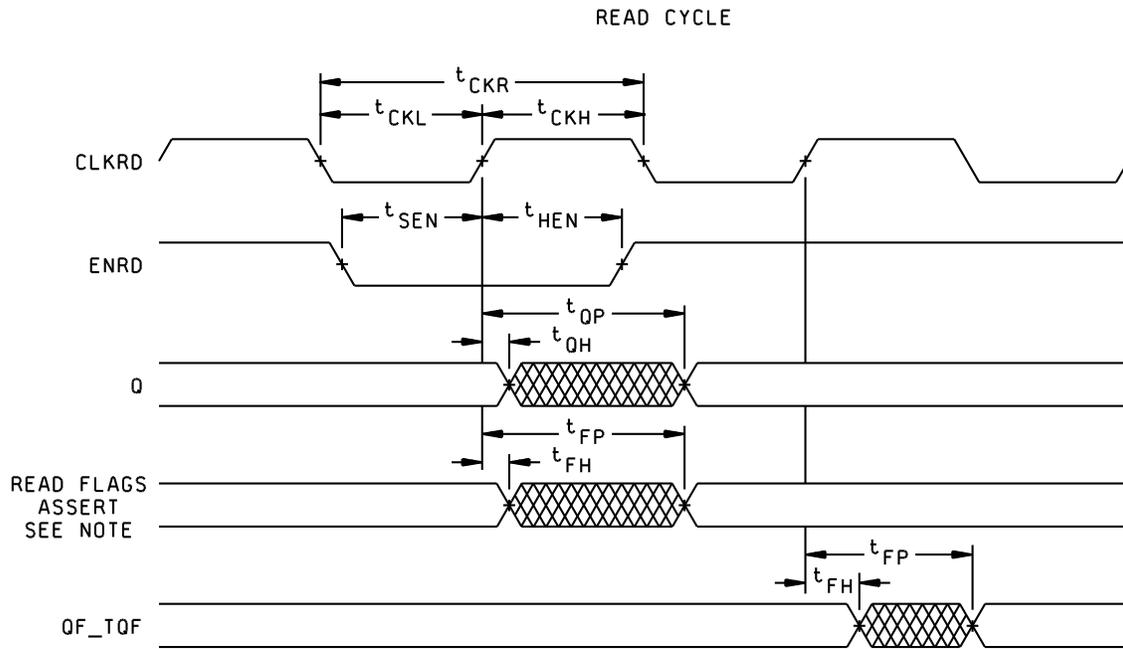
**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
12



Note: Read Flags = E, E_F, and E_F_Fault

FIGURE 3. Timing waveforms.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

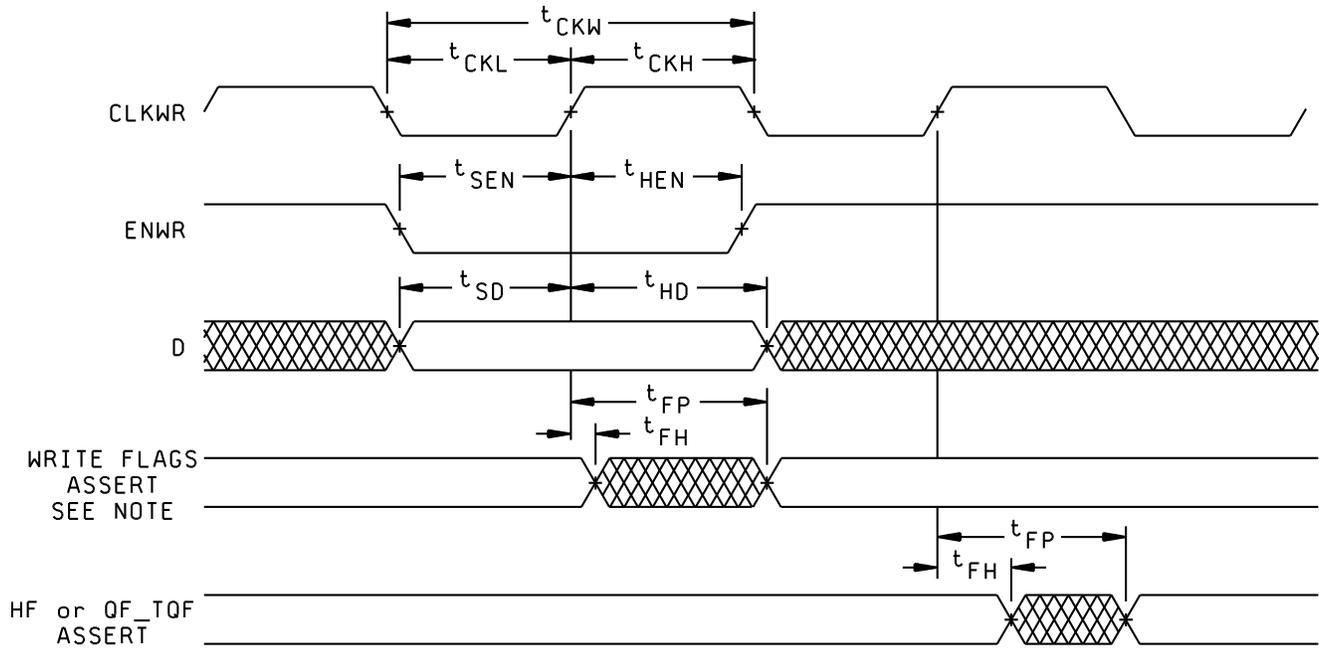
SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
13

WRITE CYCLE



Note: Write Flags = F, E_F, and E_F_Fault

FIGURE 3. Timing Waveforms – continued.

<p>STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990</p>	<p>SIZE A</p>		<p>5962-08208</p>
		<p>REVISION LEVEL A</p>	<p>SHEET 14</p>

SYNCHRONOUS RESET

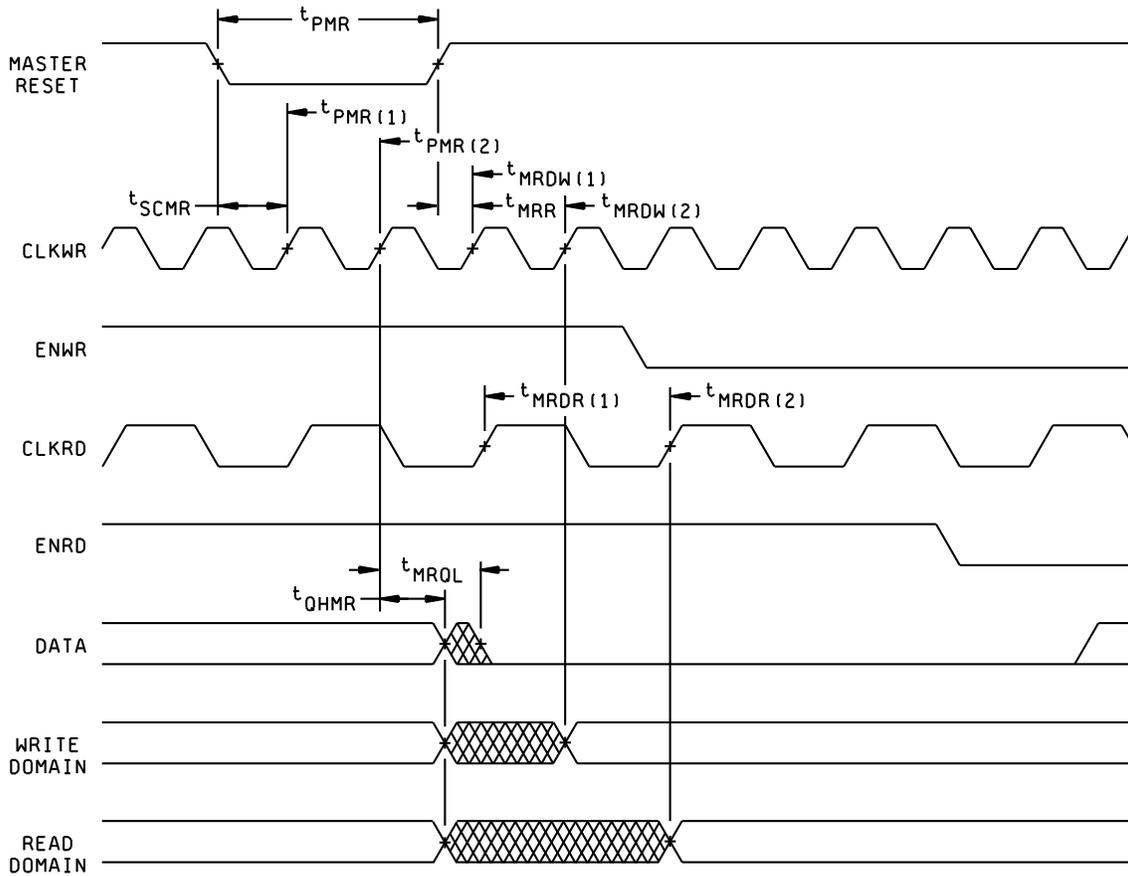


FIGURE 3. Timing Waveforms – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
15

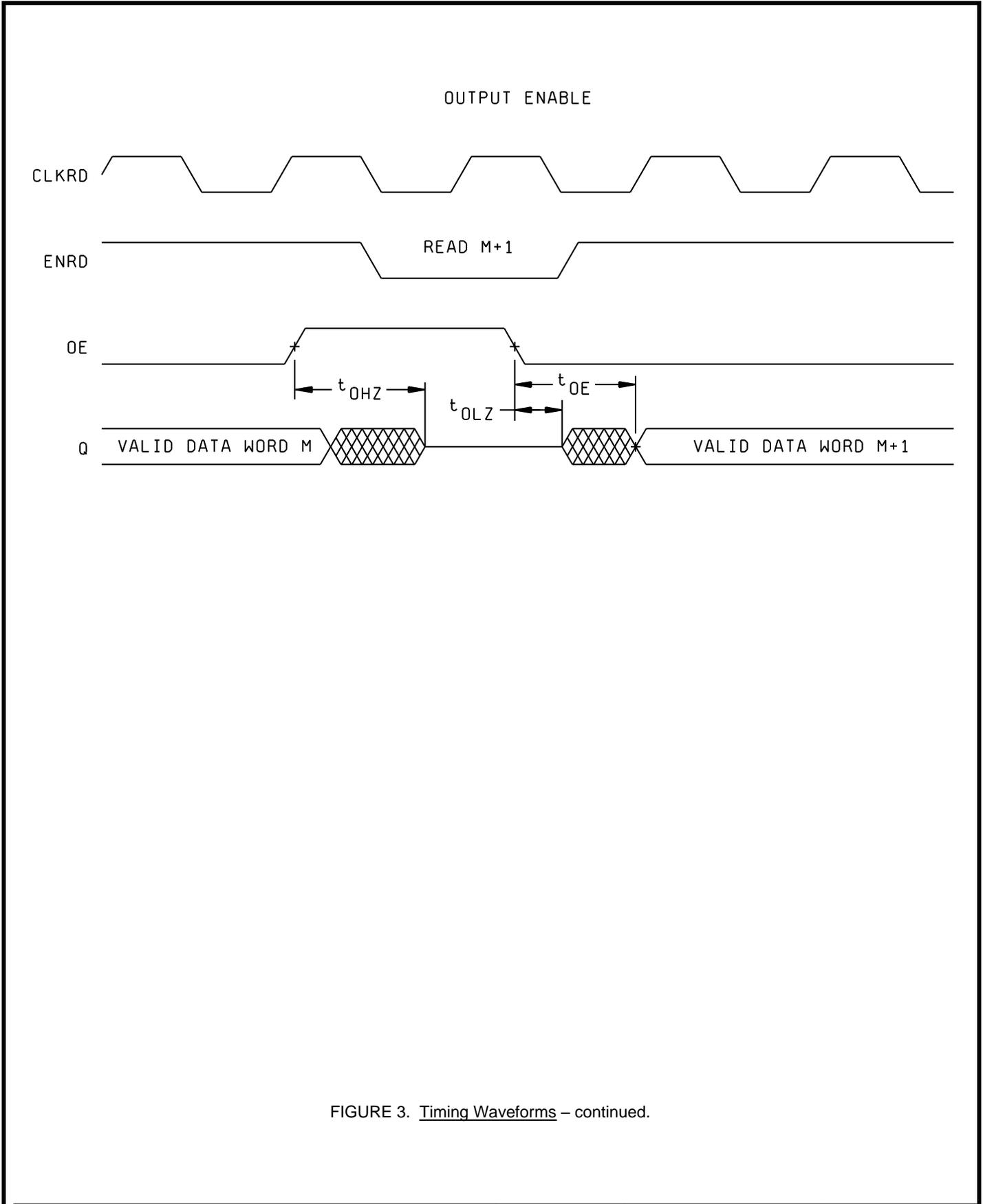


FIGURE 3. Timing Waveforms – continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 16

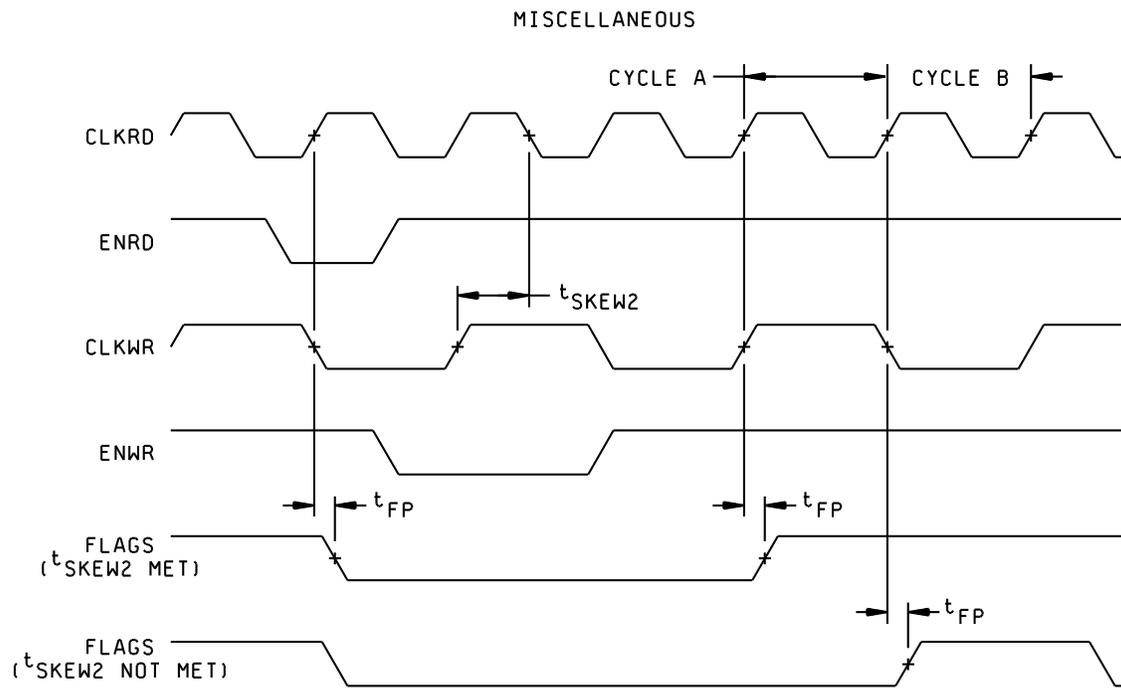


FIGURE 3. Timing Waveforms – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
17

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. In addition, special test structures may be used for latch-up characterization in place of using product. If test structures are used, testing shall be on five wafers. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 18

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^\circ\text{C} \pm 5^\circ\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

- a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^\circ\text{C} \pm 10^\circ\text{C}$. The latchup test temperature shall be at $125^\circ\text{C} \pm 10^\circ\text{C}$.
- f. Bias conditions shall be V_{DD} maximum = 2.97 V dc for the upset measurements and V_{DD} minimum = 3.63 V dc for the latchup measurements.
- g. For SEP test limits, see table IB herein.

4.4.4.5 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ after an exposure of 2×10^{13} neutrons/cm² (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 19

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1*, 7*, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
6	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limits
I _{DDSB} (standby)	± 10% of value listed in Table 1

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-08208

REVISION LEVEL
A

SHEET
20

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions (SEP).
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-08208
		REVISION LEVEL A	SHEET 21

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-06-28

Approved sources of supply for SMD 5962-08208 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962G0820801VXC	1RU44	8407971-1
5962G0820801QXC	1RU44	8407971-4
	1RU44	8407971-5

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

1RU44

Vendor name and address

BAE Systems
9300 Wellington Road
Manassas, VA 20110-4122

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.