REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete the word “DIGITAL” from the title block. Under paragraph 1.3, Voltage range, Enables or Y limit, delete “-1 V to +6 V” and substitute “-0.5 V to V_{CC} + 4 V”. - ro	10-10-19	C. Saffle
B	Update paragraphs to MIL-PRF-38535 requirements. - drw	19-07-12	Charles F. Saffle

REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rajesh Pithadia

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Robert M. Heber

DRAWING APPROVAL DATE
08-06-02

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, QUADRUPLE, DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-07248**

SHEET 1 OF 17

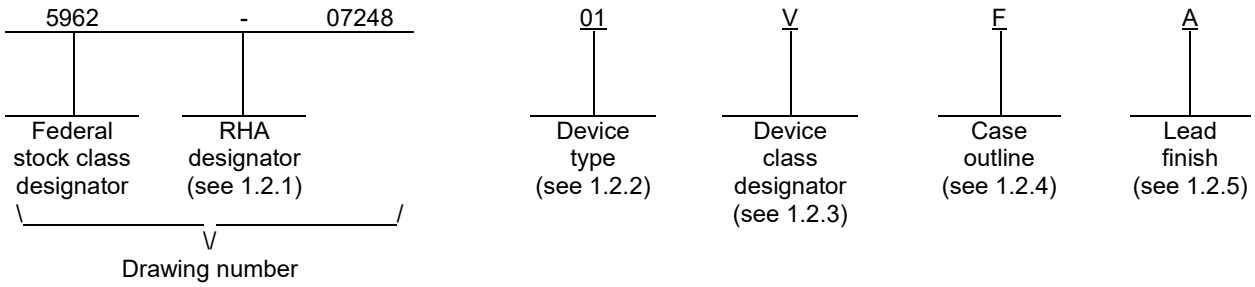
DSCC FORM 2233
APR 97

5962-E399-19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	SN55LVDS33-SP	Quad, differential line receiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +4 V 2/
Voltage range :	
Enables or Y	-0.5 V to V_{CC} +4 V
A or B	-5 V to +6 V
Lead temperature , 1.6 mm from case for 10 seconds	+260°C
Junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to case (θ_{JC})	12.0°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+3 V to +3.6 V
High level input voltage (V_{IH}) range, Enables	+2 V to +5 V
Low level input voltage (V_{IL}) range, Enables	0 V to +0.8 V
Magnitude of differential input voltage range, $\|V_{ID}\|$	+0.1 V to +3 V
Voltage range at any bus terminal (separately or common-mode)	-4 V to +5 V
Operating temperature range (T_J)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $3.0\ V \le V_{CC} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive going differential 1/ input voltage threshold	V_{IT1}	V_{IB} = -4 V or 5 V, see figure 4	1, 2, 3	01		50	mV
Negative going differential input voltage threshold	V_{IT2}	V_{IB} = -4 V or 5 V, see figure 4	1, 2, 3	01	-50		mV
Differential input failsafe 1/ voltage threshold	V_{IT3}	See figures 5 and 6	1, 2, 3	01	-32	-100	mV
High level output voltage	V_{OH}	I_{OH} = -4 mA	1, 2, 3	01	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 4 mA	1, 2, 3	01		0.4	V
Supply current	I_{CC}	G at V_{CC}, no load, steady state	1, 2, 3	01		25	mA
		G at GND	1, 2, 3			6	
Input current (A or B inputs)	I_I	V_I = 0 V, other input open	1, 2, 3	01		±25	µA
		V_I = 2.4 V, other input open	1, 2, 3			±25	
		V_I = -4 V, other input open	1, 2, 3			±80	
		V_I = 5 V, other input open	1, 2, 3			±45	
Differential input current ($I_{IA} - I_{IB}$)	I_{IO}	V_{ID} = 100 mV, V_{IC} = -4 V or 5 V	1, 2, 3	01		±5	µA
Power off input current (A or B inputs)	$I_{I(OFF)}$	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V	1, 2, 3	01		±25	µA
		V_A or V_B = -4 V or 5 V, V_{CC} = 0 V	1, 2, 3			±60	
High level input current (Enables)	I_{IH}	V_{IH} = 2 V	1, 2, 3	01		12	µA
Low level input current (Enables)	I_{IL}	V_{IL} = 0.8 V	1, 2, 3	01		12	µA
High impedance output current	I_{OZ}		1, 2, 3	01	-10	12	µA
Functional tests		See 4.4.1c	7, 8	01			
Propagation delay, low to high level output	$t_{PLH(1)}$	See figure 7	9, 10, 11	01	1.8	8	ns
Propagation delay, high to low level output	$t_{PHL(1)}$	See figure 7	9, 10, 11	01	1.8	8	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $3.0\ V \le V_{CC} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, failsafe 1/ deactivate time	t_{d1}	CL = 10 pF, see figures 6 and 7	9, 10, 11	01		11	ns
Delay time, failsafe 1/ activate time	t_{d2}	CL = 10 pF, see figures 6 and 7	9, 10, 11	01	0.2	2	µs
Part-to-part skew 2/	$t_{sk(pp)}$	See figure 7	9, 10, 11	01		1.2	ns
Propagation delay, high level to high impedance output	t_{PHZ}	See figure 8	9, 10, 11	01		12	ns
Propagation delay, low level to high impedance output	t_{PLZ}	See figure 8	9, 10, 11	01		12	ns
Propagation delay, high impedance to high level output	t_{PZH}	See figure 8	9, 10, 11	01		12	ns
Propagation delay, high impedance to low level output	t_{PZL}	See figure 8	9, 10, 11	01		12	ns

1/ If not tested, shall be guaranteed to the limits specified in table I herein.

2/ $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Device type	01
Case outline	F
Terminal number	Terminal symbol
1	1B
2	1A
3	1Y
4	G
5	2Y
6	2A
7	2B
8	GND
9	3B
10	3A
11	3Y
12	$\overline{G}$
13	4Y
14	4A
15	4B
16	V_{CC}

FIGURE 1. Terminal connections.

Differential input	Enables		Output
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq$ -32 mV	H	X	H
	X	L	H
-100 mV $\leq V_{ID} \leq$ -32 mV	H	X	?
	X	L	?
$V_{ID} \leq$ -100 mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = High voltage level
L = Low voltage level
? = Indeterminate
X = Irrelevant
Z = high impedance (off)

FIGURE 2. Truth table.

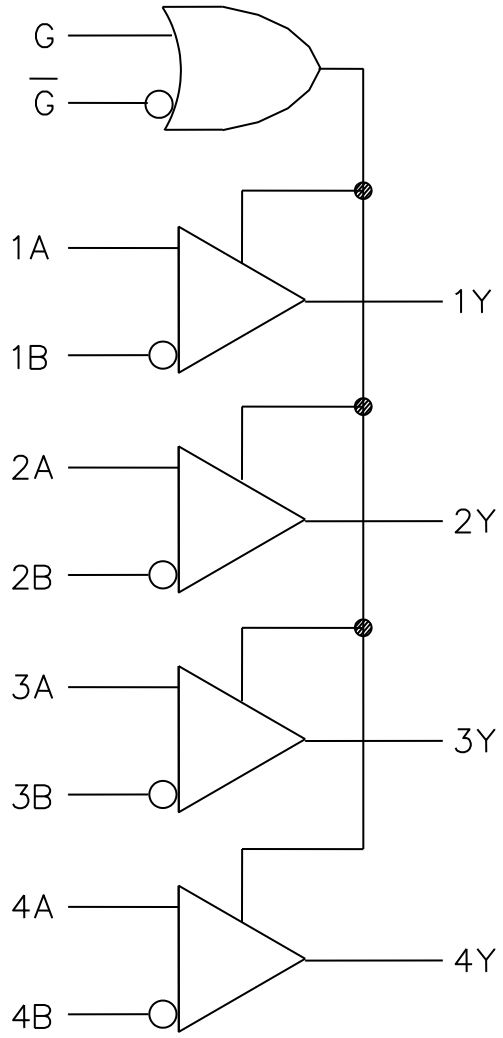
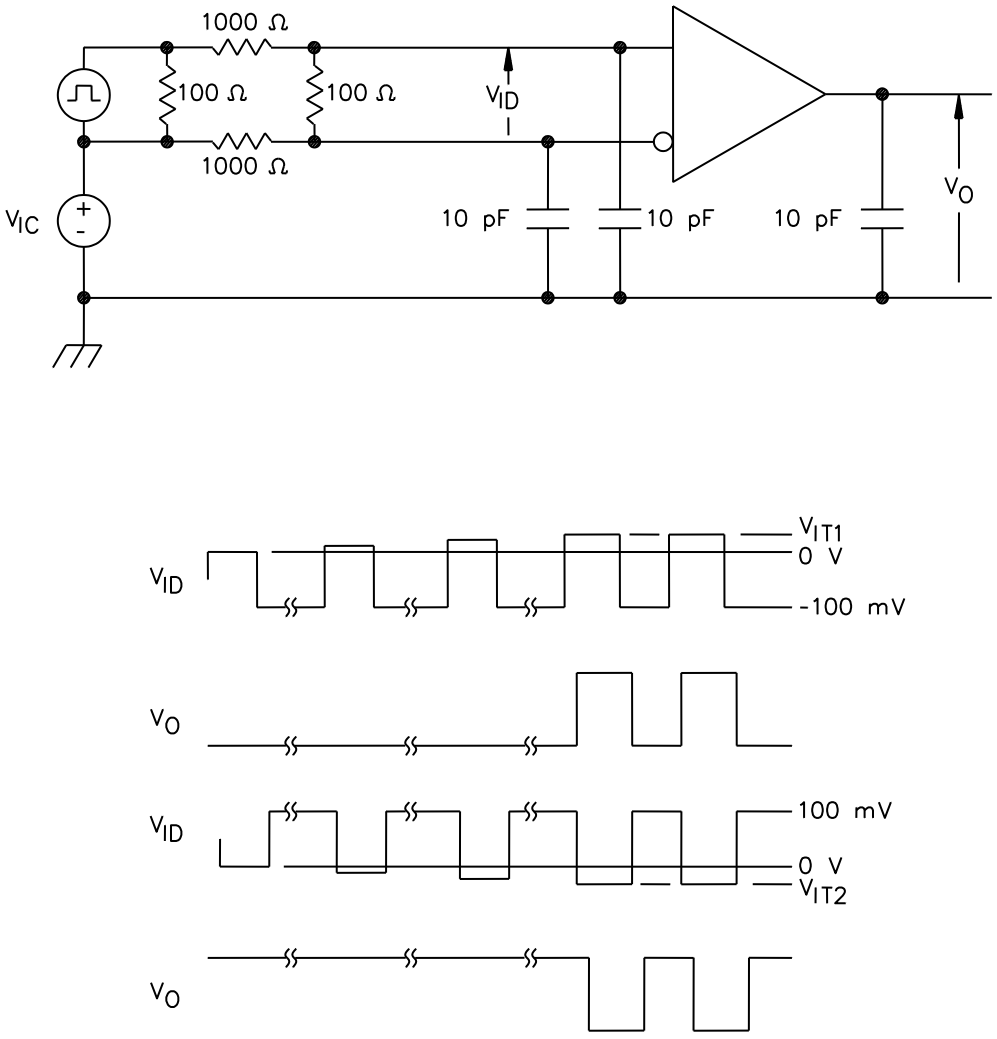


FIGURE 3. Logic diagram.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of < 1 ns. V_{IC} = common mode voltage, V_{ID} = Differential input voltage, and V_{IT} = input voltage threshold.

FIGURE 4. V_{IT1} and V_{IT2} input voltage threshold test circuit and waveforms.

Applied voltages 1/		Resultant inputs		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV) 2/	Output
-4000	-3900	-100	-3950	L
-4000	-3968	-32	-3984	H
4900	5000	-100	4950	L
4968	5000	-32	4984	H

1/ These voltages are applied for a minimum of 1.5 μs.

2/ Actual common mode value = $V_{IC} = (V_{IA} + V_{IB}) / 2$

FIGURE 5. Receiver minimum and maximum V_{IT3} input threshold test voltages.

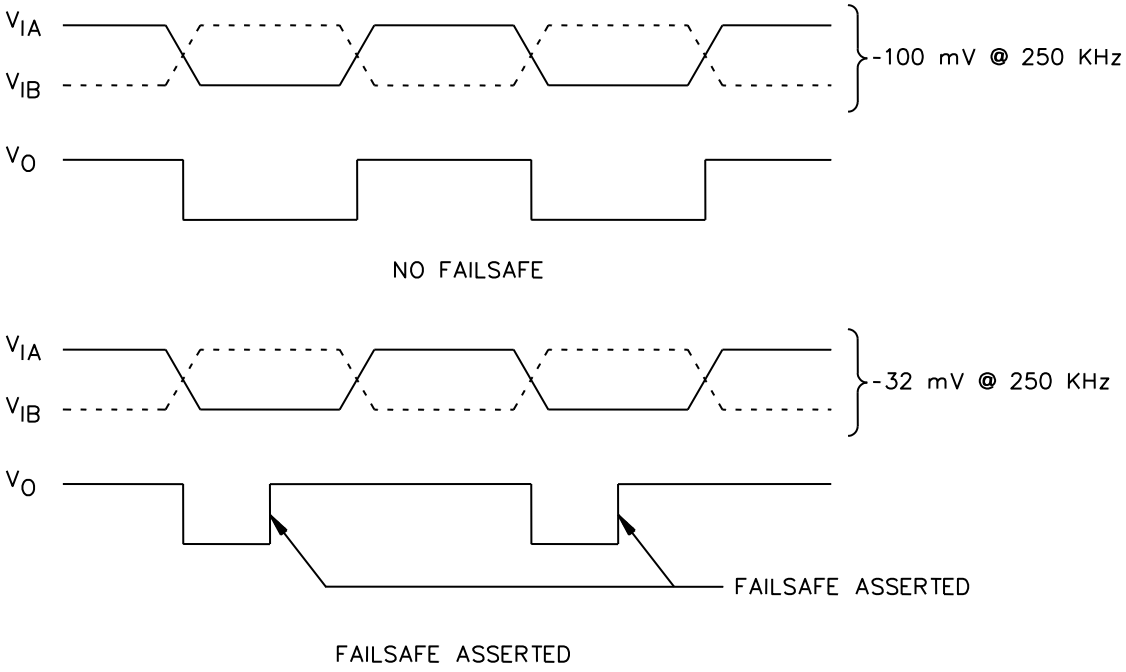


FIGURE 6. V_{IT3} failsafe threshold test.

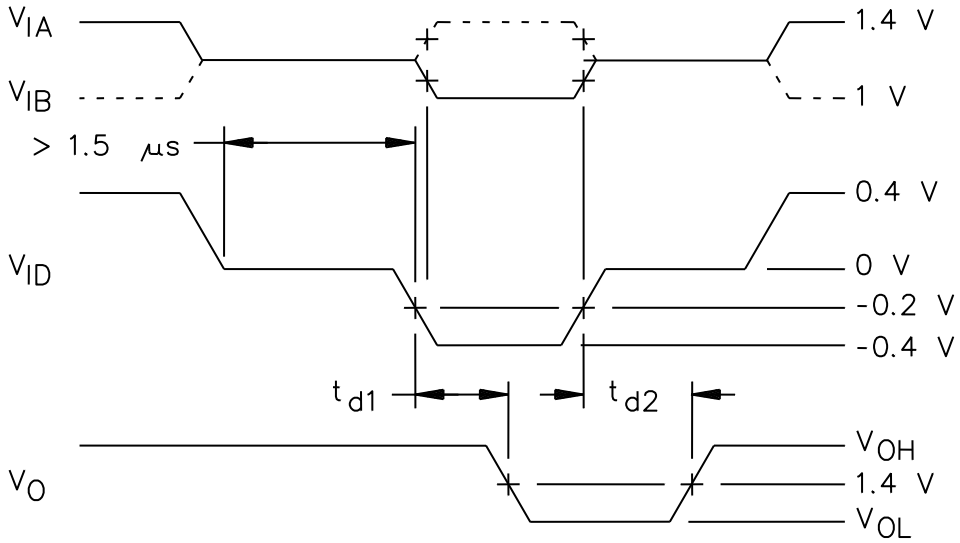
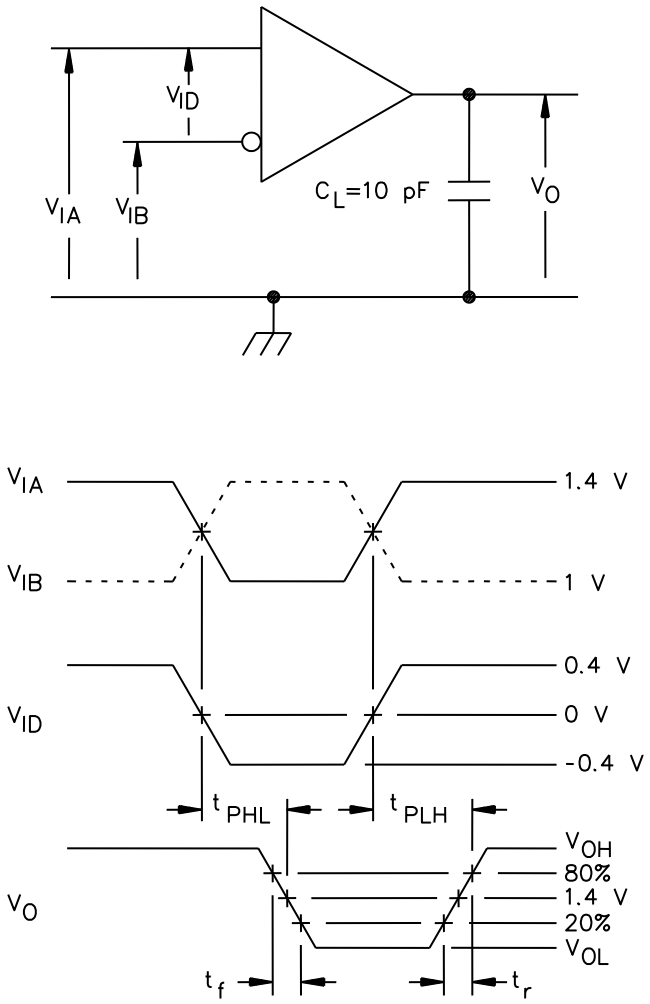
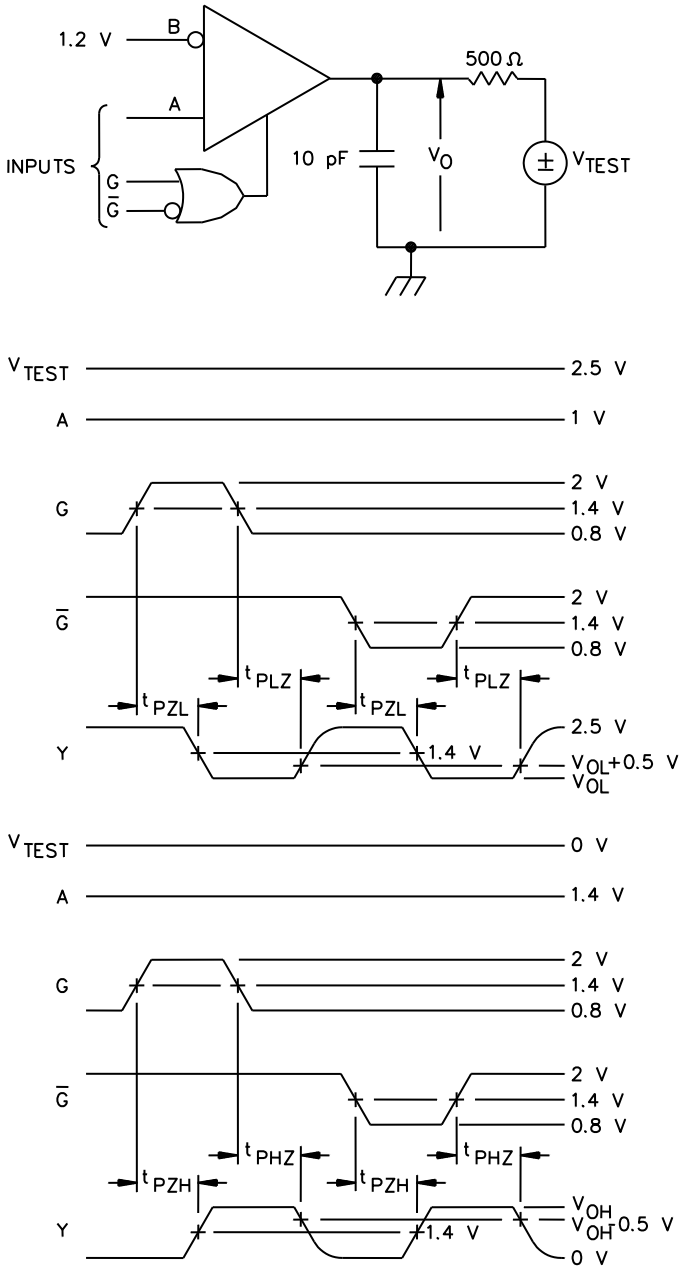


FIGURE 6. Failsafe activate and deactivate waveforms - continued.



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test (D.U.T).

FIGURE 7. Timing test circuit and waveforms.



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test (D.U.T).

FIGURE 8. Enable/Disable time test circuit and waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 1/	1, 2, 3, 9 1/, 2/
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11 3/
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	----	----

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.
3/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

TABLE IIB. Burn-in and operating life test delta parameters at +25°C.

Parameter 1/	Symbol	Conditions	Delta limit
Output voltage high level	V_{OH}	I_{OH} = -4 mA, V_{CC} = 3 V	±0.18 V
		I_{OH} = -4 mA, V_{CC} = 3.6 V	±0.18 V
Output voltage low level	V_{OL}	I_{OH} = -4 mA, V_{CC} = 3 V	±40 mV
		I_{OL} = 4 mA, V_{CC} = 3.6 V	±40 mV
Supply current disabled	I_{CCZ}		±0.6 mA
High level supply current	I_{CCH}		±2.5 mA
Low level supply current	I_{CCL}		±2.5 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-12

Approved sources of supply for SMD 5962-07248 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0724801VFA	01295	SN55LVDS33-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243