REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrected maximum output update rate test, f_{DAC}, in Table I from 2.4 min to 2.4 max. Added differential data interface section in Table I which includes T_{setup}, T_{hold} tests. Added delay lock loop (DLL) section in Table I which includes NegD, PosD, and f_{DAC} tests. Corrected terminal connection for terminal number M14 from GND to a blank space. Added to description for terminal number M12 in figure 2. Added figures 4 and 5. Removed references to class M. -rrp	13-05-01	C. Saffle
B	For sheet 7, table I, made corrections to the test limits for the t_{SETUP} and t_{HOLD} parameters. Figure 4, correct t_{SETUP} and t_{HOLD} timing. - drw	18-12-13	Charles F. Saffle

REV																				
SHEET																				
REV	B	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rajesh Pithadia

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COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Robert M. Heber

DRAWING APPROVAL DATE
09-01-26

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 2.4 GSPS DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-07247**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

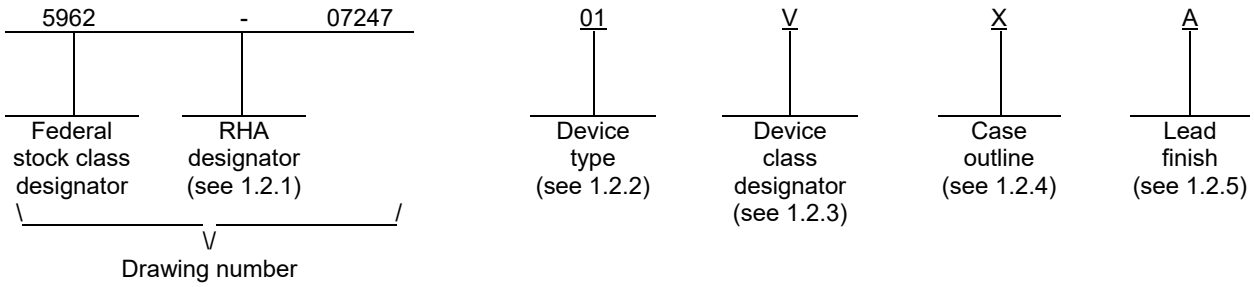
5962-E108-19

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	DAC5670-SP	14 bit, 2.4 GSPS digital-to-analog converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	see figure 1	192	Ceramic ball grid array

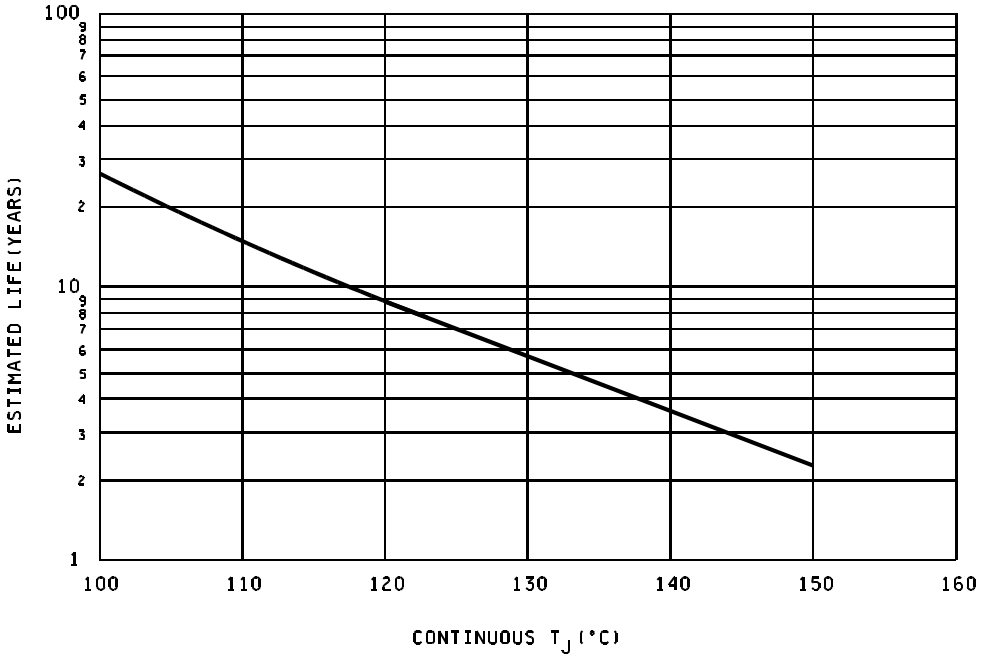
1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage, AV_{DD} to GND ..... 5.0 V
DA_P[13…0], DA_N[13…0], DB_P[13…0], DB_N[13…0] ..... -0.3 V min to AV_{DD} + 0.3 V max 2/
NORMAL, A_ONLY, A_ONLY_INV, A_ONLY_ZS ..... -0.3 V min to AV_{DD} + 0.3 V max 2/
DTCLK_P, DTCLK_N, DACCLK_P, DACCLK_N ..... -0.3 V min to AV_{DD} + 0.3 V max 2/
LVDS_HTB, INV_CLK, RESTART ..... -0.3 V min to AV_{DD} + 0.3 V max 2/
IOUT_P, IOUT_N ..... AV_{DD} – 0.5 V min to AV_{DD} + 0.3 V max 2/
CSCAP_IN, REFIO_IN, RBIAS_IN ..... -0.3 V min to AV_{DD} + 0.3 V max 2/
Total power dissipation (P_D) ..... 2350 mW
Peak input current (any input) ..... 20 mA
Peak total input current (all inputs) ..... -30 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds ..... +260°C
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 41.3°C/W
Thermal resistance, junction-to-case (θ_{JC}) ..... 3.8°C/W

1.4 Recommended operating conditions.

Operating case temperature range (T_C) ..... -55°C to +125°C
Estimated device life at elevated temperatures electromigration fail modes:



1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Measured with respect to GND.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution			1, 2, 3	All	14		Bits
DC accuracy section							
Integral nonlinearity	INL	f_{DAC} = 640 kHz, f_{OUT} = 10 kHz	1, 2, 3	All	-7.5	7.5	LSB
Differential nonlinearity	DNL		1, 2, 3		-0.98	1.75	LSB
Monotonocity			1, 2, 3	All	14		Bits
Analog output section							
Offset error		Mid code offset	1, 2, 3	All	-0.45	0.45	%FSR
Gain error		With external reference	1, 2, 3	All	-6.0	6.0	%FSR
		With internal reference	1, 2, 3		-6.0	6.0	%FSR
Full scale output current	I_{OFS}		1, 2, 3	All		30	mA
Output compliance range		$I_{O(FS)}$ = 20 mA, AV_{DD} = 3.15 V to 3.45 V	1, 2, 3	All	AV_{DD} - 0.5	AV_{DD} + 0.5	V
Reference output section							
Reference voltage	V_{REF}		1, 2, 3	All	1.14	1.26	V
Reference input section							
Input voltage range	V_{REFIO}		1, 2, 3	All	1.14	1.26	V
Power supply section							
Analog supply voltage	AV_{DD}		1, 2, 3	All	3	3.6	V
Analog supply current	I_{AVDD}	f_{DAC} = 2.4 GHz, NORMAL input mode	1, 2, 3	All		650	mA
Sleep mode, AV_{DD} supply current	I_{AVDD}	Sleep mode (SLEEP pin high)	1, 2, 3	All		180	mA
Power dissipation	P_D	f_{DAC} = 2.4 GHz, NORMAL input mode	1, 2, 3	All		2350	mW
Power supply rejection ratio	PSRR	AV_{DD} = 3.15 V to 3.45 V	1, 2, 3	All		1.3	%FSR/ V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog output section							
Maximum output update rate	f_{DAC}		4, 5, 6	All		2.4	GSPS
AC performance section							
Spurious free dynamic range	SFDR	f_{DAC} = 2.4 GSPS, f_{OUT} = 100 MHz, dual port mode, 0 dBFS	4, 5, 6	All	46		dBc
		f_{DAC} = 2.4 GSPS, f_{OUT} = 300 MHz, dual port mode, 0 dBFS	4, 5, 6		31		
		f_{DAC} = 2.4 GSPS, f_{OUT} = 500 MHz, dual port mode, 0 dBFS	4, 5, 6		35		
Signal-to-noise ratio	SNR	f_{DAC} = 2.4 GSPS, f_{OUT} = 100 MHz, dual port mode, 0 dBFS	4, 5, 6	All	58		dBc
		f_{DAC} = 2.4 GSPS, f_{OUT} = 300 MHz, dual port mode, 0 dBFS	4, 5, 6		56		
		f_{DAC} = 2.4 GSPS, f_{OUT} = 500 MHz, dual port mode, 0 dBFS	4, 5, 6		51		
Total harmonic distortion	THD	f_{DAC} = 2.4 GSPS, f_{OUT} = 100 MHz, dual port mode, 0 dBFS	4, 5, 6	All	45		dBc
		f_{DAC} = 2.4 GSPS, f_{OUT} = 300 MHz, dual port mode, 0 dBFS	4, 5, 6		31		
		f_{DAC} = 2.4 GSPS, f_{OUT} = 500 MHz, dual port mode, 0 dBFS	4, 5, 6		35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC performance section - continued							
Third order tow tone intermodulation	IMD3	f_{DAC} = 2.4 GSPS, f_{OUT} = 253 MHz and 257 MHz, each tone at -6 dBFS, dual port mode	4, 5, 6	All	47		dBc
		f_{DAC} = 2.4 GSPS, f_{OUT} = 299 MHz and 302 MHz, each tone at -6 dBFS, dual port mode	4, 5, 6		35		
Four tone intermodulation	IMD	f_{DAC} = 2.4 GSPS, f_{OUT} = 298 MHz, 299 MHz, 300 MHz, and 301 MHz. Each tone at -12 dBFS, dual port mode	4, 5, 6	All	47		dBc
Digital characteristics							
CMOS interface (SLEEP, RESTART, INV_CLK, NORMAL, A_ONLY, A_ONLY_INV, A_ONLY_ZS)							
High level input voltage	V_{IH}		1, 2, 3	All	2		V
Low level input voltage	V_{IL}		1, 2, 3	All	0	0.8	V
High level input current	I_{IH}		1, 2, 3	All		10	µA
Low level input current	I_{IL}		1, 2, 3	All	-10		µA
Differential data interface (DA_P[13:0], DA_N[13:0], DB_P[13:0], DB_N[13:0], DTCLK_P, DTCLK_N)							
Differential input threshold	V_{ITH}		1, 2, 3	All	-100	100	mV
Internal termination impedance	Z_T		1, 2, 3	All	80	125	Ω
Input common mode	V_{ICOM}		1, 2, 3	All	0.6	1.4	V
Differential data interface (DA_P[13:0], DA_N[13:0], DB_P[13:0], DB_N[13:0], DTCLK_P, DTCLK_N External timing with DLL in restart)							
Data setup to DLYCLK 2/	t_{setup}	RESTART = 1, DLYCLK 20 pF load, see figure 4	9, 10, 11	All	4.75		ns
Data hold to DLYCLK 2/	t_{hold}	RESTART = 1, DLYCLK 20 pF load, see figure 4	9, 10, 11	All	-3.5		ns

See footnotes at end of table.

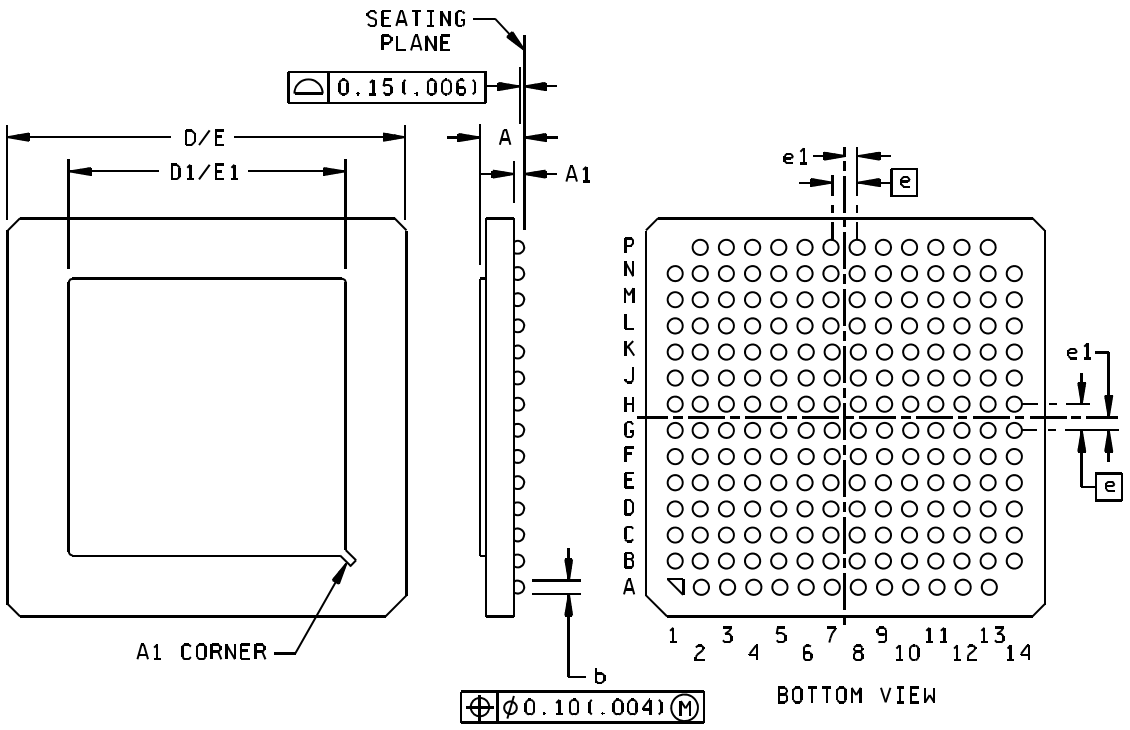
TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital characteristics - continued							
Clock inputs (DACCLK_P, DACCLK_N)							
Clock differential input voltage	V_{CLKTH}		1, 2, 3	All	200	1000	mV
Clock duty cycle			9, 10, 11	All	40	60	%
Clock common mode	V_{CLKCM}		1, 2, 3	All	1.0	1.4	V
Delay lock loop (DLL) See figure 5							
DLL minimum negative delay	NegD	RESTART = 0	9, 10, 11		150		
DLL minimum positive delay	PosD	RESTART = 0	9, 10, 11		600		
Maximum output update rate	f_{DAC}	RESTART = 0	4, 5, 6	All	1	2.4	GHz

1/ Unless otherwise specified, AV_{DD} = 3 V to 3.6 V, $I_{OUT(FS)}$ = 20 mA.

2/ Tested using signal to noise ratio (SNR) as pass/fail criteria.

Case X



Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	----	3.30	----	0.130
A1	0.50	0.70	0.020	0.028
b	0.60	0.90	0.024	0.035
D/E	18.80	19.20	0.740	0.756
D1/E1	13.00	13.40	0.512	0.528
e	1.27 BSC		0.05 BSC	
e1	0.635 BSC		0.025 BSC	
N	192			

NOTES:
1. Controlling dimensions are millimeters, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid.

FIGURE 1. Case outline.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	----	C1	DB9_N	E1	DB7_P
A2	DB10_N	C2	DB8_P	E2	DB5_N
A3	DB10_P	C3	AV_{DD}	E3	AV_{DD}
A4	DB12_P	C4	AV_{DD}	E4	AV_{DD}
A5	DB12_N	C5	AV_{DD}	E5	GND
A6	DLYCLK_N	C6	GND	E6	GND
A7	DLYCLK_P	C7	GND	E7	GND
A8	DTCLK_N	C8	GND	E8	GND
A9	DTCLK_P	C9	GND	E9	GND
A10	DA2_N	C10	AV_{DD}	E10	GND
A11	DA2_P	C11	DA7_N	E11	AV_{DD}
A12	DA3_N	C12	DA7_P	E12	AV_{DD}
A13	DA3_P	C13	DA5_P	E13	DA9_N
A14	----	C14	DA4_N	E14	DA8_P
B1	DB9_P	D1	DB7_N	F1	DB3_N
B2	GND	D2	DB8_N	F2	DB5_P
B3	GND	D3	DB6_P	F3	GND
B4	DB11_P	D4	DB6_N	F4	AV_{DD}
B5	DB11_N	D5	AV_{DD}	F5	GND
B6	DB13_N	D6	AV_{DD}	F6	GND
B7	DB13_P	D7	AV_{DD}	F7	GND
B8	DA0_P	D8	AV_{DD}	F8	GND
B9	DA0_N	D9	AV_{DD}	F9	GND
B10	DA1_P	D10	AV_{DD}	F10	GND
B11	DA1_N	D11	DA6_N	F11	AV_{DD}
B12	GND	D12	DA6_P	F12	GND
B13	GND	D13	DA5_N	F13	DA9_P
B14	DA4_P	D14	DA8_N	F14	DA10_N

FIGURE 2. Terminal connections.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
G1	DB3_P	J1	DB4_P	L1	DB1_N
G2	AV_{DD}	J2	DB2_P	L2	AV_{DD}
G3	GND	J3	GND	L3	REFIO_IN
G4	AV_{DD}	J4	AV_{DD}	L4	REFIO
G5	GND	J5	GND	L5	AV_{DD}
G6	GND	J6	GND	L6	AV_{DD}
G7	AV_{DD}	J7	GND	L7	AV_{DD}
G8	AV_{DD}	J8	GND	L8	AV_{DD}
G9	GND	J9	GND	L9	AV_{DD}
G10	GND	J10	GND	L10	AV_{DD}
G11	AV_{DD}	J11	AV_{DD}	L11	GND
G12	GND	J12	GND	L12	INV_CLK
G13	DA11_N	J13	DA13_P	L13	AV_{DD}
G14	DA10_P	J14	DA12_P	L14	DACCLK_N
H1	DB4_N	K1	DB1_P	M1	DB0_P
H2	AV_{DD}	K2	DB2_N	M2	GND
H3	GND	K3	AV_{DD}	M3	AV_{DD}
H4	AV_{DD}	K4	AV_{DD}	M4	AV_{DD}
H5	GND	K5	GND	M5	AV_{DD}
H6	GND	K6	GND	M6	IOUT_N
H7	AV_{DD}	K7	GND	M7	IOUT_P
H8	AV_{DD}	K8	GND	M8	GND
H9	GND	K9	GND	M9	GND
H10	GND	K10	GND	M10	AV_{DD}
H11	AV_{DD}	K11	AV_{DD}	M11	GND
H12	GND	K12	AV_{DD}	M12	RESTART
H13	DA11_P	K13	DA13_N	M13	GND
H14	DA12_N	K14	DACCLK_P	M14	----

FIGURE 2. Terminal connections – continued.

Device type	All
Case outline	X
Terminal number	Terminal symbol
N1	DB0_N
N2	GND
N3	GND
N4	AV_{DD}
N5	GND
N6	GND
N7	GND
N8	GND
N9	GND
N10	A_ONLY
N11	----
N12	----
N13	A_ONLY_Z
N14	GND
P1	----
P2	CSCAP_IN
P3	CSCAP
P4	RBIAS_IN
P5	RBIAS_OUT
P6	----
P7	GND
P8	GND
P9	LVDS_HTB
P10	AV_{DD}
P11	SLEEP
P12	A_ONLY_INV
P13	M_NORMAL
P14	----

FIGURE 2. Terminal connections – continued.

Terminal name	Terminal number	I/O	Description
DACCLK_P	K14	I	External clock, sample clock for the DAC
DACCLK_N	L14	I	Complementary external clock, sample clock for the DAC.
DLYCLK_P	A7	O	DDR type data clock to data source.
DLYCLK_N	A6	O	DDR type data clock to data source complementary signal.
DTCLK_P	A9	I	Input data toggling reference bit.
DTCLK_N	A8	I	Input data toggling reference bit, complementary signal.
DA_P[13]	J13	I	Port A data bit 13 (MSB)
DA_N[13]	K13	I	Port A data bit 13 complement (MSB)
DA_P[12]	J14	I	Port A data bit 12
DA_N[12]	H14	I	Port A data bit 12 complement
DA_P[11]	H13	I	Port A data bit 11
DA_N[11]	G13	I	Port A data bit 11 complement
DA_P[10]	G14	I	Port A data bit 10
DA_N[10]	F14	I	Port A data bit 10 complement
DA_P[9]	F13	I	Port A data bit 9
DA_N[9]	E13	I	Port A data bit 9 complement
DA_P[8]	E14	I	Port A data bit 8
DA_N[8]	D14	I	Port A data bit 8 complement
DA_P[7]	C12	I	Port A data bit 7
DA_N[7]	C11	I	Port A data bit 7 complement
DA_P[6]	D12	I	Port A data bit 6
DA_N[6]	D11	I	Port A data bit 6 complement
DA_P[5]	C13	I	Port A data bit 5
DA_N[5]	D13	I	Port A data bit 5 complement
DA_P[4]	B14	I	Port A data bit 4
DA_N[4]	C14	I	Port A data bit 4 complement
DA_P[3]	A13	I	Port A data bit 3
DA_N[3]	A12	I	Port A data bit 3 complement
DA_P[2]	A11	I	Port A data bit 2

FIGURE 2. Terminal connections – continued.

Terminal name	Terminal number	I/O	Description
DA_N[2]	A10	I	Port A data bit 2 complement
DA_P[1]	B10	I	Port A data bit 1
DA_N[1]	B11	I	Port A data bit 1 complement
DA_P[0]	B8	I	Port A data bit 0 (LSB)
DA_N[0]	B9	I	Port A data bit 0 complement (LSB)
DB_P[13]	B7	I	Port B data bit 13 (MSB)
DB_N[13]	B6	I	Port B data bit 13 complement (MSB)
DB_P[12]	A4	I	Port B data bit 12
DB_N[12]	A5	I	Port B data bit 12 complement
DB_P[11]	B4	I	Port B data bit 11
DB_N[11]	B5	I	Port B data bit 11 complement
DB_P[10]	A3	I	Port B data bit 10
DB_N[10]	A2	I	Port B data bit 10 complement
DB_P[9]	B1	I	Port B data bit 9
DB_N[9]	C1	I	Port B data bit 9 complement
DB_P[8]	C2	I	Port B data bit 8
DB_N[8]	D2	I	Port B data bit 8 complement
DB_P[7]	E1	I	Port B data bit 7
DB_N[7]	D1	I	Port B data bit 7 complement
DB_P[6]	D3	I	Port B data bit 6
DB_N[6]	D4	I	Port B data bit 6 complement
DB_P[5]	F2	I	Port B data bit 5
DB_N[5]	E2	I	Port B data bit 5 complement
DB_P[4]	J1	I	Port B data bit 4
DB_N[4]	H1	I	Port B data bit 4 complement
DB_P[3]	G1	I	Port B data bit 3
DB_N[3]	F1	I	Port B data bit 3 complement
DB_P[2]	J2	I	Port B data bit 2
DB_N[2]	K2	I	Port B data bit 2 complement

FIGURE 2. Terminal connections – continued.

Terminal name	Terminal number	I/O	Description
DB_P[1]	K1	I	Port B data bit 1
DB_N[1]	L1	I	Port B data bit 1 complement
DB_P[0]	M1	I	Port B data bit 0 (LSB)
DB_N[0]	N1	I	Port B data bit 0 complement (LSB)
IOUT_P	M7	O	DAC current output. Full scale when all input bits are set 1.
IOUT_N	M6	O	DAC complementary current output. Full scale when all input bits are 0.
RBIASOUT	P5	O	Rbias resistor current output.
RBIASIN	P4	I	Rbias resistor sense input.
CSCAP	P3	O	Current source bias voltage.
CSCAP_IN	P2	I	Current source bias voltage sense input.
REFIO	L4	O	Bandgap reference output.
REFIO_IN	L3	I	Bandgap reference sense input.
RESTART	M12	I	Resets DLL when high. Low for DLL operation. High for using external setup/hold timing.
LVDS_HTB	P9	I	DLYCLK_P/N control, lvds mode when high, ht mode when low.
INV_CLK	L12	I	Inverts the DLL target clocking relationship when high. Low for normal DLL operation.
SLEEP	P11	I	Active-high sleep.
NORMAL	P13	I	High for {a0, b0, a1,b1,a2,b2,…} normal mode.
A_ONLY	N10	I	High for {a0, a0, a1,a1,a2,a2,…} A_only mode.
A_ONLY_INV	P12	I	High for {a0, -a0, a1,-a1,a2,-a2,…} A_only_inv mode.
A_ONLY_ZS	N13	I	High for {a0, 0,a1,0, a2,0,…} A_only_zs mode.

FIGURE 2. Terminal connections – continued.

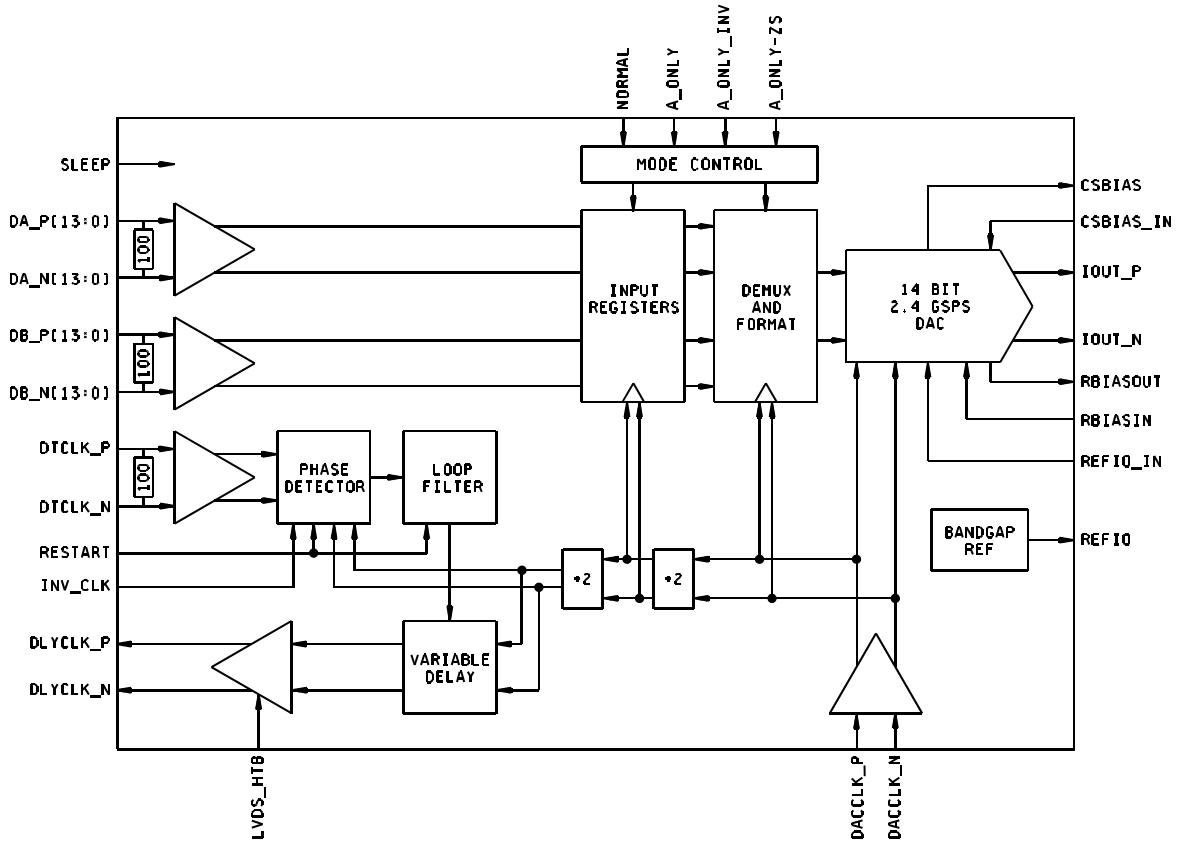


FIGURE 3. Block diagram.

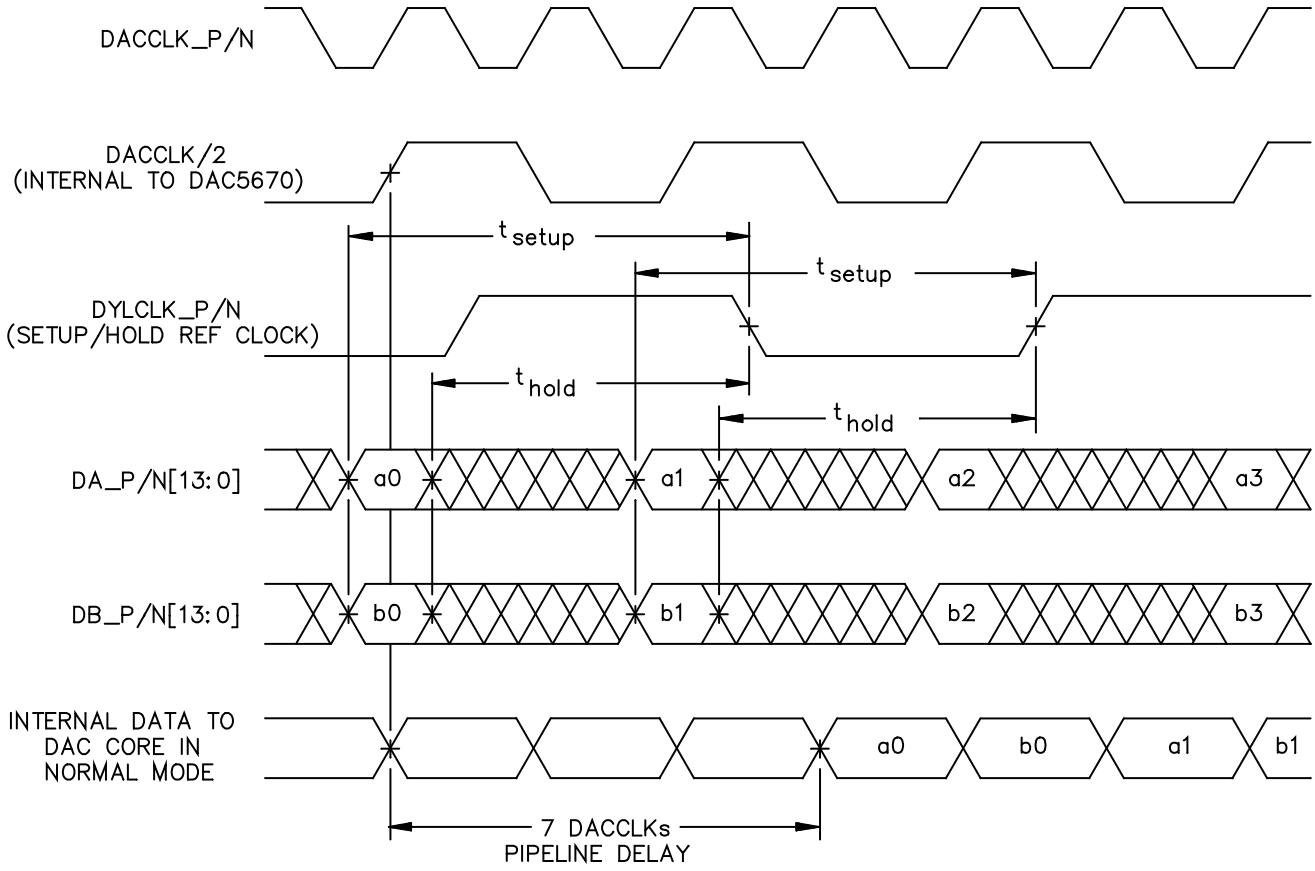


FIGURE 4. External interface timing with DLL in Restart waveform.

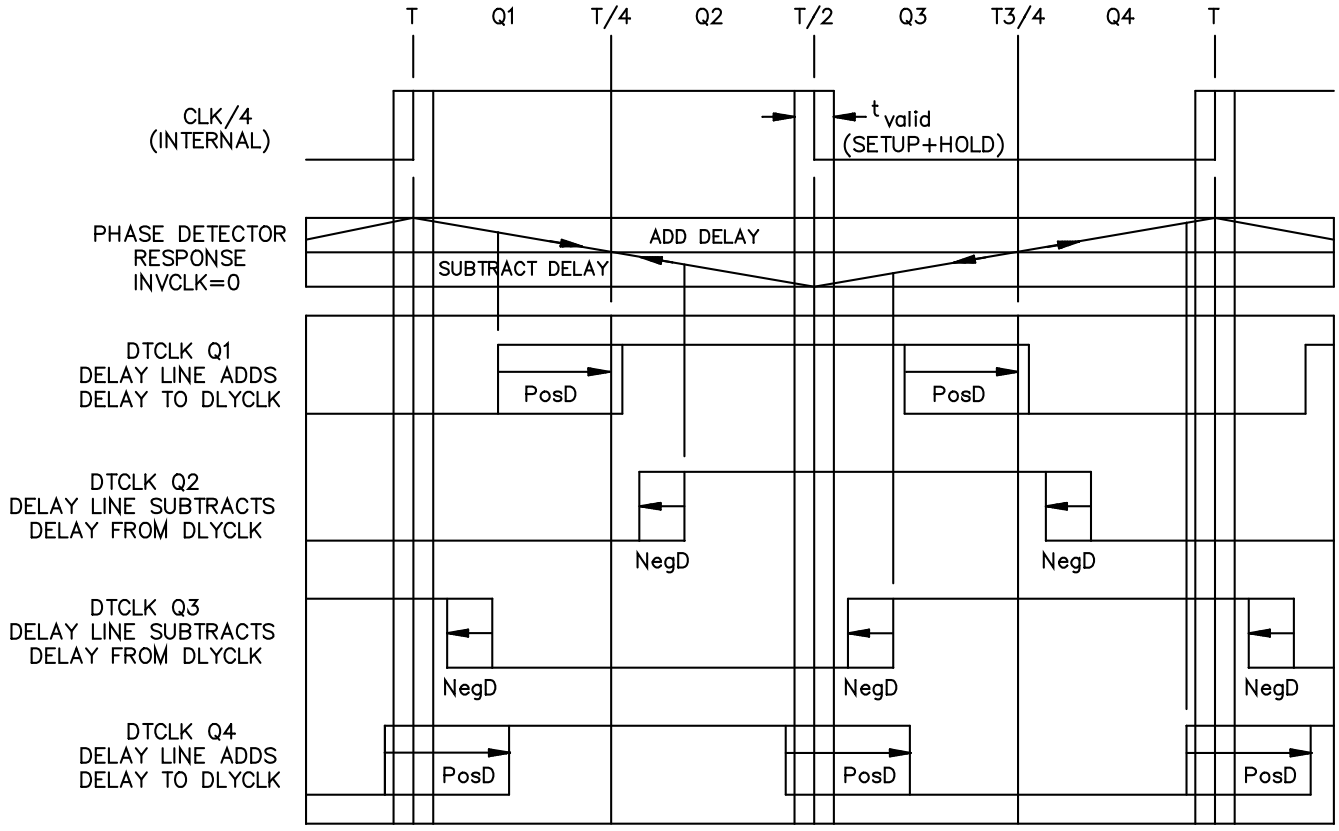


FIGURE 5. DLL phase detector behavior waveform.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4	1, 4
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 9, 10, 11 1/, 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11 2/
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	----	----

1/ PDA applies to subgroup 1
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters 1/	Delta limits
Reference voltage, V_{REF}	±55 mV
Total supply current, I_{AVDD}	±65 mA
CMOS interface input current, I_{IH}/I_{IL}	±350 nA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-12-13

Approved sources of supply for SMD 5962-07247 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0724701VXA	01295	DAC5670MGEM-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243