REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct Receiver input voltage range in section 1.3, Receiver differential voltage in section 1.4 and Output voltage swing (Vo) per MIL-STD-1760 and footnotes 9/ in the table IA. - MAA	09-03-10	Thomas M. Hess
B	Correct physical dimension of case outline Y in figure 1. Update Boilerplate paragraphs to current requirement of MIL-PRF-38535 - MAA	10-09-29	Thomas M. Hess
C	Correct transformer coil ratio, in Figure 9. - PHN	15-10-07	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Phu H. Nguyen

DLA LAND AND MARITIME
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
08-07-01

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, DUAL CHANNEL, BUS TRANSCEIVER, TTL INPUT/OUTPUT, MONOLITHIC SILICON

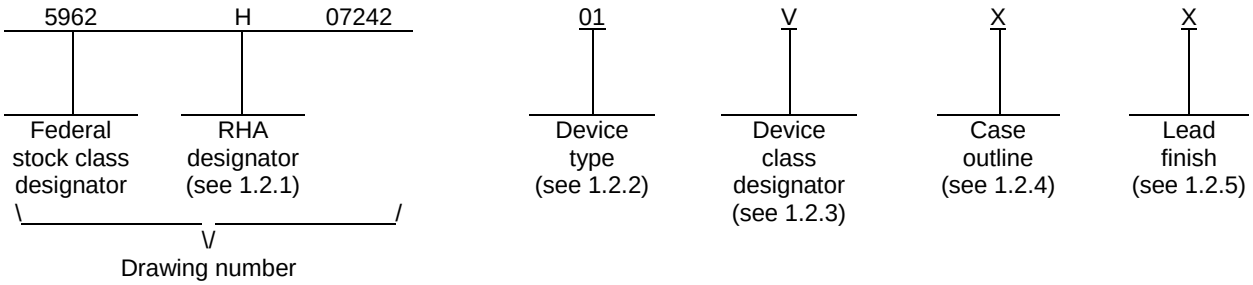
SIZE	CAGE CODE	
A	**67268**	**5962-07242**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT63M143	Dual channel, bus transceiver, TTL input/output, MIL-STD-1553 A/B compatible.
02	UT63M143	Dual channel, bus transceiver, TTL input/output, MIL-STD-1760 compatible.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	36	Dual in-line package
Y	See figure 1	24	Dual flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) ..... -0.3 V to +7.0 V
Input voltage range (Receiver) ..... +8.0 V_{P-P}
Logic input voltage range ..... -0.3 V to V_{DD} +0.3 V
Receiver common mode input voltage range ..... -5.0 V to +5.0 V
Maximum package power dissipation @ T_C = 125°C ..... 7.1 W 2/
Thermal impedance, junction to case (θ_{JC}): ..... 7.0 °C/W
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Maximum junction temperature (T_J) ..... 175°C

1.4 Recommended operating conditions.

Supply voltage range ..... +3.15 V to 3.45 V
Logic input voltage range ..... 0 V to V_{DD}
Receiver differential voltage @ RXIN & $\overline{\text{RXIN}}$ ..... 0.4 to 3.0 $V_{PP,L-L}$
Receiver common mode voltage range ..... ±4.0 V
Driver peak output current ..... 960 mA
Serial data rate ..... 0.3 to 1.0 MHz
Driver typical output current ..... 600 mA
Case operating temperature range (T_C) ..... -55°C to 125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) ..... ≥1 x 10^6 Rads(Si)
Single event phenomenon (SEP):
No SEU at effective LET (see 4.4.4.4): 3/
No SEL at effective LET (see 4.4.4.4): ..... ≤111 MeV/(mg/cm^2) 4/
Dose rate upset (20 ns pulse) 5/
Dose rate survivability 5/
Dose rate latch-up 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2/ V_{DD} = 3.45 V, T_C = 125°C, $P_{DMAX} = (T_{JMAX} - T_{CMAX})/\theta_{JC}$, per MIL-STD-883, method 1012, section 3.4.1. Applications that dissipate more than the specified amount of power must reduce the case temperature to ensure the maximum junction temperature is not violated.

3/ This device has no storage elements to upset.

4/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

5/ When characterized as a result of the procuring activities request, the condition will be specified.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1553 - Digital time division command/response multiplex data bus.
MIL-STD-1760 - Aircraft/Store Electrical Interconnector System.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.
MIL-HDBK-1553 - Multiplex Application handbook.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Driver, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Transmit operating mode. The transmit operating mode shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Typical transmitter and receiver waveforms. The typical transmitter and receiver waveforms shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Transceiver test circuit with load. The transceiver test circuit with load shall be as specified on figure 7-9.

3.2.8 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 89 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.15\ V \le V_{DD} \le 3.45\ V$ Device type: All unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage	V_{IL}	Pin: RXEN, TXIHB, TXIN, $\overline{TXIN}$	1, 2, 3		0.8	V
		M, D, P, L , R, F, G, H	1		0.8	
High level input voltage	V_{IH}	Pin: RXEN, TXIHB, TXIN, $\overline{TXIN}$	1, 2, 3	2.0		
		M, D, P, L , R, F, G, H	1	2.0		
Input current	I_I	$V_{IN} = V_{DD}$ or V_{SS} Pin: RXEN 2/,TXIHB, TXIN, $\overline{TXIN}$	1, 2, 3	-10	10	µA
		M, D, P, L , R, F, G, H	1	-10	10	
Low level output voltage	V_{OL}	I_{OL} = +4 mA Pin: RXOUT, $\overline{RXOUT}$	1, 2, 3		0.55	V
		M, D, P, L , R, F, G, H	1		0.55	
High level output voltage	V_{OH}	I_{OH} = -0.4 mA Pin: RXOUT, $\overline{RXOUT}$	1, 2, 3	2.4		
		M, D, P, L , R, F, G, H	1	2.4		
Supply current to V_{dd}	I_{DD}	0% duty cycle (non-transmitting)	1, 2, 3		14.5	mA
		25% duty cycle (f = 1 MHz)	1, 2, 3		200	
		50% duty cycle (f = 1 MHz)	1, 2, 3		387	
		87.5% duty cycle (f = 1 MHz)	1, 2, 3		670	
		100% duty cycle (f = 1 MHz) 3/	1, 2, 3		761	
Input capacitance 4/	C_{IN}	f = 1 MHz at 0 V, See 4.4.1.c Pin: RXEN, TXIHB, TXIN, $\overline{TXIN}$	4		15	pF
Output capacitance 4/	C_{OUT}	f = 1 MHz at 0 V, See 4.4.1.c Pin: RXOUT, $\overline{RXOUT}$	4		20	pF
Common mode input voltage 3/	V_{IC}	Direct-coupled stub; see figure 8, point A. input 1.2 V_{P-P}, 200 ns rise/fall time ±25 ns, f = 1 MHz	1,2,3	-5	5	V
		M, D, P, L , R, F, G, H	1	-5	5	
Input threshold voltage (no response)	V_{TH}	Transformer-coupled stub; see figure 9, point A input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0 → 1 transition) 3/	1,23		0.20	$V_{PP,L-L}$
		Direct-coupled stub; see figure 8, point A. input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0 → 1 transition) 5/	1,2,3		0.28	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.15\ V \le V_{DD} \le 3.45\ V$ Device type: All unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input threshold voltage (response)	V_{TH}	Transformer-coupled stub; see figure 9, point A, input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0 ⟶ 1 transaction) 3/	1,23	0.86	14.0	$V_{PP,L-L}$
		Direct-couple stub; see figure 8, point A input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0 ⟶ 1 transaction) 5/	1,2,3	1.20	20.0 7/	
Common mode rejection ratio 3/ 6/	CMRR		1,2,3			Pass/ Fail
Output voltage swing per: MIL-STD-1553B 3/	V_O	Transformer-coupled stub, see figure 9, point A input f = 1 MHz, R_L = 70 Ω, device type 01	1,2,3	18	27	$V_{PP,L-L}$
MIL-STD-1553B		Direct-coupled stub, see figure 8, point A input f = 1 MHz, R_L = 35 Ω, device type 01		6	9	
MIL-STD-1553A 3/		Transformer-coupled stub, see figure 9, point A input f = 1 MHz, R_L = 70 Ω, device type 01		6	20	
MIL-STD-1760 3/ 9/		Transformer-coupled stub, see figure 9, point A input f = 1 MHz, R_L = 70 Ω, device type 02		20	27	
Output noise voltage differential	V_{NS}	Transformer-coupled stub, see figure 9, point A, input f = DC to 10 MHz, R_L = 70 Ω 3/	1,2,3		14	mV-RMS$_{L-L}$
		Direct-coupled stub, see figure 8, point A; input f = DC to 10 MHz, R_L = 35 Ω 8/			5	
Output symmetry	V_{OS}	Transformer-coupled stub, see figure 9, point A, R_L = 140 Ω, measurement taken 2.5 µs after end of transmission 3/	1,2,3	-250	+250	$mV_{PP,L-L}$
		Direct-coupled stub, see figure 8,point A; R_L = 35 Ω, measurement taken 2.5 µs after end of transmission 10/		-90	+90	
Output voltage distortion (overshoot or ring)	V_{DIS}	Transformer-coupled stub, see figure 9, point A R_L = 70 Ω 3/	1,2,3	-900	+900	$mV_{peak,L-L}$
		Direct-coupled stub, see figure 8,Point A; R_L = 35 Ω		-300	+300	
Terminal input impedance 3/	T_{IZ}	Transformed-coupled stub, see figure 9, point A; input f = 75 KHz to 1 MHz, (power on or power off; non-transmitting, R_L removed from circuit)	1,2,3	1		kΩ
		Direct-couple stub, see figure 8, point A; input f = 75 KHz to 1 MHz (power on or power off; non-transmitting, R_L removed from circuit)		2		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.15\ V \le V_{DD} \le 3.45\ V$ Device type: All unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Transmitter output rise/fall time	t_R, t_F	Input f = 1 MHz 50% duty cycle: direct-couple RL = 35 Ω output at 10% through 90% points TXOUT, $\overline{TXOUT}$ See figure 6.	9,10,11	100	300	ns
RXOUT delay	t_{RXDD}	RXOUT to $\overline{RXOUT}$, see figure 5.		-200	200	
TXIN skew 11/	t_{TXDD}	TXIN to $\overline{TXIN}$, see figure 5.		-25	25	
Zero crossing distortion 5/	t_{RZCD}	Direct-couple stub; input f = 1 MHz, 3 VPP (skew INPUT ±150 ns), rise/fall time 200 ns, see figure 6		-150	150	
Zero crossing stability	t_{TZCS}	Input TXIN and $\overline{TXIN}$ should create transmitter output zero crossing at 500 ns, 1000 ns, 1500 ns, and 2000 ns. These zero crossing should not deviate more than ±25 ns. See figure 6.		-25	25	
Transmitter off; delay from inhibit active 12/	t_{DXOFF}	TXIN and $\overline{TXIN}$ toggling @ 1 MHz; TXIHB transitions from logic zero to one, see figure 6.			100	
Transmitter on; delay from inhibit active 13/	t_{DXON}	TXIN and $\overline{TXIN}$ toggling @ 1 MHz; TXIHB transitions from logic one to zero, see figure 6.			150	
Receiver off time	t_{RCVOFF}	See figure 6.			50	
Receiver on time	t_{RCVON}				50	
Receiver propagation delay	t_{RCVPD}				450	
Transmitter propagation delay	t_{XMITPD}				200	

1/ Device supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G and H of irradiation. However, this device only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ RXEN has ~1.2 µA pull up.
3/ Guaranteed by design but not tested.
4/ Guaranteed by device characterization. Capacitance is measured only for initial qualification and after any process or design changes which may affect input or output capacitance.
5/ Tested functionally.
6/ Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation test plan, section 5.1.2.2, Common Mode Rejection.
7/ Upper limit guaranteed by design but not tested.
8/ Guaranteed by device characterization.
9/ For MIL-STD-1760, Output voltage swing (V_O) = 20 $V_{P-P, L-L}$ min.
10/ Test in accordance with method described in MIL-STD-1553B output symmetry, section 4.5.2.1.1.4.
11/ Supplied as a design limit but not guaranteed or tested.
12/ Delay time from transmit inhibit (1.5 V) rising to transmit off (280 mV).
13/ Delay time from not transmit inhibit (1.5 V) falling to transmit on (1.2 V).

TABLE IB. SEP test limits. 1/ 2/

Device type	V_{DD} = 3.15 V 4/		Bias for latch-up test V_{DD} = 3.45 V no latch-up LET = 3/ [MeV/(mg/cm^2)]
	Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section (cm^2)	
All	5/	5/	≤111

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A. For SEP test conditions, see 4.4.4.4 herein.

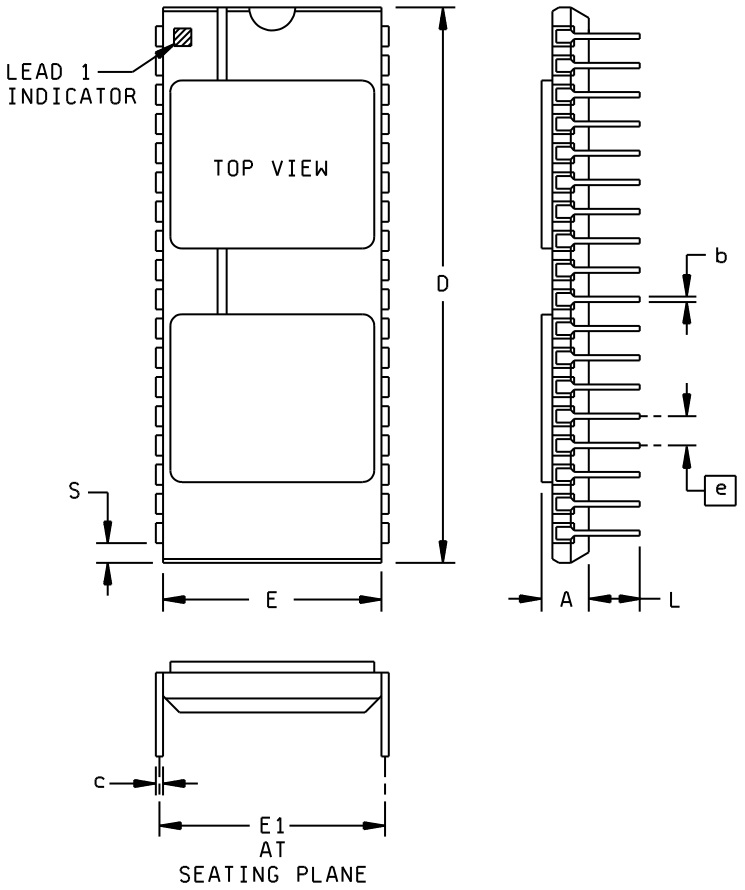
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature tested for latch up T_A = +125°C.

4/ Worst case temperature tested for upset T_A = 25°C ±10°C.

5/ This device has no memory storage elements to upset.

Case X

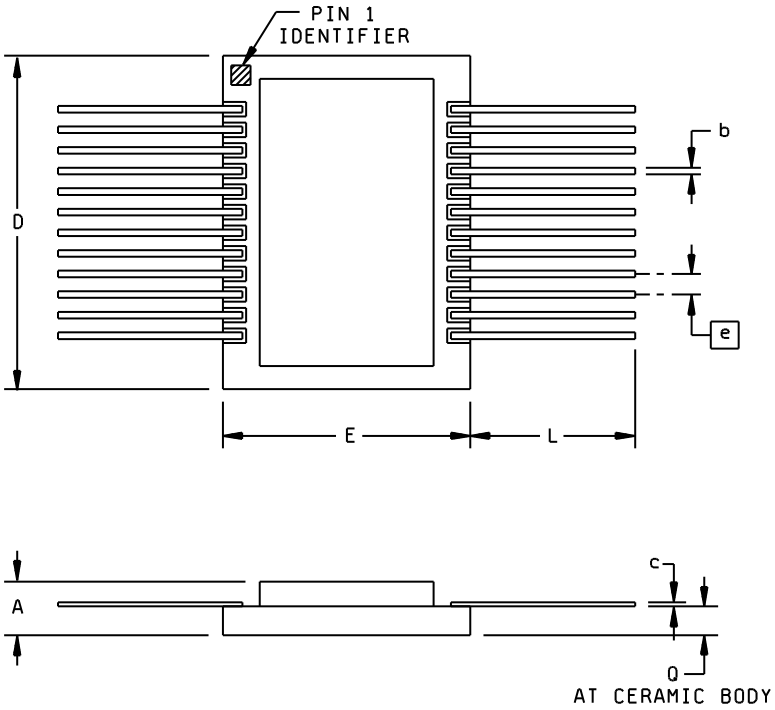


Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.155		3.94	E	.570	.610	14.48	15.49
b	.014	.023	0.36	0.58	E1	.590	.620	14.99	15.75
c	.008	.015	0.20	0.38	S	.005		0.13	
D		1.890		48.00	L	.150		3.81	
e	.100 BSC		2.54						

Notes:
1. Package material: opaque ceramic.
2. It is recommended that package ceramic be mounted on a heat removal rail in the printed circuit board. A thermally conductive material should be used.

FIGURE 1. Case outline.

Case Y



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		0.095		2.41
b	0.014	0.018	0.36	0.46
c	0.006	0.009	0.15	0.23
D	0.790	0.810	20.07	20.57
e	.050 BSC		1.27 BSC	
E	0.580	.600	14.73	15.24
L	.400		10.16	
Q	0.063	0.077	1.60	1.96

Notes:
3. Package material: opaque ceramic.
4. It is recommended that package ceramic be mounted on a heat removal rail in the printed circuit board. A thermally conductive material should be used.

FIGURE 1. Case outline - Continued.

Case X				
Terminal number	Terminal name		Terminal number	Terminal name
1	TXOUT	CHANNEL A	36	$\overline{\text{TXIN}}$
2	$\overline{\text{TXOUT}}$		35	TXIN
3	GND		34	TXIHB
4	NC		33	V_{DD}
5	RXOUT		32	NC
6	RXEN		31	GND
7	GND		30	$\overline{\text{RXIN}}$
8	$\overline{\text{RXOUT}}$		29	RXIN
9	NC		28	NC
10	TXOUT	CHANNEL B	27	$\overline{\text{TXIN}}$
11	$\overline{\text{TXOUT}}$		26	TXIN
12	GND		25	TXIHB
13	NC		24	V_{DD}
14	RXOUT		23	NC
15	RXEN		22	GND
16	GND		21	$\overline{\text{RXIN}}$
17	$\overline{\text{RXOUT}}$		20	RXIN
18	NC		19	NC

Case Y				
Terminal number	Terminal name		Terminal number	Terminal name
1	CHA	CHANNEL A	24	$\overline{\text{TXIN}}$
2	$\overline{\text{CHA}}$		23	TXIN
3	GND		22	TXIHB
4	RXOUT		21	GND
5	RXEN		20	V_{DD}
6	$\overline{\text{RXOUT}}$		19	GND
7	CHB	CHANNEL B	18	$\overline{\text{TXIN}}$
8	$\overline{\text{CHB}}$		17	TXIN
9	GND		16	TXIHB
10	RXOUT		15	GND
11	RXEN		14	V_{DD}
12	$\overline{\text{RXOUT}}$		13	GND

Note:
1. The 24 lead flatpack (case Y) internally connects TXOUT TO RXIN (CHA, CHB) and $\overline{\text{TXOUT}}$ to $\overline{\text{RXIN}}$ ($\overline{\text{CHA}}$, $\overline{\text{CHB}}$) for each channel.

FIGURE 2. Terminal connections.

TXIN	$\overline{\text{TXIN}}$	TXIHB	TXOUT
X	X	H	OFF 1/
L	L	X	OFF 2/
L	H	L	ON
H	L	L	ON
H	H	X	OFF 2/

Notes:
H = High
L = Low
X = Irrelevant.
1. Transmitter output terminals are in the non-transmitting mode during OFF time.
2. Transmitter output terminals are in the non-transmitting mode during OFF time, independent of TXIHB status.

FIGURE 3. Transmit operating mode.

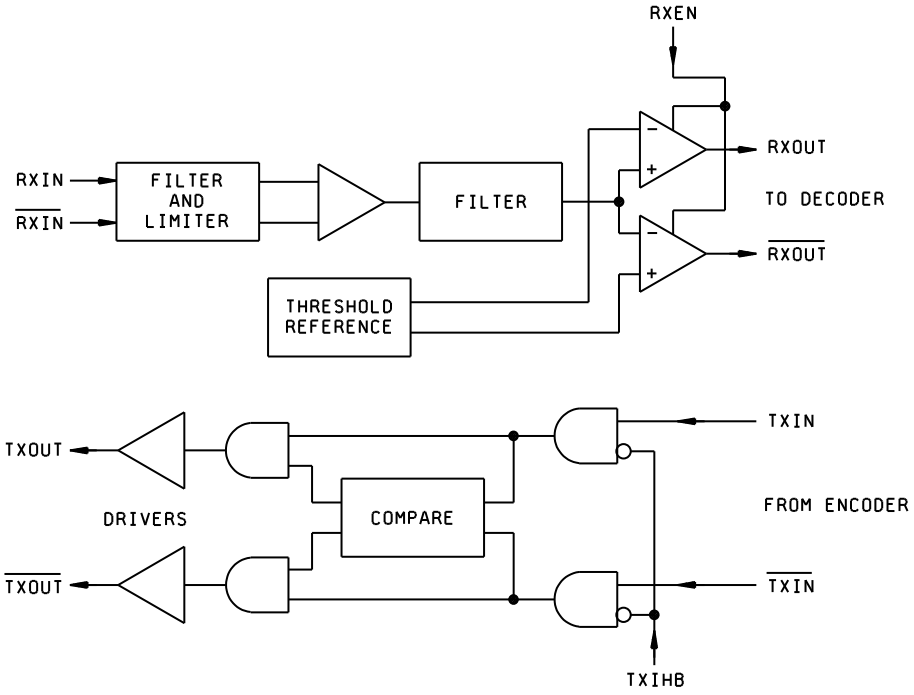
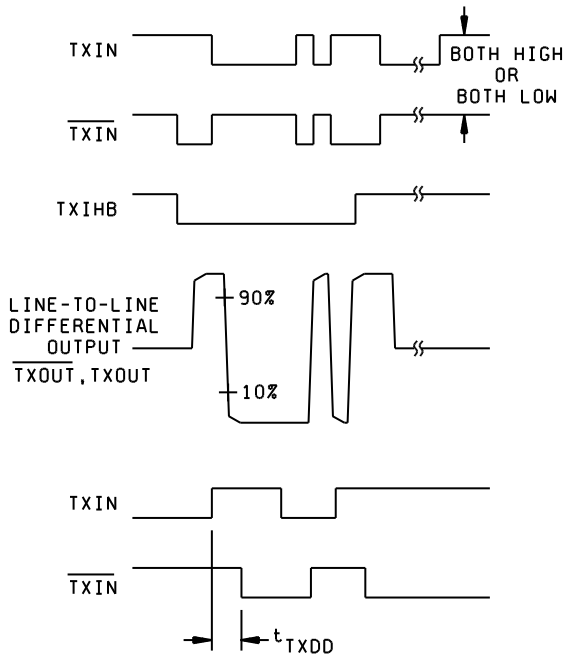
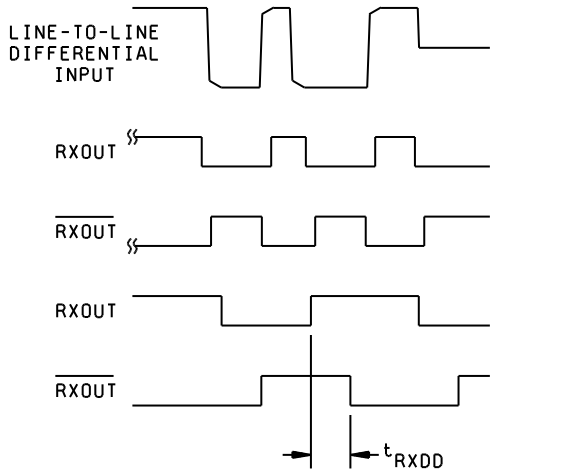


FIGURE 4. Block diagram.

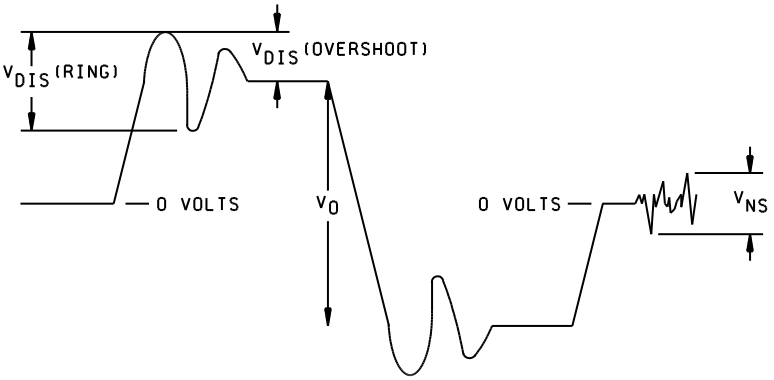


TYPICAL TRANSMITTER WAVE

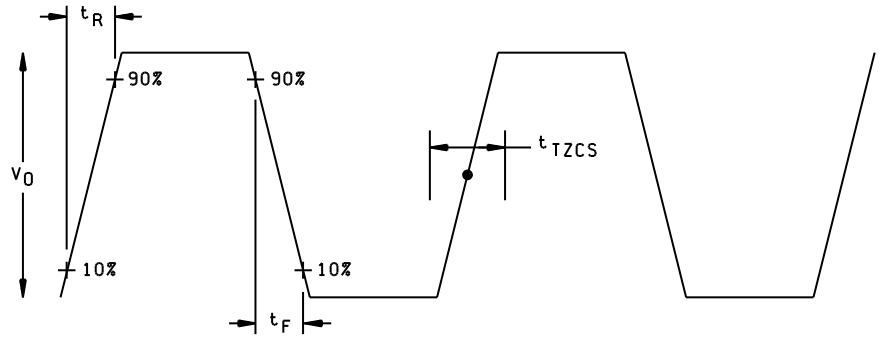


TYPICAL RECEIVER WAVEFORMS

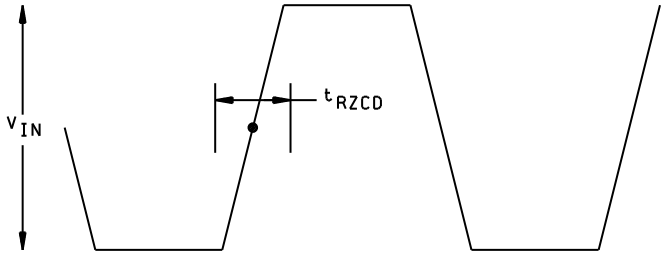
FIGURE 5. Typical transmitter and receiver waveforms.



TRANSMITTER OUTPUT CHARACTERISTICS (V_{DIS}, V_{NS}, V_O)

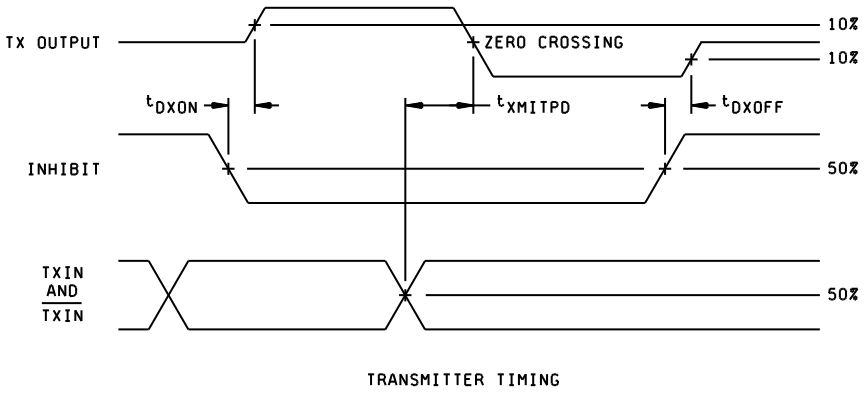


TRANSMITTER OUTPUT ZERO CROSSING STABILITY, RISE TIME, FALL TIME (t_{TZCS}, t_R, t_F)

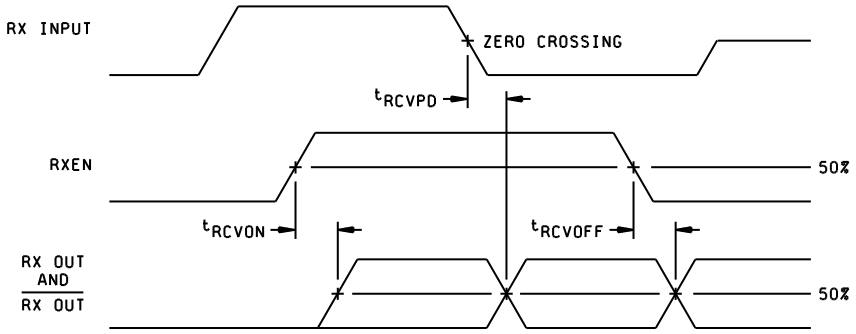


RECEIVER INPUT ZERO CROSSING DISTORTION (t_{RZCD})

FIGURE 6. Switching waveforms and test circuit.

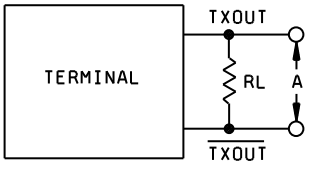


TRANSMITTER TIMING



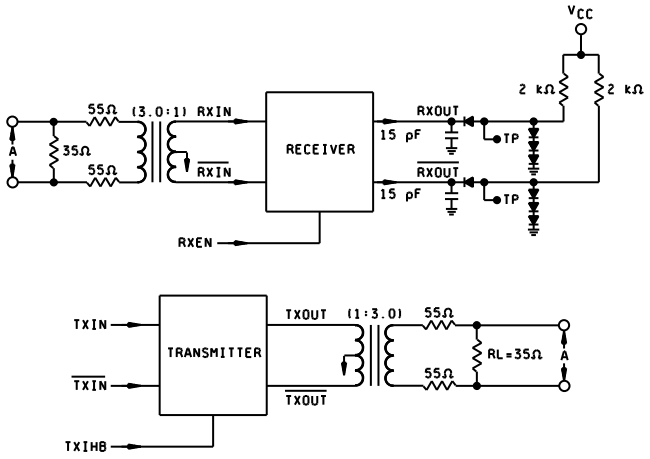
RECEIVER TIMING

FIGURE 6. Switching waveforms and test circuit – Continued.



Notes:
1. Direct coupled stub: Terminal is defined as transceiver plus isolation transformer and fault resistor. Point A is defined in figure 8
2. Transformer Coupled stub: Terminal is defined as transceiver plus isolation transformer. Point A is defined in figure 9.

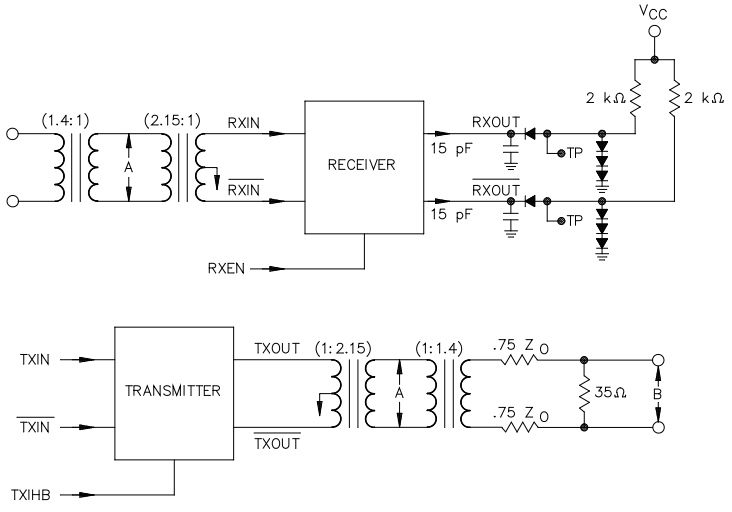
FIGURE 7. Transceiver test with load.



DIRECT COUPLED TRANSCEIVER WITH LOAD

Notes:
1. TP = test point.
2. RL removed for terminal input impedance test.
3. TXOUT and RXIN tied together. $\overline{\text{TXOUT}}$ AND $\overline{\text{RXIN}}$ tied together.

FIGURE 8. Transceiver test with load.



TRANSFORMER COUPLED TRANSCEIVER WITH LOAD

Notes:
1. TP = test point.
2. RL removed for terminal input impedance test.
3. TXOUT and RXIN tied together. $\overline{\text{TXOUT}}$ and $\overline{\text{RXIN}}$ tied together.

FIGURE 9. Transceiver test with load.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT}) shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. A minimum sample size of five devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8	1, 2, 3, 7, 8 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	1, 2, 7, 8A
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7 and deltas.
3/ Delta limits, as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Condition	Limits
Supply current	I_{DD}	T_A = 25°C 0% duty cycle	± 10% of measured value, or 300 µA whichever is greater

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \le$ angle $\le 60°$). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be $\ge$ 100 errors or $\ge 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\ge$ 20 micron in silicon.

e. The upset test temperature shall be +25°C. The latch-up test temperature shall be at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime, Columbus when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime Columbus will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

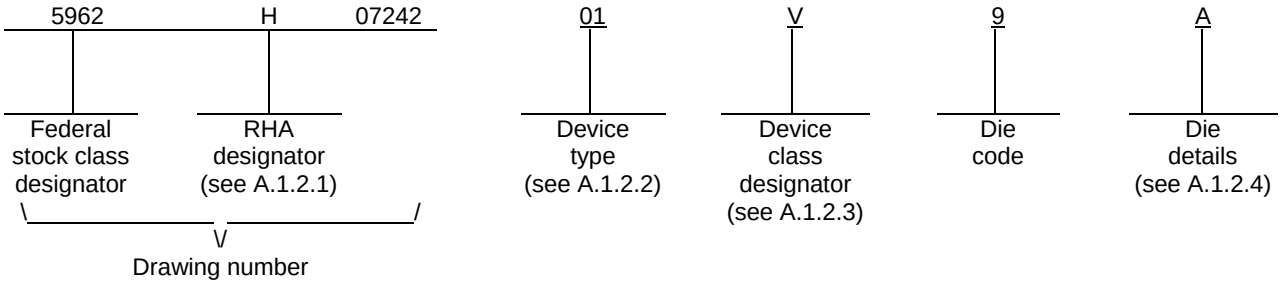
APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-07242

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT63M143	Dual channel, bus transceiver, TTL input/output, MIL-STD-1553 A/B compatible.
02	UT63M143	Dual channel, bus transceiver, TTL input/output, MIL-STD-1760 compatible.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

APPENDIX A FORMS A PART OF SMD 5962-07242

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

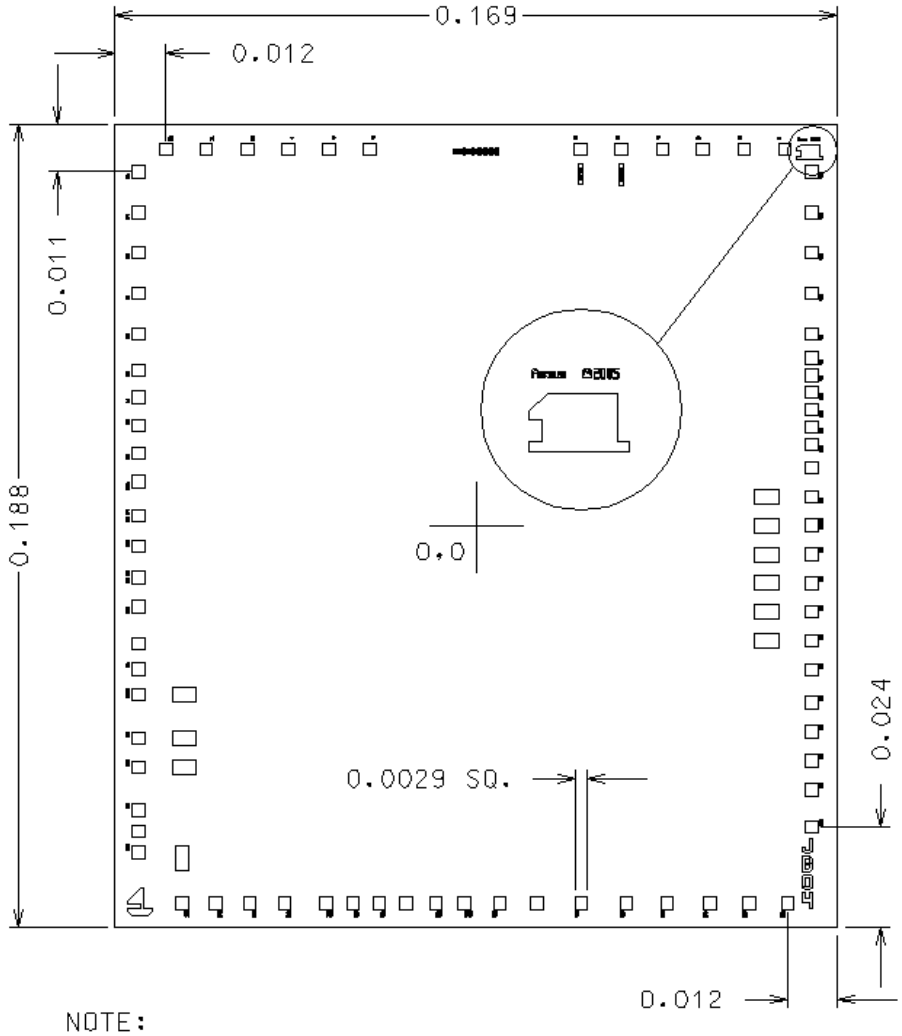
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.



NOTE:
1. SUBSTRATE IS VSS
2. DIMENSIONS ARE IN MILS.
3. DIE THICKNESS IS 17.5 ±0.5
4. DIE CENTER IS 0,0 COORDINATE.

DIEPAD LOCATION TABLE					
DP#	X	Y	DP#	X	Y
1	72.5	88.4	39	-35.2	-88.7
2	62.9	88.4	40	-29.0	-88.7
3	53.3	88.4	41	-22.8	-88.6
4	43.8	88.4	42	-16.4	-88.7
5	34.2	88.4	43	-9.4	-88.7
6	24.6	88.4	44	-2.9	-88.7
7	-25.0	88.4	45	5.7	-88.7
8	-34.5	88.4	46	14.3	-88.6
9	-44.1	88.4	47	24.8	-88.7
10	-53.7	88.4	48	35.3	-88.7
11	-63.3	88.4	49	44.8	-88.7
12	-72.8	88.4	50	54.9	-88.7
13	-79.2	83.1	51	64.1	-88.7
14	-79.2	73.6	52	73.1	-88.7
15	-79.2	64.1	53	78.9	-70.6
16	-79.2	54.6	54	78.9	-62.0
17	-79.2	45.0	55	78.9	-55.2
18	-79.2	36.4	56	78.9	-48.4
19	-79.2	30.2	57	78.9	-41.6
20	-79.2	23.5	58	78.9	-33.9
21	-79.2	17.0	59	78.9	-27.1
22	-79.2	10.3	60	78.9	-20.3
23	-79.2	2.4	61	78.9	-13.5
24	-79.2	-4.9	62	78.9	-6.8
25	-79.2	-12.1	63	78.9	0.1
26	-79.2	-19.1	64	78.9	6.9
27	-79.2	-27.7	65	78.9	13.6
28	-79.2	-33.6	66	78.9	19.1
29	-79.2	-39.7	67	78.9	23.2
30	-79.2	-49.9	68	78.9	27.2
31	-79.2	-56.7	69	78.9	31.3
32	-79.2	-66.7	70	78.9	35.4
33	-79.2	-71.6	71	78.9	39.5
34	-79.2	-76.6	72	78.9	45.0
35	-69.0	-88.7	73	78.9	54.6
36	-61.2	-88.7	74	78.9	64.1
37	-53.2	-88.7	75	78.9	73.6
38	-44.8	-88.7	76	78.9	83.1

Note: Pad numbers reflect terminal numbers when placed in case outlines X and Y (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	169 x 188 mils.
Die thickness:	17.5 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness:	9.0 k Ĺ – 12.5 k Ĺ
Backside metallization:	None

Glassivation.

Type:	PSG with Nitride
Thickness:	9.0 k Ĺ – 11.0 k Ĺ
Substrate:	V_{SS}

Assembly related information.

Substrate potential: Connect die attach pad to the V_{SS}.

Special assembly instructions: TXOUT and $\overline{\text{TXOUT}}$ bond out must be matched within 10 mΩ and have low resistance of less than 250 mΩ. V_{DD} bond out on bond pads 1, 2, 3, and 22, 23, 24 must be within 10 mΩ and low resistance of less than 250 mΩ

FIGURE A-1. Die bonding pad locations and electrical functions-Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN
DATE: 15-10-07

Approved sources of supply for SMD 5962-07242 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime-VA maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0724201Q9A	65342	UT63M143-Q DIE
5962-0724201QXA	65342	UT63M143-BQA
5962-0724201QXC	65342	UT63M143-BQC
5962-0724201QYA	65342	UT63M143-CQA
5962-0724201QYC	65342	UT63M143-CQC
5962-0724201V9A	65342	UT63M143-V DIE
5962-0724201VXA	65342	UT63M143-BVA
5962-0724201VXC	65342	UT63M143-BVC
5962-0724201VYA	65342	UT63M143-CVA
5962-0724201VYC	65342	UT63M143-CVC
5962-0724202Q9A	65342	UT63M143-Q DIE
5962-0724202QXA	65342	UT63M143-BQA
5962-0724202QXC	65342	UT63M143-BQC
5962-0724202QYA	65342	UT63M143-CQA
5962-0724202QYC	65342	UT63M143-CQC
5962-0724202V9A	65342	UT63M143-V DIE
5962-0724202VXA	65342	UT63M143-BVA
5962-0724202VXC	65342	UT63M143-BVC
5962-0724202VYA	65342	UT63M143-CVA
5962-0724202VYC	65342	UT63M143-CVC
5962H0724201Q9A	65342	UT63M143-Q DIE
5962H0724201QXA	65342	UT63M143-BQA
5962H0724201QXC	65342	UT63M143-BQC
5962H0724201QYA	65342	UT63M143-CQA
5962H0724201QYC	65342	UT63M143-CQC
5962H0724201V9A	65342	UT63M143-V DIE
5962H0724201VXA	65342	UT63M143-BVA
5962H0724201VXC	65342	UT63M143-BVC
5962H0724201VYA	65342	UT63M143-CVA
5962H0724201VYC	65342	UT63M143-CVC
5962H0724202Q9A	65342	UT63M143-Q DIE
5962H0724202QXA	65342	UT63M143-BQA
5962H0724202QXC	65342	UT63M143-BQC
5962H0724202QYA	65342	UT63M143-CQA
5962H0724202QYC	65342	UT63M143-CQC

See footnotes at end of table

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H0724202V9A	65342	UT63M143-V DIE
5962H0724202VXA	65342	UT63M143-BVA
5962H0724202VXC	65342	UT63M143-BVC
5962H0724202VYA	65342	UT63M143-CVA
5962H0724202VYC	65342	UT63M143-CVC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486