REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to meet current MIL-PRF-38535 requirements. - glg	16-11-04	Charles Saffle

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Kenneth Rice

DLA LAND AND MARITIME

COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Cheri Rida

APPROVED BY
Robert Heber

DRAWING APPROVAL DATE
09-01-27

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 128K x 16-BIT (2M), STATIC RANDOM ACCESS MEMORY (SRAM), (3.3 V), MONOLITHIC SILICON

REVISION LEVEL
A

SIZE	CAGE CODE	
A	**67268**	**5962-07235**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	07235	01	Q	X	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_____ _____/
\/
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01		128K x 16 CMOS SRAM	Yes	12 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	44	SO Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Voltage on any input relative to V_{SS}	-0.3 V dc to + 4.6 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	0.41 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	7° C/W 3/
Junction temperature (T_J)	+140°C 4/
Output current	20 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	3.0 V dc to 3.6 V dc
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	2.0 V dc to V_{CC} + 0.3 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 5/
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ Tested initially and after any design or process changes that may affect these parameters.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ V_{IL} (MIN) = -2.0 V dc and V_{IH}(MAX)= V_{CC} +2 V dc for pulse width less than 20 ns.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and Figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on Figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on Figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55C° ≤ T_C ≤ 125°C 3.0 V ≤ V_{CC} ≤ 3.6 V Unless Otherwise Specified	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Output HIGH Voltage	V_{OH}	V_{CC} = Min., I_{OH} = -4.0 mA	1, 2, 3	01	2.4		V
Output LOW Voltage	V_{OL}	V_{CC} = Min., I_{OL} = 8.0 mA	1, 2, 3	01		0.4	V
Input Leakage Current	I_{LK}	GND ≤ V_I ≤ V_{CC}	1, 2, 3	01	-1	+1	uA
Output Leakage Current	I_{OLK}	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	1, 2, 3	01	-1	+1	uA
V_{CC} Operating Supply Current	I_{CC}	V_{CC} = MAX f = f_{MAX} = 1/t_{RC}	1, 2, 3	01		90	mA
Automatic Power Down Current -TTL Inputs	I_{SB1}	MAX V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX}	1, 2, 3	01		20	mA
Automatic Power Down-Current - CMOS Inputs	I_{SB2}	MAX V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f=0	1, 2, 3	01		20	mA
Input Capacitance 1/	C_{IN}	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3 V	4	01		8	pF
Input /Output Capacitance 1/	C_{OUT}	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3 V	4	01		8	pF
V_{CC} for Data Retention	V_{DR}	2/	1, 2, 3	01	2.0		V
Data Retention Current	I_{CCDR}	V_{CC} = V_{DR} = 2.0 V $\overline{CE}$ ≥ V_{CC} – 0.3 V V_{IN} ≥ V_{CC}- 0.3 V or V_{IN} ≤ 0.3 V 2/	1, 2, 3	01		15	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55C° ≤ T_C ≤ 125°C 3.0 V ≤ V_{CC} ≤ 3.6 V Unless Otherwise Specified	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Read Cycle Time	t_{RC}	See figure 5 as applicable. 3/ 4/	9, 10, 11	01	12		ns
Address to Data Valid	t_{AA}		9, 10, 11	01		12	ns
Data Hold from Address Change	t_{OHA}		9, 10, 11	01	3		ns
$\overline{CE}$ LOW to Data Valid	t_{ACE}		9, 10, 11	01		12	ns
$\overline{OE}$ LOW to Data Valid	t_{DOE}		9, 10, 11	01		6	ns
$\overline{OE}$ LOW to Low Z 5/ 6/	t_{LZOE}		9, 10, 11	01	0		ns
$\overline{OE}$ HIGH to High Z 5/ 6/ 7/	t_{HZOE}		9, 10, 11	01		6	ns
$\overline{CE}$ LOW to Low Z 5/ 6/	t_{LZCE}		9, 10, 11	01	3		ns
$\overline{CE}$ HIGH to High Z 5/ 6/ 7/	t_{HZCE}		9, 10, 11	01		6	ns
Byte Enable to Data Valid	t_{DBE}		9, 10, 11	01		6	ns
Byte Enable to Low Z 5/ 6/	t_{LZBE}		9, 10, 11	01	0		ns
Byte Enable to High Z 5/ 6/ 7/	t_{HZBE}		9, 10, 11	01		6	ns
Write Cycle Time 8/ 9/	t_{WC}		9, 10, 11	01	12		ns
$\overline{CE}$ LOW to Write End	t_{SCE}		9, 10, 11	01	8		ns
Address Set-Up to Write End	t_{AW}		9, 10, 11	01	8		ns
Address Hold from Write End	t_{HA}		9, 10, 11	01	0		ns
Address Set-Up to Write Start	t_{SA}		9, 10, 11	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55C° ≤ T_C ≤ 125°C 3.0 V ≤ V_{CC} ≤ 3.6 V Unless Otherwise Specified	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
$\overline{WE}$ Pulse Width	t_{PWE}	See figure 5 as applicable. 3/ 4/	9, 10, 11	01	8		ns
Data Set-Up to Write End 9/	t_{SD}		9, 10, 11	01	5.5		ns
Data Hold from Write End	t_{HD}		9, 10, 11	01	0		ns
$\overline{WE}$ HIGH to Low Z 5/ 6/ 9/	t_{LZWE}		9, 10, 11	01	3		ns
$\overline{WE}$ LOW to High Z 5/ 6/ 7/ 9/	t_{HZWE}		9, 10, 11	01		6	ns
Byte Enable to End of Write	t_{BW}		9, 10, 11	01	8		ns
Chip Deselect to Data Retention Time 1/ 6/	t_{DCR}	$V_{CC} = V_{DR} = 2.0$ V $\overline{CE} \geq V_{CC} - 0.3$V $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V 2/ 3/ 4/	9, 10, 11	01	0		ns
Operation Recovery Time 6/ 10/	t_R		9, 10, 11	01	t_{RC}		ns

1/ Tested initially and after any design or process changes that may affect these parameters.

2/ No input may exceed V_{CC} + 0.3 V.

3/ Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

4/ AC characteristics (except High-Z) are tested using the load conditions shown in Figure 4 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 4 (b).

5/ At a given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.

6/ Parameter, if not tested, shall be guaranteed to the limits specified in Table I.

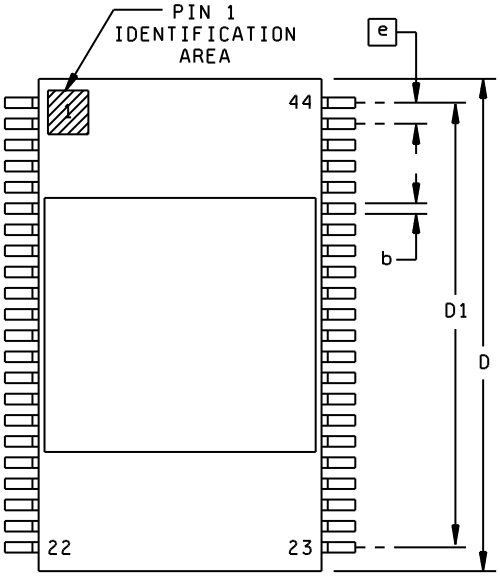
7/ t_{HZOE} , t_{HZCE} , t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5pF as in Figure 4 (b). Transition is measured when the outputs enter a high impedance state.

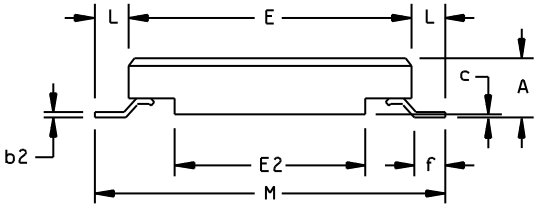
8/ The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

9/ The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

10/ Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(MIN)≥ 50 us or stable at V_{CC}(MIN)≥ 50 us.

Case X (see note)





Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.986	3.842	E	9.96	10.36
b	0.300	0.400	E2	5.280	5.680
b2	.150	.250	e	0.80 BSC	
c	0.05	---	f	.406	.597
D	18.215	18.615	L	.839 NOM (ref)	
D1	16.60	17.00	M	11.735	11.938
N	44				

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outlines.

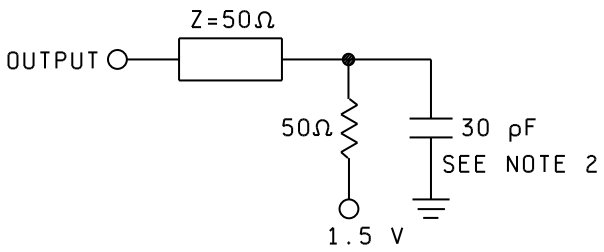
Device Type - All			
Case Outline X			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	A_4	23	NC
2	A_3	24	A_{11}
3	A_2	25	A_{10}
4	A_1	26	A_9
5	A_0	27	A_8
6	$\overline{CE}$	28	NC
7	I/O_O	29	I/O_8
8	I/O_1	30	I/O_9
9	I/O_2	31	I/O_{10}
10	I/O_3	32	I/O_{11}
11	V_{CC}	33	V_{CC}
12	V_{SS}	34	V_{SS}
13	I/O_4	35	I/O_{12}
14	I/O_5	36	I/O_{13}
15	I/O_6	37	I/O_{14}
16	I/O_7	38	I/O_{15}
17	$\overline{WE}$	39	$\overline{BLE}$
18	A_{16}	40	$\overline{BHE}$
19	A_{15}	41	$\overline{OE}$
20	A_{14}	42	A_7
21	A_{13}	43	A_6
22	A_{12}	44	A_5

FIGURE 2. Terminal connections.

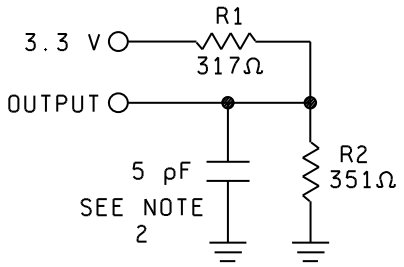
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0 – I/O_7$	I/O_8-I/O_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

FIGURE 3. Truth Table.

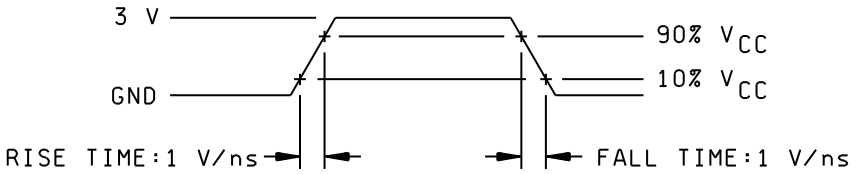


CIRCUIT A



CIRCUIT B

ALL INPUT PULSES



AC test conditions

Input pulse levels	VSS to 3.0 V
Input rise, fall times	3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

NOTES:
1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{HZCE}, t_{HZWE}, and t_{HZOE}

FIGURE 4. Output load circuits.

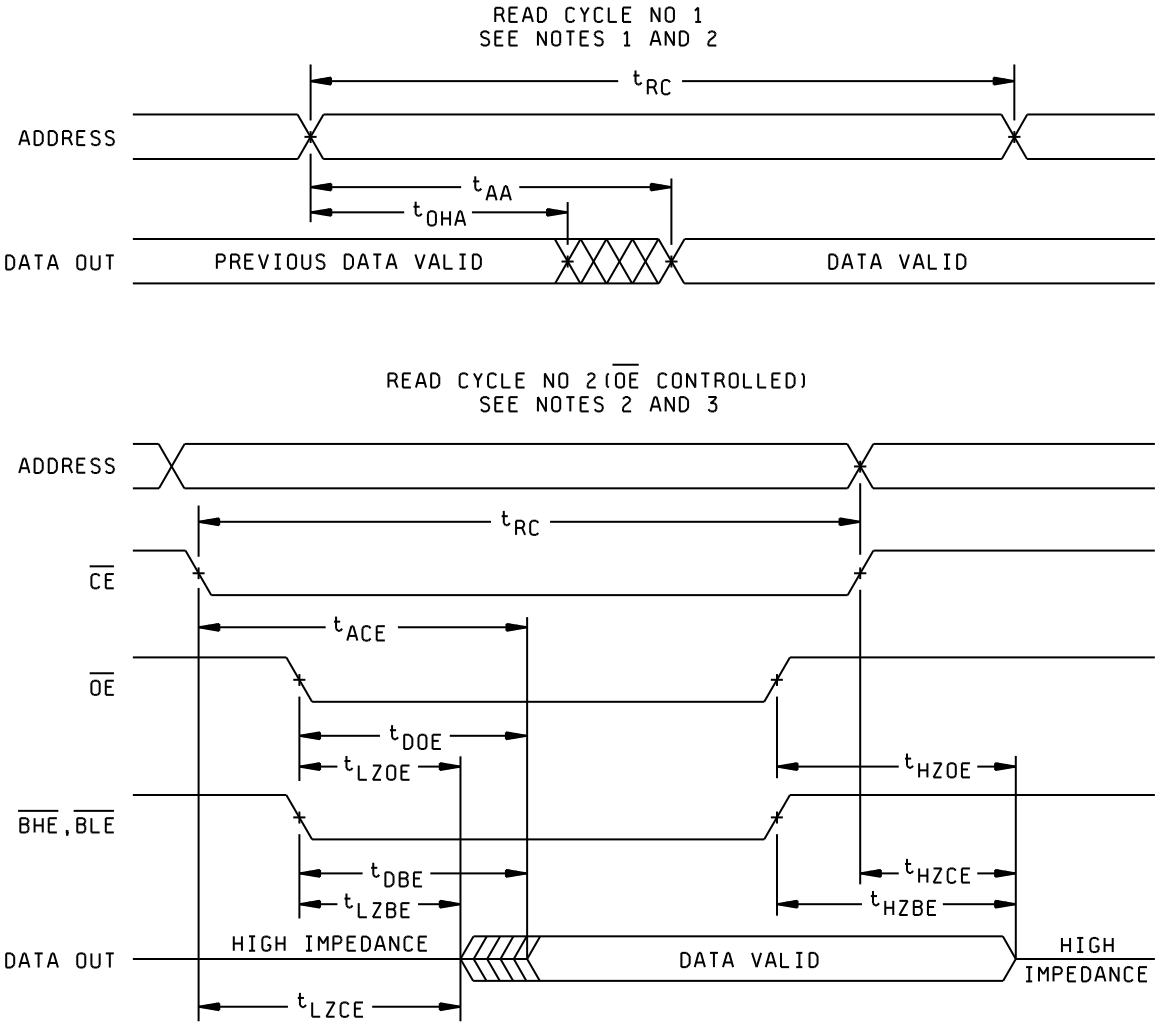
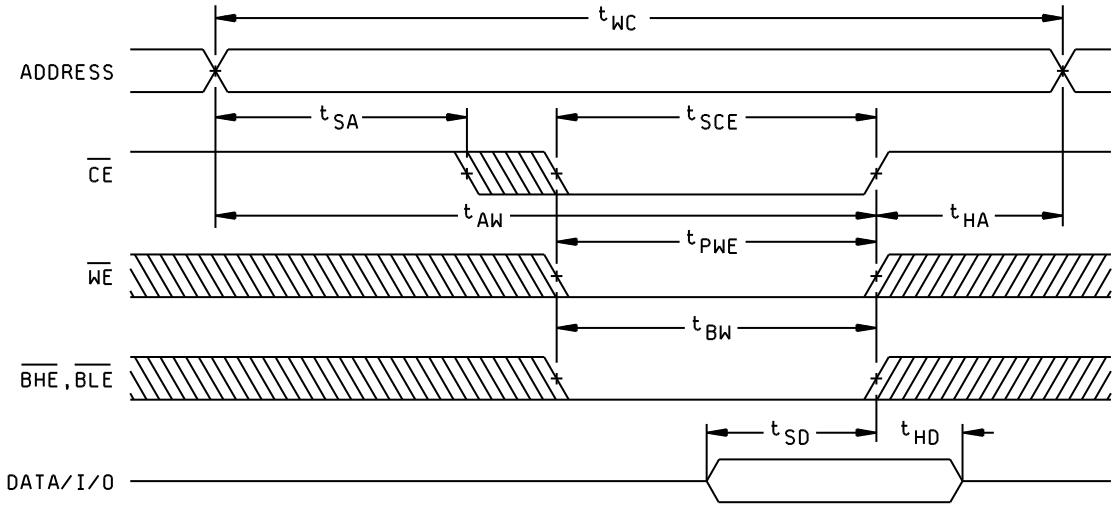


FIGURE 5. Timing waveforms.

WRITE CYCLE NO 1 ($\overline{CE}$ CONTROLLED)
SEE NOTES 4 AND 5



WRITE CYCLE NO 2 ($\overline{BLE}$ OR $\overline{BHE}$ CONTROLLED)

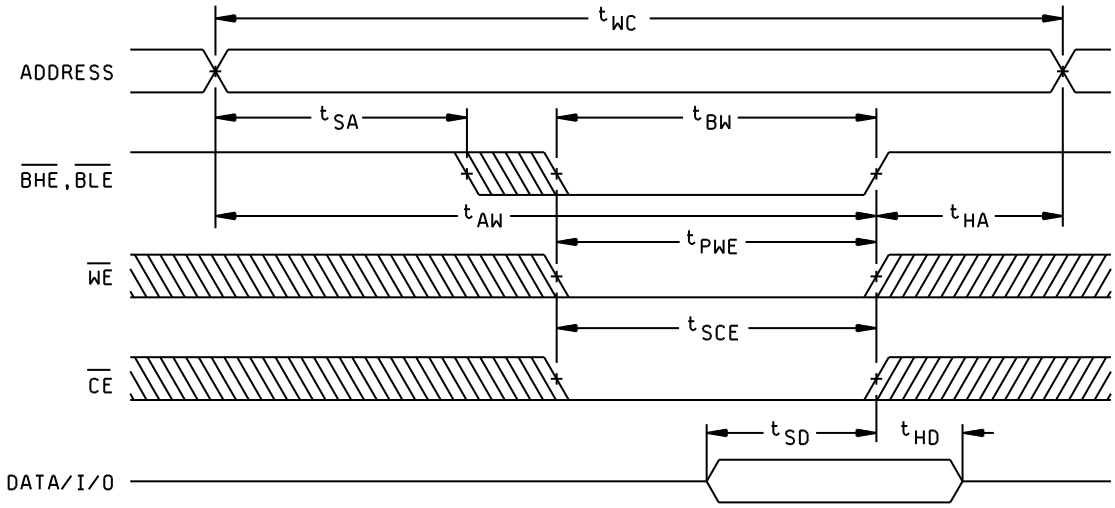
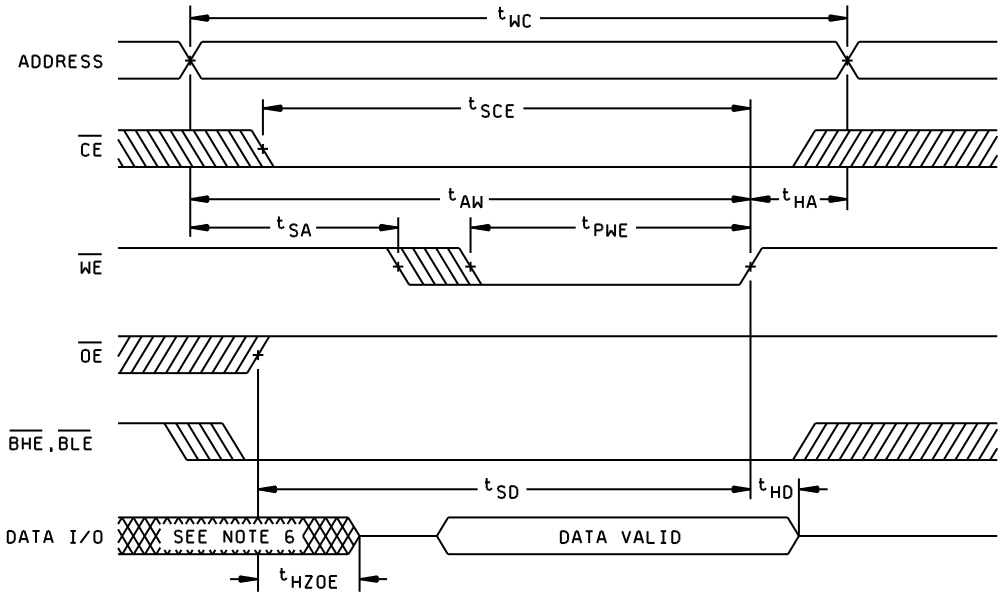


FIGURE 5. Timing waveforms - continued.

WRITE CYCLE NO 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ HIGH DURING WRITE)
SEE NOTES 4 AND 5



WRITE CYCLE NO 4 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW)

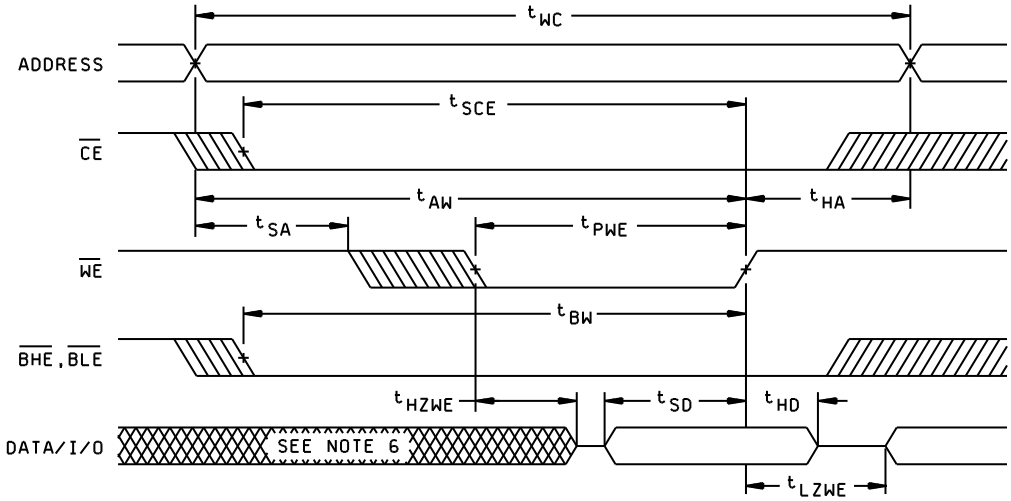
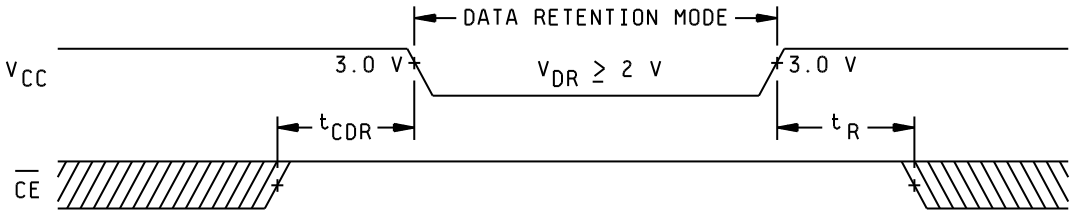


FIGURE 5. Timing waveforms - continued.

DATA RETENTION WAVEFORM



Notes:

1. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
2. $\overline{WE}$ is HIGH for read cycle.
3. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
4. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
5. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
6. During this period the I/Os are in the output state and input signals should not be applied.

FIGURE 5. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I_{SB2} standby	±10% of specified value in table I
I_{ILK}, I_{OLK}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

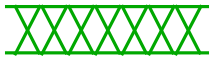
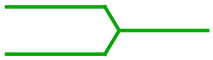
6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A

Appendix A forms a part of SMD 5962-07235

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 3.2.7 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-11-04

Approved sources of supply for SMD 5962-07235 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0723501QXA	6S055	DPA71011DV3302A
5962-0723501QXC	6S055	DPA71011DV3302C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
6S055	DPA Components International 2251 Ward Avenue Simi Valley, CA 93065

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.