REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make a correction to the clock frequency limit from 8.0 MHz to 0.8 MHz as specified under paragraph 1.4 and figure 1. Make a correction to f_{SCLK} limit from 8.0 MHz to 0.8 MHz in footnotes 2/ and 3/ as specified under Table IA. Make clarification to footnote 1/ as specified under Table IIB. - ro	09-10-27	C. SAFFLE
B	Add case outline F, paragraph 3.1.1, and Appendix A for microcircuit die. Delete references to device class M requirements. - ro	15-10-23	C. SAFFLE
C	Under paragraph 1.5, footnote 6/, delete the effective dose rate of "0.16 rad(Si)/s" and substitute "0.027 rad(Si)/s". Add glassification and substrate information under figure A-1. - ro	16-11-30	C. SAFFLE
D	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	22-08-24	J. ESCHMEYER

Revision Status of Sheets

REV	D	D	D	D	D																		
SHEET	24	25	26	27	28																		
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RICK OFFICER CHECKED BY RAJESH PITHADIA	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**		
	APPROVED BY ROBERT M. HEBER DRAWING APPROVAL DATE 09-03-11	MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 8 CHANNEL, 50 kSPS TO 1 MSPS, 12 BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON		
AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-07227**
		SHEET 1 OF 28		

DSCC FORM 2233
APR 97

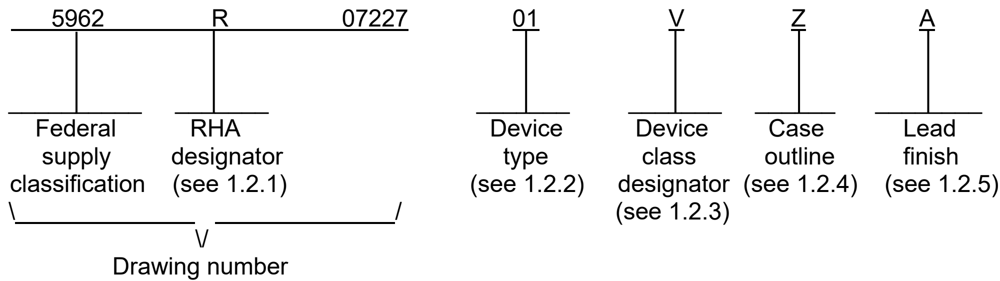
5962-E442-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC128S102	Radiation hardened, CMOS, 8 channel, 50 kSPS to 1 MSPS, 12 bit analog to digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
Z	GDFP1-G16	16	Flat pack with gullwing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Analog supply voltage (V_A)	-0.3 V to 6.5 V
Digital supply voltage (V_D)	-0.3 V to V_A + 0.3 V 6.5 V maximum
Voltage on any pin to GND	-0.3 V to V_A + 0.3 V
Input current at any pin	±10 mA 2/
Power dissipation (P_D) at T_A = +25°C	1.181 W 3/
Package input current	±20 mA 2/
Electrostatic susceptibility: 4/	
Human body model (HBM)	8,000 V
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) :	
Cases F and Z	11.2°C/W
Thermal resistance, junction-to-ambient (θ_{JA}) :	
Cases F and Z	127°C/W

1.4 Recommended operating conditions.

V_A supply voltage	+2.7 V to +5.25 V
V_D supply voltage	+2.7 V to V_A
Digital input voltage	0 V to V_A
Analog input voltage	0 V to V_A
Clock frequency	0.8 MHz to 16 MHz
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ When the input voltage at any pin exceeds the power supplies ($V_{IN} < AGND$ or $V_{IN} > V_A$ or V_D), current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

3/ The absolute maximum junction temperature (T_J max) for this device is 175°C. The maximum allowable power dissipation is dictated by T_J max, the junction to ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), can be calculated using the formula $P_DMAX = (T_JMAX – T_A) / \theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed).

4/ Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 200 pF discharged through 0 Ω.

1.4.1 Operating performance characteristics. 5/

Full power bandwidth (FPBW) (-3 dB):

$V_A = V_D = +3.0$ V .... 6.8 MHz

$V_A = V_D = +5.0$ V .... 10 MHz

Channel to channel isolation (ISO):

$V_A = V_D = +3.0$ V .... 84 dB

$V_A = V_D = +5.0$ V .... 85 dB

Input voltage range (V_{IN}) .... 0 to V_A

Input capacitance (C_{INA}):

Track mode .... 38 pF

Hold mode .... 4.5 pF

Digital input capacitance (C_{IND}) .... 3.5 pF maximum

High impedance output capacitance (C_{OUT}) .... 3.5 pF maximum

Output coding .... Straight natural binary

SCLK duty cycle (DC) .... 30 %
70 %

Aperture delay (t_D) .... 4 ns

SCLK high time (t_{CH}) .... 0.4 x t_{SCLK} ns minimum

SCLK low time (t_{CL}) .... 0.4 x t_{SCLK} ns minimum

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si) / s) .... 100 krads(Si) 6/

Single event latch-up (SEL) .... ≥ 120 MeV-cm^2/mg 7/

______

5/ These represent performance characteristics of the device and are not guaranteed through test.

6/ Device type 01 is irradiated at dose rate = 50 - 300 rads(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 0.027 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

7/ Limits are based on characterization, but not production tested unless specified on the purchase order or contract. See table IB.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figures 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Static converter characteristics 2/							
Resolution with no missing codes			1,2,3	01		12	Bits
Integral non linearity	INL	V_A = V_D = +3.0 V	1,2,3	01	-1.0	+1.1	LSB
(end point method)		V_A = V_D = +5.0 V			-1.25	+1.4	
Differential non linearity	DNL	V_A = V_D = +3.0 V	1,2,3	01		+0.9	LSB
					-0.7		
		V_A = V_D = +5.0 V				+1.5	
					-0.9		
Offset error	V_{OFF}	V_A = V_D = +3.0 V	1,2,3	01	-2.3	+2.3	LSB
		V_A = V_D = +5.0 V			-2.3	+2.3	
Offset error match	OEM	V_A = V_D = +3.0 V	1,2,3	01	-1.5	+1.5	LSB
		V_A = V_D = +5.0 V			-1.5	+1.5	
Full scale error	FSE	V_A = V_D = +3.0 V	1,2,3	01	-2.0	+2.0	LSB
		V_A = V_D = +5.0 V			-2.0	+2.0	
Full scale error match	FSEM	V_A = V_D = +3.0 V	1,2,3	01	-1.5	+1.5	LSB
		V_A = V_D = +5.0 V			-1.5	+1.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic converter characteristics 2/							
Signal to noise plus distortion ratio	SINAD	$V_A = V_D = +3.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS	4,5,6	01	68		dB
		$V_A = V_D = +5.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS			68		
Signal to noise ratio	SNR	$V_A = V_D = +3.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS	4,5,6	01	69		dB
		$V_A = V_D = +5.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS			68.5		
Total harmonic distortion	THD	$V_A = V_D = +3.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS	4,5,6	01		-74	dB
		$V_A = V_D = +5.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS				-74	
Spurious free dynamic range	SFDR	$V_A = V_D = +3.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS	4,5,6	01	75		dB
		$V_A = V_D = +5.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS			75		
Effective number of bits	ENOB	$V_A = V_D = +3.0$ V, f_{IN} = 40.2 kHz	4,5,6	01	11.1		Bits
		$V_A = V_D = +5.0$ V, f_{IN} = 40.2 kHz, -0.02 dBFS			11.1		
Intermodulation distortion, second order terms	IMD	$V_A = V_D = +3.0$ V, f_a = 19.5 kHz, f_b = 20.5 kHz	4,5,6	01		-78	dB
		$V_A = V_D = +5.0$ V, f_a = 19.5 kHz, f_b = 20.5 kHz				-78	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Lints		Unit
					Min	Max	
Dynamic converter characteristics - continued 2/							
Intermodulation distortion, third order terms	IMD	V_A = V_D = +3.0 V, f_a = 19.5 kHz, f_b = 20.5 kHz	4,5,6	01		-70	dB
		V_A = V_D = +5.0 V, f_a = 19.5 kHz, f_b = 20.5 kHz				-70	
Analog input characteristics 2/							
DC leakage current			1,2,3	01		±1.0	µA
Digital input characteristics 3/							
Input high voltage	V_{IH}	V_A = V_D = +2.7 V to +3.6 V	1,2,3	01	2.1		V
		V_A = V_D = +4.75 V to +5.25 V			2.4		
Input low voltage	V_{IL}	V_A = V_D = +2.7 V to +5.25 V	1,2,3	01		0.8	V
Input current	I_{IN}	V_{IN} = 0 V or V_D	1,2,3	01		±1.0	µA
Digital output characteristics 3/							
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA, V_A = V_D = +2.7 V to +5.25 V	1,2,3	01	V_D – 0.5		V
Output low voltage	V_{OL}	I_{SINK} = 200 µA to 1.0 mA, V_A = V_D = +2.7 V to +5.25 V	1,2,3	01		0.4	V
High impedance output leakage current	I_{OZH}, I_{OZL}	V_A = V_D = +2.7 V to +5.25 V	1,2,3	01		±1.0	µA
		V_A = V_D = +2.7 V to +5.25 V M,D,P,L,R	1			±10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply characteristics 2/		C_L = 10 pF					
Analog and digital supply voltages	V_A, V_D	$V_A \geq V_D$	1,2,3	01	2.7		V
						5.25	
Total supply current normal mode ($\overline{CS}$ low)	$I_A + I_D$	$V_A = V_D$ = +2.7 V to +3.6 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	1,2,3	01		1.5	mA
		$V_A = V_D$ = +4.75 V to +5.25 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz				3.1	
Total supply current shutdown mode ($\overline{CS}$ high)	$I_A + I_D$	$V_A = V_D$ = +2.7 V to +3.6 V, f_{SCLK} = 0 kSPS	1,2,3	01		1.0	µA
		$V_A = V_D$ = +2.7 V to +3.6 V, f_{SCLK} = 0 kSPS, M,D,P,L,R	1			30	
		$V_A = V_D$ = +4.75 V to +5.25 V, f_{SCLK} = 0 kSPS	1,2,3			1.4	
		$V_A = V_D$ = +4.75 V to +5.25 V, f_{SCLK} = 0 kSPS, M,D,P,L,R	1			100	
Power consumption normal mode ($\overline{CS}$ low)	PC	$V_A = V_D$ = +3.0 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	1,2,3	01		4.5	mW
		$V_A = V_D$ = +5.0 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz				15.5	
Power consumption shutdown mode ($\overline{CS}$ high)	PC	$V_A = V_D$ = +3.0 V, f_{SCLK}= 0 kSPS	1,2,3	01		3.0	µW
		$V_A = V_D$ = +5.0 V, f_{SCLK} = 0 kSPS				7.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC electrical characteristics 3/							
Minimum clock frequency	$f_{SCLK\ MIN}$	$V_A = V_D = +2.7$ V to +5.25 V	9,10,11	01	0.8		MHz
Maximum clock frequency	$f_{SCLK\ MAX}$	$V_A = V_D = +2.7$ V to +5.25 V	9,10,11	01		16	MHz
Sample rate continuous mode	f_S	$V_A = V_D = +2.7$ V to +5.25 V	9,10,11	01	50		kSPS
						1	MSPS
Conversion (hold) time	$t_{CONVERT}$	$V_A = V_D = +2.7$ V to +5.25 V	9,10,11	01		13	SCLK cycles
Acquisition (track) time	t_{ACQ}	$V_A = V_D = +2.7$ V to +5.25 V, see figure 3	9,10,11	01		3	SCLK cycles
Throughput time		Acquisition time + conversion time, $V_A = V_D = +2.7$ V to +5.25 V	9,10,11	01		16	SCLK cycles

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing specification section 3/		See figure 3					
$\overline{CS}$ hold time after SCLK rising edge	t_{CSH}	4/	9,10,11	01	10		ns
$\overline{CS}$ setup time prior SCLK rising edge	t_{CSS}	4/	9,10,11	01	10		ns
$\overline{CS}$ falling edge to DOUT enabled	t_{EN}		9,10,11	01		30	ns
DOUT access time after SCLK falling edge	t_{DACC}		9,10,11	01		27	ns
DOUT hold time after SCLK falling edge	t_{DHLD}		9,10,11	01	11		ns
DIN setup time prior to SCLK rising edge	t_{DS}		9,10,11	01	10		ns
DIN hold time after SCLK rising edge	t_{DH}		9,10,11	01	10		ns
$\overline{CS}$ rising edge to DOUT high impedance	t_{DIS}	DOUT falling	9,10,11	01		20	ns
		DOUT rising				20	

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Unless otherwise specified, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF.

3/ Unless otherwise specified, $V_A = V_D$ = +2.7 V to +5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF.

4/ Clock may be in any state (high or low) when $\overline{CS}$ goes high. Setup and hold time restrictions apply only to $\overline{CS}$ going low.

TABLE IB. SEP test limits. 1/ 2/

Device type	Single event latch-up	Temperature (T_C)	V_{CC}	Effective linear energy transfer (LET)
01	SEL	+125°C	5.25 V	≥ 120 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

Device types	01
Case outlines	F and Z
Terminal number	Terminal symbol
1	$\overline{CS}$
2	V_A
3	AGND
4	INPUT 0
5	INPUT 1
6	INPUT 2
7	INPUT 3
8	INPUT 4
9	INPUT 5
10	INPUT 6
11	INPUT 7
12	DGND
13	V_D
14	DIN
15	DOUT
16	SCLK

FIGURE 1. Terminal connections.

Terminal symbol	Description
	Analog I / O
INPUT 0 – INPUT 7	Analog inputs. These signals can range from 0 V to V_{REF}.
	Digital I / O
SCLK	Digital clock input. The guaranteed performance range of frequencies for this input is 0.8 MHz to 16 MHz. This clock directly controls are conversion and readout processes.
DOUT	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
DIN	Digital data input. The device's control register is loaded through this pin on rising edges of the SCLK pin.
$\overline{CS}$	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
	Power supply
V_A	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7 V to +5.25 V source and bypassed to GND with 1 μF and 0.1 μF monolithic ceramic capacitors located within 1 centimeter of the power pin.
V_D	Positive digital supply pin. This pin should be connected to a +2.7 V to V_A supply, and bypassed to GND with a 0.1 μF monolithic ceramic capacitor located within 1 centimeter of the power pin.
AGND	The ground return for the analog supply and signals.
DGND	The ground return for the digital supply and signals.

FIGURE 1. Terminal connections – continued.

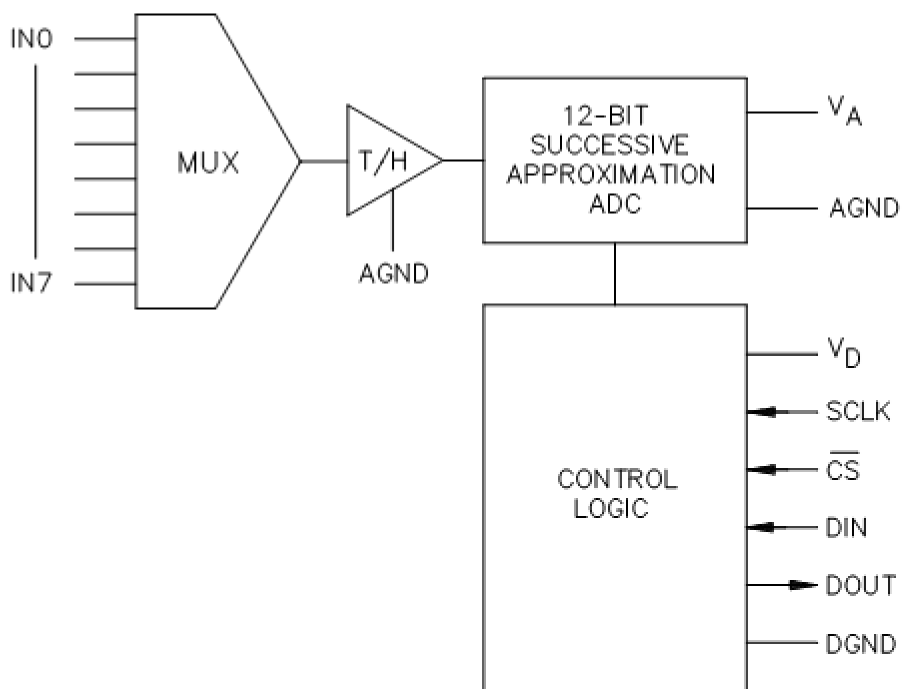
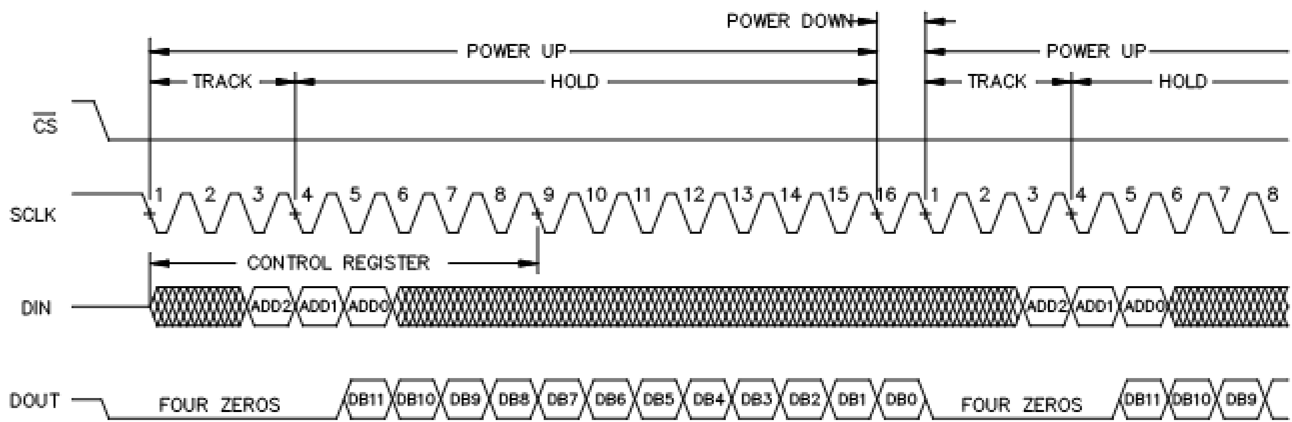


FIGURE 2. Block diagram.



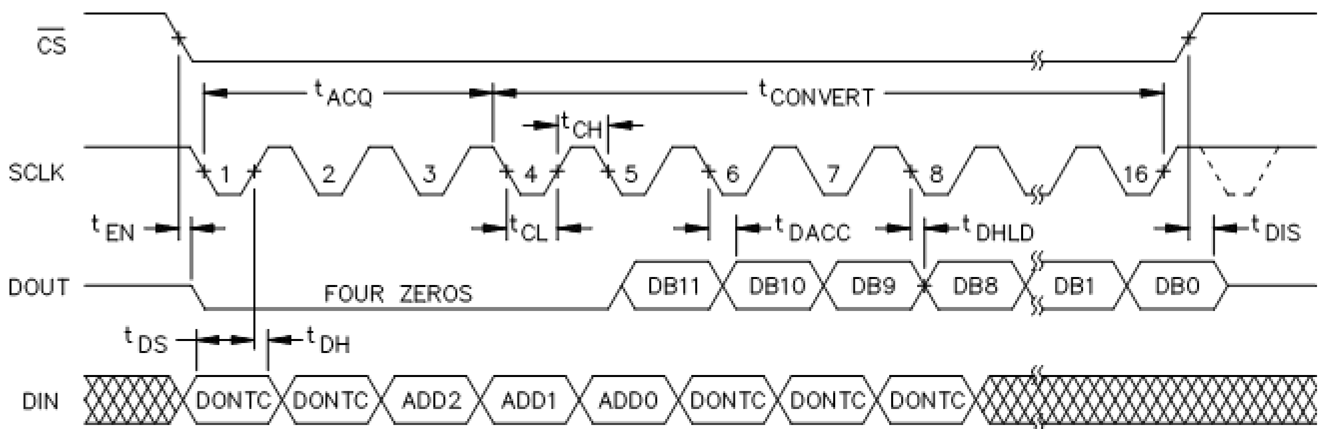


FIGURE 3. Timing waveforms.

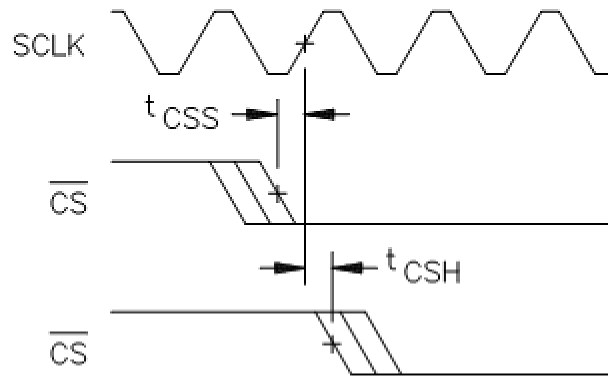


FIGURE 3. Timing waveforms – continued.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 9,10,11	1,2,3,4, 1/ 2/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4, 2/ 5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C 1/

Parameters	Symbol	Conditions	Delta limits		Units
			Min	Max	
Integral non-linearity	INL	$V_A = V_D$ = +3.0 V	-0.5	+0.5	LSB
		$V_A = V_D$ = +5.0 V	-0.35	+0.35	
Intermodulation distortion, second order terms	IMD	$V_A = V_D$ = +3.0 V	-14	+14	dB
		$V_A = V_D$ = +5.0 V	-17	+17	
Intermodulation distortion, third order terms	IMD	$V_A = V_D$ = +3.0 V	-10	+10	dB
		$V_A = V_D$ = +5.0 V	-10	+10	

1/ This is worse case drift, delta are performed at room temperature post operational life. All other parameters, no deltas are required.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature +125°C.

f. Bias conditions shall be V_{CC} = 5.25 V for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

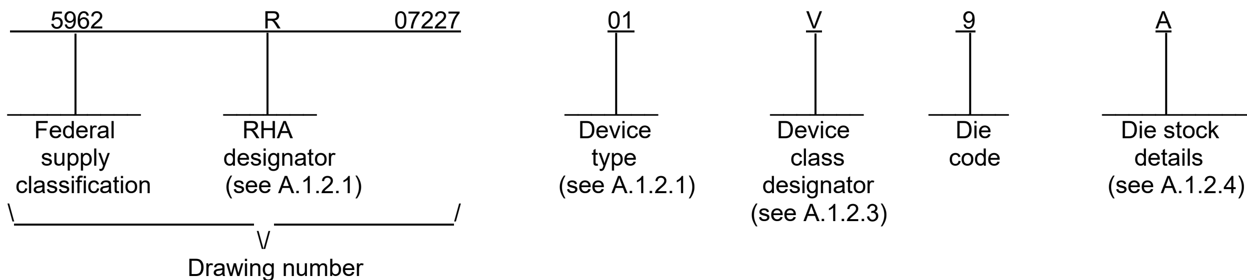
b. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-07227

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC128S102	Radiation hardened, CMOS, 8 channel, 50 kSPS to 1 MSPS, 12 bit analog to digital converter

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

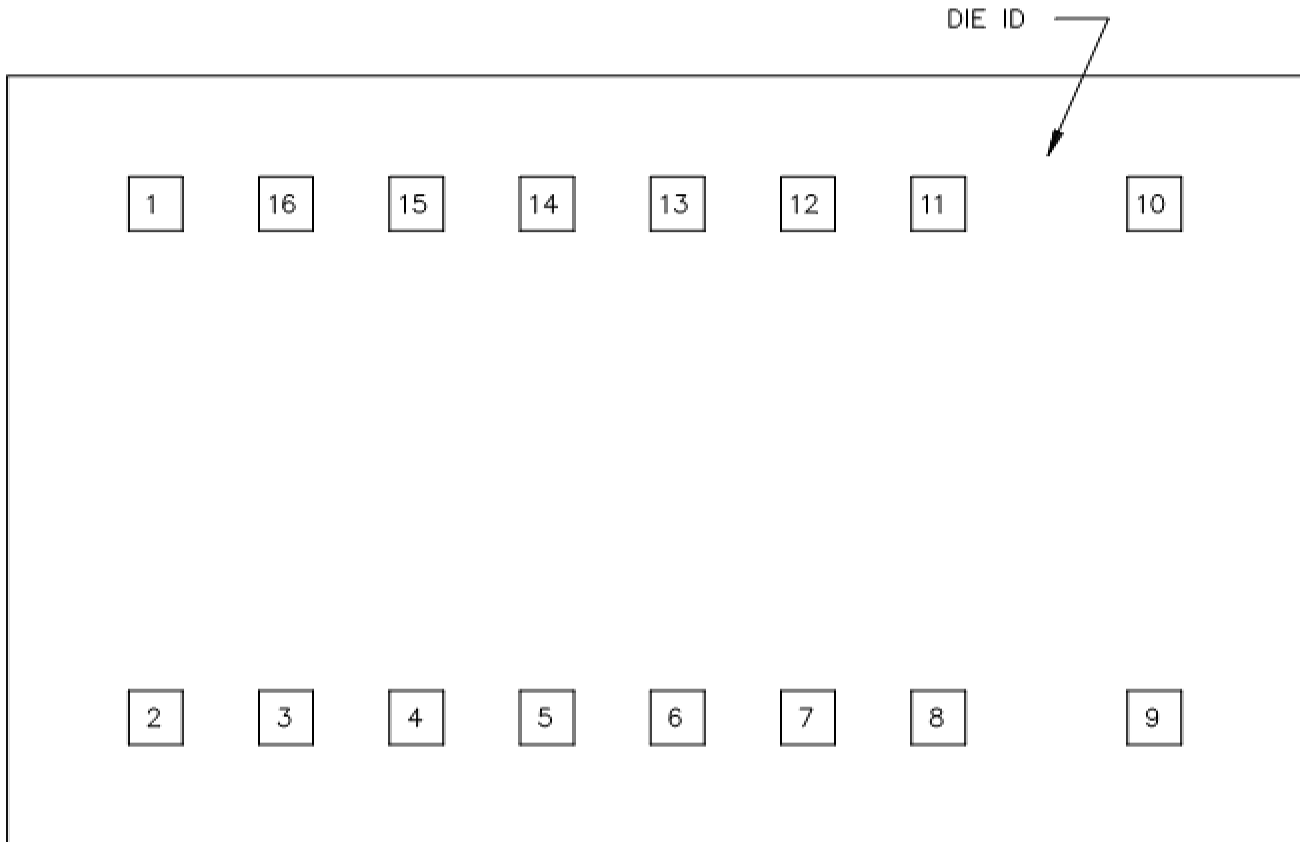


FIGURE A-1. Die bonding pad locations and electrical functions.

Die bond pad coordinate location (A-step)

Terminal symbol	Pad number	X/Y coordinates		Pad size		
		X	Y	X		Y
INPUT 4	1	-696	359	77	x	77
INPUT 5	2	-696	-359	77	x	77
INPUT 6	3	-493	-359	77	x	77
INPUT 7	4	-299	-359	77	x	77
DGND	5	-112	-359	77	x	77
V_D	6	75	-359	77	x	77
D_{IN}	7	228	-359	77	x	77
D_{OUT}	8	434	-359	77	x	77
SCLK	9	704	-359	77	x	77
$\overline{CS}$	10	704	359	77	x	77
V_A	11	400	359	77	x	77
AGND	12	242	359	77	x	77
INPUT 0	13	38	359	77	x	77
INPUT 1	14	-154	359	77	x	77
INPUT 2	15	-347	359	77	x	77
INPUT 3	16	-539	359	77	x	77

Referenced to die center, coordinates in μm. NC = no connection. NU = not used.

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 1808.48 µm (71.2 mils) x 1071.88 µm (42.2 mils)
Die thickness: 304.8 µm nominal

Interface materials.
Top metallization: Al, 0.5% CU
Backside metallization: Bare back

Glassivation.
Type: Oxide/Nitride
Thickness: 14000 Å

Substrate: Silicon

Assembly related information.
Substrate potential: Ground or floating
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-08-24

Approved sources of supply for SMD 5962-07227 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0722701VFA	01295	ADC128S102WRQV
5962R0722701VZA	01295	ADC128S102WGRQV
5962R0722701V9A	01295	ADC128S102 MDR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.