

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redraw. Add device type 02 and RHA information. - drw	12-03-15	Charles F. Saffle
B	Corrections to figure 1, case outline X. - drw	16-05-02	Charles F. Saffle



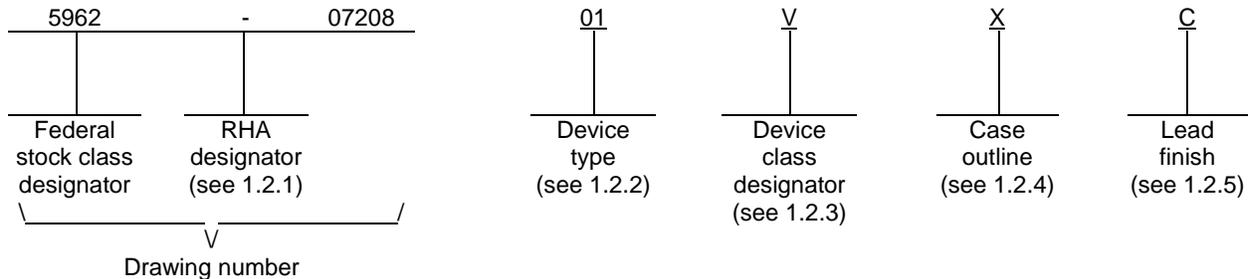
REV																				
SHEET																				
REV	B	B	B	B	B															
SHEET	15	16	17	18	19															
REV STATUS OF SHEETS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Dan Wonnell	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p align="center">MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT, 500 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Rajesh Pithadia																		
	APPROVED BY Robert M. Heber																		
	DRAWING APPROVAL DATE 07-10-26																		
AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE 67268	5962-07208															
		SHEET		1 OF 19															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	ADS5463-SP	A/D converter, 12-bit, 500 MSPS
02	ADS5463-SP	A/D converter, 12-bit, 500 MSPS

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	84	Quad flatpack with non-conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. ^{1/}

Supply voltage:

AV _{DD5} to GND	6 V
DV _{DD3} to GND	5 V
AV _{DD3} to GND	5 V
Analog input to GND	-0.3 V to AV _{DD5} + 0.3 V
Clock input to GND	-0.3 V to AV _{DD5} + 0.3 V
CLK to $\overline{\text{CLK}}$	± 2.5 V
Digital data output to GND	-0.3 V to DV _{DD3} + 0.3 V
Maximum junction temperature (T _J)	+150°C
Storage temperature range (T _{STG})	-65°C to 150°C
Thermal resistance, junction-to-ambient (θ_{JA})	21.81°C/W ^{2/}
Thermal resistance, junction-to-case (θ_{JC})	0.849°C/W ^{3/}

1.4 Recommended operating conditions.

Supplies:

Analog supply voltage (AV _{DD5})	4.75 V to 5.25 V
Analog supply voltage (AV _{DD3})	3 V to 3.6 V
Output driver supply voltage (DV _{DD3})	3 V to 3.6 V

Analog input:

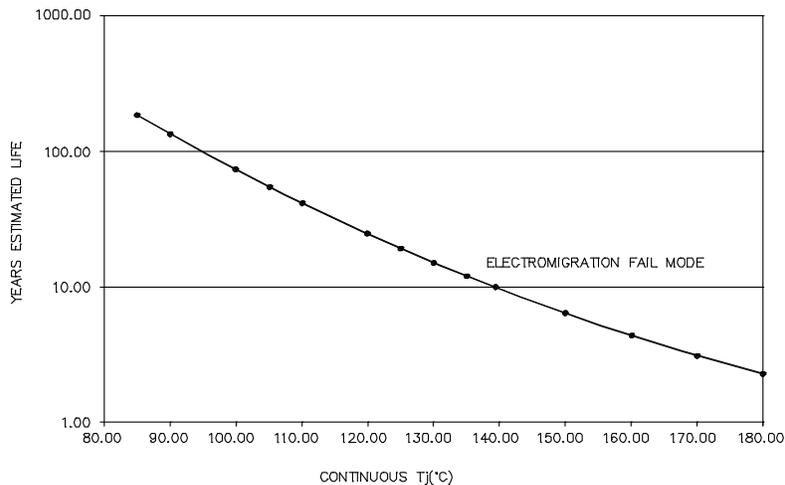
Differential input range	2.2 V _{PP}
Input common mode voltage (V _{CM})	2.4 V

Clock input:

ADCLK input sample rate (sine wave) (1/t _C)	500 MSPS
Clock amplitude, sine wave, differential	3 V _{PP}
Clock duty cycle	50 %

Operating case temperature range (T_C)

Estimated device life at elevated temperatures electromigration fail modes:



- ^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- ^{2/} Heat slug connected to PCB thermal plane. Airflow is at 0 LFM (no airflow).
- ^{3/} Specified with the thermal bond pad on the backside of the package soldered to a 2 ounce CU plate PCB thermal plane.

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1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)
 Device type 02: 100 krad(Si) 1/
 Maximum total dose available (dose rate ≤ 10 mrad(Si)/s):
 Device type 02 100 krad(Si) 2/

The manufacturer supplying RHA device type 02 on this drawing has performed characterization test to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) to 100 krad(Si) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1. Therefore these parts may be considered ELDRS free to 100 krad(Si). The manufacturer will perform high dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, conditions A for device type 02.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ The manufacturer supplying device type 02 has performed characterization testing in accordance with MIL-STD-883 method 1019, condition A at 100 krad(Si) only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krad(Si).

2/ The manufacturer supplying device type 02 has performed characterization testing in accordance with MIL-STD-883 method 1019, and the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) to 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 100 krad(Si).

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> , <u>2/</u> , <u>3/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal reference voltages section							
Reference voltage	V _{REF}		1, 2, 3	All	2.38	2.42	V
Dynamic accuracy section							
Differential linearity error	DNL	f _{IN} = 210 MHz	1, 2, 3	All	-0.98	1.2	LSB
Integral linearity error	INL	f _{IN} = 210 MHz	1, 2, 3	01	-2.9	2.9	LSB
				02	-3.5	3.5	
Offset error			1, 2, 3	All	-0.5	0.5	%FS
Gain error			1, 2, 3	All	-5	5	%FS
Power supply section							
Analog supply current	I _{AVDD5}	F _S = 500 MSPS, V _{IN} = full scale, f _{IN} = 300 MHz	1, 2, 3	01		335	mA
				02		345	
	I _{AVDD3}		01		140		
			02		148		
Output buffer supply current	I _{DVDD3}	F _S = 500 MSPS, V _{IN} = full scale, f _{IN} = 300 MHz	1, 2, 3	All		88	mA
Power dissipation	P _D	F _S = 500 MSPS, V _{IN} = full scale, f _{IN} = 300 MHz	1, 2, 3	01		2.425	W
				02		2.450	
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f _{IN} = 100 MHz	4	01	64.1		dBFS
					5	62.7	
			6		63.5		
			4, 5, 6		02	60.5	
		f _{IN} = 210 MHz	4	01	63.6		
					5	62.4	
			6		63.2		
			4, 5, 6		02	60.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> , <u>2/</u> , <u>3/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit			
					Min	Max				
Dynamic AC characteristics section - continued.										
Signal-to-noise ratio	SNR	f _{IN} = 300 MHz	4	01	62.7		dBFS			
			5		61.3					
			6		61.9					
			4, 5, 6	02	58.0					
Spurious free dynamic range	SFDR	f _{IN} = 100 MHz	4	01	57.9		dBc			
			5		58.8					
			6		58.6					
			4, 5, 6	02	57.9					
		f _{IN} = 210 MHz	4	01	55.2					
			5		56.6					
			6		56.9					
			4, 5, 6	02	55.2					
		f _{IN} = 300 MHz	4	01	54.1					
			5		51.3					
			6		56.2					
			4, 5, 6	02	51.2					
		Second harmonic	HD2	f _{IN} = 100 MHz	4	01		57.9		dBc
					5			58.8		
					6			58.6		
					4, 5, 6	02		57.9		
f _{IN} = 210 MHz	4			01	55.2					
	5				56.6					
	6				56.9					
	4, 5, 6			02	55.2					
f _{IN} = 300 MHz	4			01	54.1					
	5				51.3					
	6				56.2					
	4, 5, 6			02	51.2					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> , <u>2/</u> , <u>3/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit			
					Min	Max				
Dynamic AC characteristics section - continued.										
Third harmonic	HD3	f _{IN} = 100 MHz	4	01	69		dBc			
			5		68.5					
			6		65.6					
			4, 5, 6	02	64.0					
		f _{IN} = 210 MHz	4	01	66.7					
			5		65.3					
			6		64.1					
			4, 5, 6	02	59.0					
		f _{IN} = 300 MHz	4	01	70.1					
			5		61.9					
			6		64.8					
			4, 5, 6	02	61.9					
		Signal-to-noise and distortion	SINAD	f _{IN} = 100 MHz	4	01		58		dBc
					5			58		
					6			58.4		
					4, 5, 6	02		55.9		
f _{IN} = 210 MHz	4			01	55.8					
	5				56.2					
	6				56.7					
	4, 5, 6			02	53.8					
f _{IN} = 300 MHz	4			01	54.9					
	5				52.2					
	6				56.1					
	4, 5, 6			02	50.2					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> , <u>2/</u> , <u>3/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit			
					Min	Max				
Dynamic AC characteristics section - continued.										
Worst harmonic/spur (other than HD2 and HD3)	HDW	f _{IN} = 100 MHz	4	01	72.2		dBc			
			5		70.6					
			6		72.6					
			4, 5, 6	02	68.0					
		f _{IN} = 210 MHz	4		01	70.6				
			5			67.1				
			6	66.5						
			4, 5, 6	02	62.0					
		f _{IN} = 300 MHz	4		01	69.3				
			5			66.3				
			6	66.3						
			4, 5, 6	02	62.0					
		Total harmonic distortion	f _{IN} = 100 MHz		4	01		57.8		dBc
					5			58.3		
				6	58.1					
				4, 5, 6	02	57.8				
f _{IN} = 210 MHz	4		01	55						
	5			55.9						
	6			56.2						
	4, 5, 6		02	55.0						
f _{IN} = 300 MHz	4			01	53.9					
	5				51					
	6		55.6							
	4, 5, 6		02	51.0						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> , <u>2/</u> , <u>3/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

Dynamic AC characteristics section - continued.

Effective number of bits	ENOB	f _{IN} = 100 MHz	4	01	9.3		Bits	
			5		9.3			
			6		9.4			
			4, 5, 6	02	9.0			
		f _{IN} = 210 MHz	4		01	8.9		
			5			9.0		
			6	9.1				
			4, 5, 6	02	8.65			
		f _{IN} = 300 MHz	4		01	8.8		
			5			8.3		
			6	9.0				
			4, 5, 6	02	8.05			

Digital characteristics – LVDS digital outputs

Differential output voltage	V _{OD}		1, 2, 3	01, 02	247	454	mV
Common mode output voltage	V _{OC}		1, 2, 3	01, 02	1.125	1.375	V

Timing characteristics 4/

Clock input section

Clock period	t _{CLK}		9, 10, 11	01, 02	2	50	ns
Clock pulse duration, high	t _{CLKH}		9, 10, 11	01, 02	1		ns
Clock pulse duration, low	t _{CLKL}		9, 10, 11	01, 02	1		ns

- 1/ Device type 02 has been characterized at level of R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).
- 2/ The manufacturer supplying RHA device type 02 on this drawing has performed characterization test to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) to 100 krad(Si) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1. Therefore these parts may be considered ELDRS free to 100 krad(Si). The manufacturer will perform high dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, conditions A for device type 02.
- 3/ Unless otherwise specified, sampling rate = 500 MSPS, 50 % clock duty cycle, AV_{DD5} = 5 V, AV_{DD3} = 3.3 V, DV_{DD3} = 3.3 V, 3 V_{PP} differential clock.
- 4/ Timing parameters are assured by design or characterization, but not production tested.

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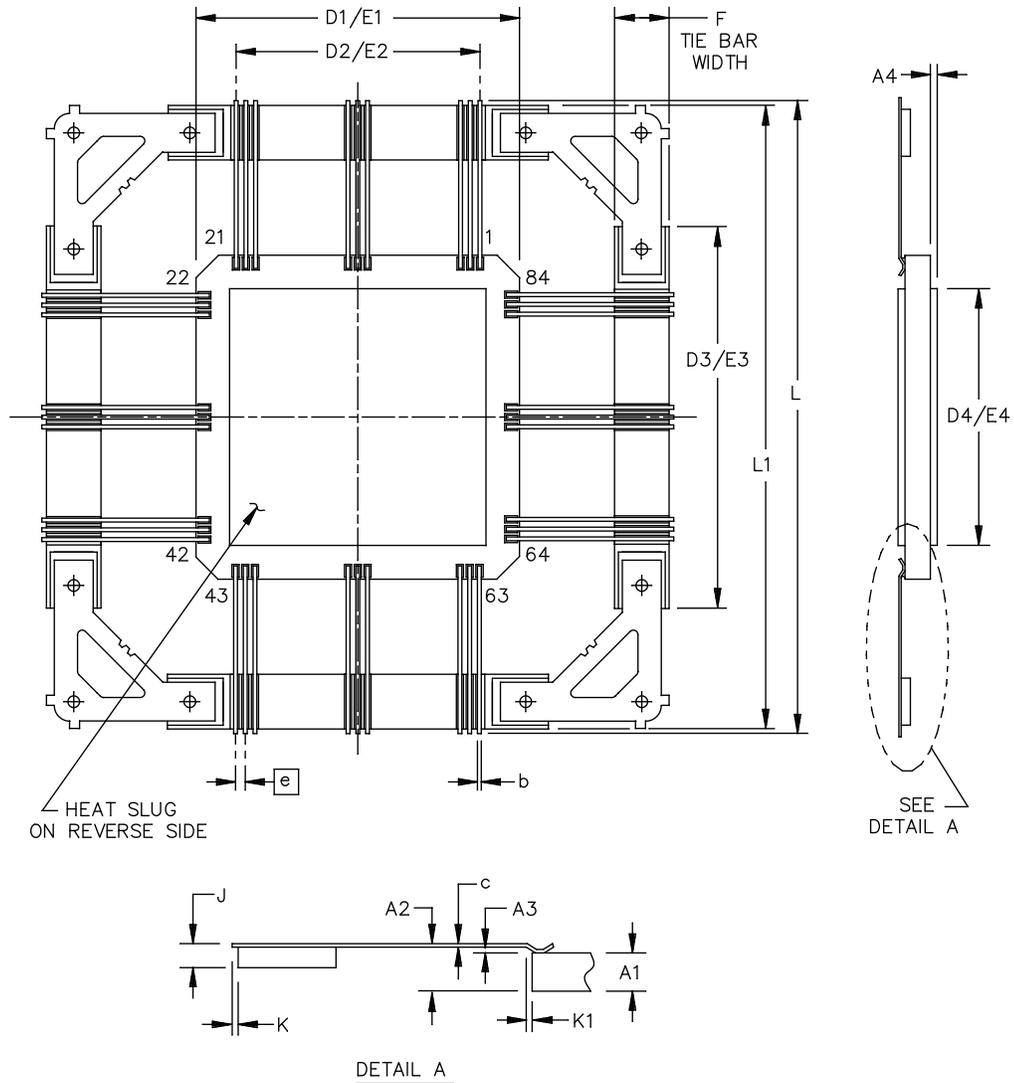


FIGURE 1. Case outline X.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	---	0.091	---	2.31
A2	---	0.115	---	2.92
A3	0.002	0.014	0.05	0.36
A4	0.03 BSC		0.762 BSC	
b	0.006	0.013	0.15	0.33
c	0.004	0.009	0.10	0.23
D1/E1	0.740	0.760	18.80	19.30
D2/E2	0.500 BSC		12.7 BSC	
D3/E3	1.196	1.222	30.38	31.04
D4/E4	0.629 BSC		15.98 BSC	
e	0.025 BSC		0.64 BSC	
F	0.175	0.225	4.45	5.72
J	0.030	0.040	0.76	1.02
K	---	0.020	---	0.51
K1	---	0.018	---	0.46
L		2.025		51.44
L1	1.980	2.024	50.29	51.41
N	84			

NOTES:

1. Controlling dimensions are inches, millimeter dimensions are given for reference only.
2. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heat sink are connected to GND leads.

FIGURE 1. Case outline X – continued.

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Device type	01 and 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	22	GND	43	GND	64	GND
2	DV _{DD3}	23	AV _{DD5}	44	$\overline{\text{OVR}}$	65	$\overline{\text{D4}}$
3	GND	24	GND	45	OVR	66	D4
4	AV _{DD5}	25	AV _{DD5}	46	NC	67	$\overline{\text{D5}}$
5	NC	26	GND	47	NC	68	D5
6	NC	27	AV _{DD5}	48	NC	69	GND
7	V _{REF}	28	GND	49	NC	70	DV _{DD3}
8	GND	29	AV _{DD5}	50	NC	71	$\overline{\text{D6}}$
9	AV _{DD5}	30	GND	51	NC	72	D6
10	GND	31	RESERVED	52	NC	73	$\overline{\text{D7}}$
11	CLK	32	GND	53	NC	74	D7
12	$\overline{\text{CLK}}$	33	AV _{DD5}	54	DV _{DD3}	75	$\overline{\text{D8}}$
13	GND	34	GND	55	GND	76	D8
14	AV _{DD5}	35	RESERVED	56	$\overline{\text{D0}}$	77	$\overline{\text{D9}}$
15	AV _{DD5}	36	GND	57	D0	78	D9
16	GND	37	AV _{DD3}	58	$\overline{\text{D1}}$	79	$\overline{\text{D10}}$
17	AIN	38	GND	59	D1	80	D10
18	$\overline{\text{AIN}}$	39	AV _{DD3}	60	$\overline{\text{D2}}$	81	$\overline{\text{D11}}$
19	GND	40	GND	61	D2	82	D11
20	AV _{DD5}	41	AV _{DD3}	62	$\overline{\text{D3}}$	83	$\overline{\text{DRY}}$
21	GND	42	GND	63	D3	84	DRY

FIGURE 2. Terminal connections.

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Terminal symbol	Description
AIN	Differential input signal (positive)
$\overline{\text{AIN}}$	Differential input signal (negative)
AV _{DD5}	Analog power supply (5 V)
AV _{DD3}	Analog power supply (3.3 V)
CLK	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	Differential input clock (negative)
D0, $\overline{\text{D0}}$	LVDS digital output pair, least significant bit (LSB)
$\overline{\text{D1-D3}}$, D1 - D3	LVDS digital output pairs
$\overline{\text{D4-D5}}$, D4 - D5	LVDS digital output pairs
$\overline{\text{D6-D10}}$, D6 - D10	LVDS digital output pairs
D11, $\overline{\text{D11}}$	LVDS digital output pair, most significant bit (MSB)
DRY, $\overline{\text{DRY}}$	Data ready LVDS output pair
DV _{DD}	Output driver power supply (3.3 V)
GND	Ground
NC	No connect
OVR, $\overline{\text{OVR}}$	Over range indicator LVDS output. A logic high signals an analog input excess of full scale range.
RESERVED	Reserved for possible future control features
VREF	Reference voltage

FIGURE 2. Terminal connections – continued.

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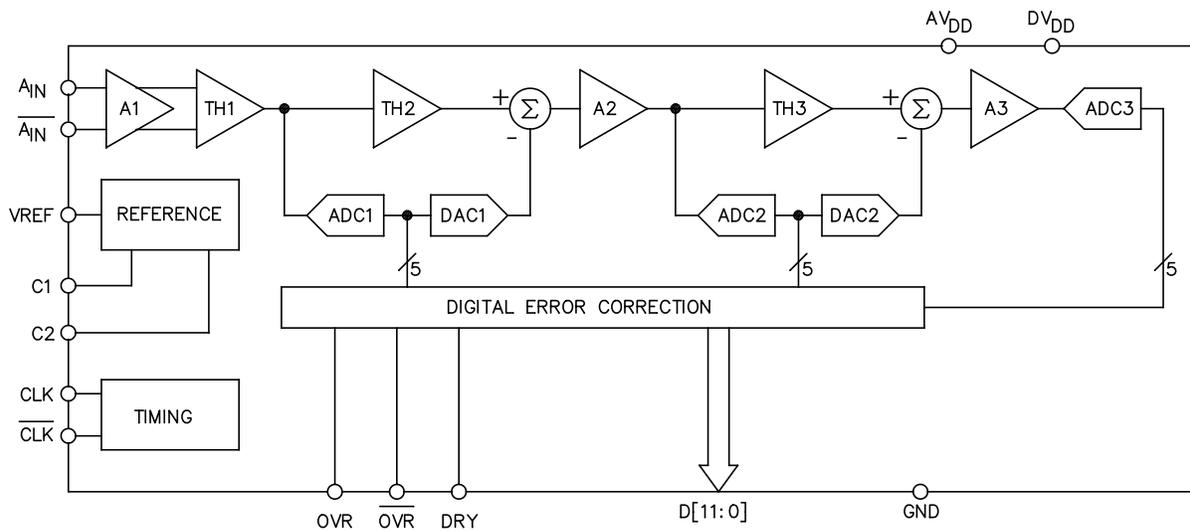


FIGURE 3. Block diagram.

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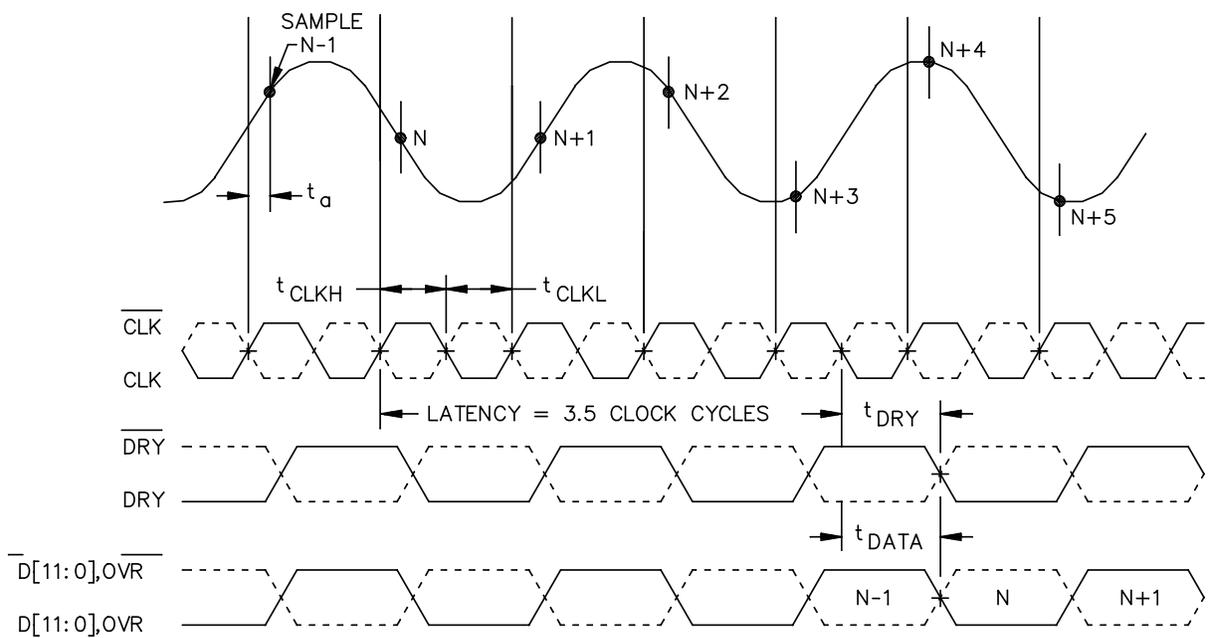


FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, <u>1/ 2/</u> 4, 5, 6, 9, 10, 11	1, 2, 3, <u>1/ 2/ 3/</u> 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, <u>2/</u> 9,10,11	1, 2, 3, 4, 5, 6, <u>2/</u> 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 4	1, 4, 9 <u>3/</u>
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4, 9
Group E end-point electrical parameters (see 4.4)	1, 4	1, 4, 9

1/ PDA applies to subgroup 1.

2/ Subgroups 9, 10, 11, if not tested, are guaranteed to the limits in table I.

3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters <u>1/</u>	Delta limits
Reference voltage (V _{REF})	+/- 10 mV
3.3 V digital supply (I _{DVDD3})	+/- 2 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A and as specified herein. The manufacturer shall performed high dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, conditions A for device type 02.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-05-02

Approved sources of supply for SMD 5962-07208 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0720801VXC	01295	ADS5463MHFG-V
5962R0720802VXC	01295	ADS5463MHFG-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.