REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrections to figure 1, case outline X. - drw	16-05-02	Charles F. Saffle
B	Update document paragraphs to current MIL-PRF-38535 requirements. - ro	22-09-07	James R. Eschmeyer

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
07-10-25

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL-LINEAR, 13-BIT, 250 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON

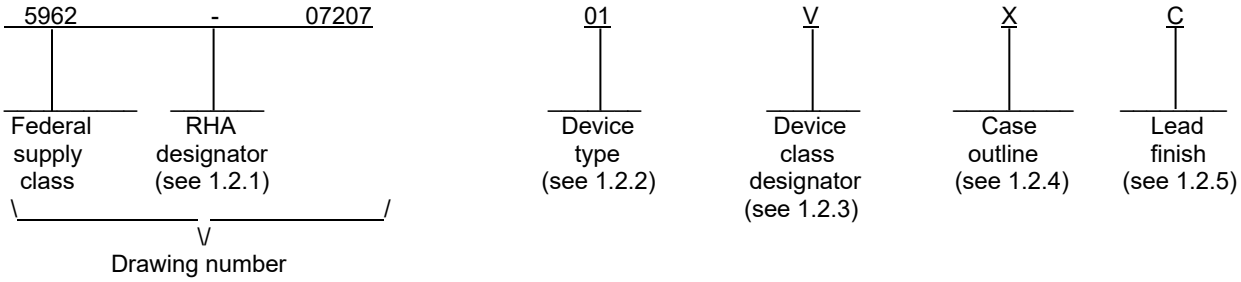
AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE **67268**	**5962-07207**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADS5444M	A/D converter, 13-bit, 250 MSPS

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	84	Quad flatpack with non-conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage :
- AV_{DD} to GND ..... 6 V
- DRV_{DD} to GND ..... 5 V

Analog input to GND ..... -0.3 V to AV_{DD} + 0.3 V
Clock input to GND ..... -0.3 V to AV_{DD} + 0.3 V
CLK to $\overline{CLK}$ ..... ±2.5 V
Digital data output to GND ..... -0.3 V to DRV_{DD} + 0.3 V
Maximum junction temperature (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 21.813°C/W
Thermal resistance, junction-to-case (θ_{JC}) ..... 0.849°C/W

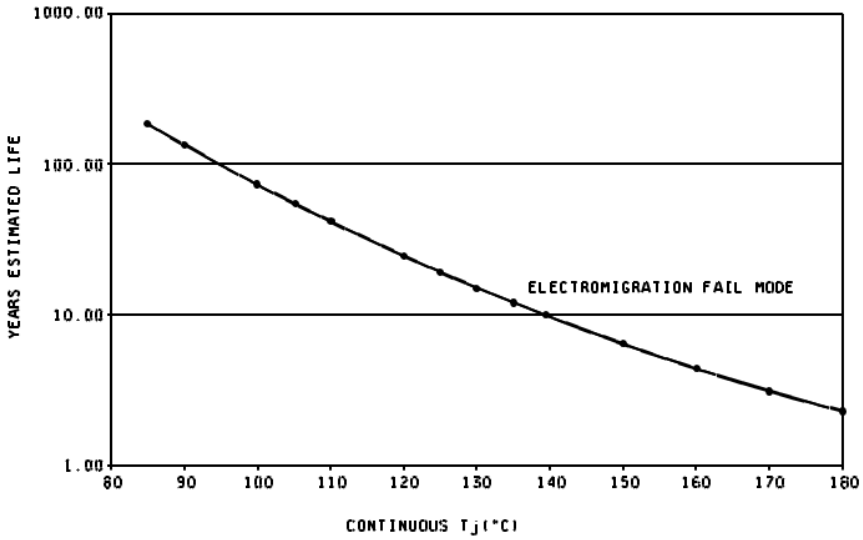
1.4 Recommended operating conditions.

Supplies:
- Analog supply voltage (AV_{DD}) ..... 4.75 V to 5.25 V
- Output driver supply voltage (DRV_{DD}) ..... 3 V to 3.6 V

Analog input:
- Differential input range ..... 2.2 V_{PP}
- Input common mode voltage (V_{CM}) ..... 2.4 V

Clock input:
- ADCLK input sample rate (sinewave) (1/t_C) ..... 10 MSPS to 250 MSPS
- Clock amplitude, sine wave, differential ..... 3 V_{PP}
- Clock duty cycle ..... 50 %

Operating case temperature range (T_C) ..... -55°C to +125°C
Estimated device life at elevated temperatures electromigration fail modes:



1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal reference voltages section							
Reference voltage	V_{REF}		1, 2, 3	01	2.38	2.42	V
Dynamic accuracy section							
Differential linearity error	DNL	f_{IN} = 100 MHz	1, 2, 3	01	-0.98	2	LSB
Integral linearity error	INL	f_{IN} = 100 MHz	1, 2	01	-2.8	2.8	LSB
			3		-4.8	4.8	
Offset error			1, 2, 3	01	-0.6	0.6	%FS
Gain error			1, 2, 3	01	-5	5	%FS
Power supply section							
Analog supply current	I_{AVDD}	F_S = 250 MSPS, V_{IN} = full scale, f_{IN} = 170 MHz	1, 2, 3	01		410	mA
Output buffer supply current	I_{DRVDD}	F_S = 250 MSPS, V_{IN} = full scale, f_{IN} = 170 MHz	1, 2, 3	01		100	mA
Power dissipation	P_D	F_S = 250 MSPS, V_{IN} = full scale, f_{IN} = 170 MHz	1, 2, 3	01		2.29	W
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f_{IN} = 10 MHz	4	01	68		dBc
			5		66.8		
			6		63.2		
		f_{IN} = 100 MHz	4		67.3		
			5		66.5		
			6		62.1		
		f_{IN} = 170 MHz	4		66.5		
			5		66.1		
			6		60.8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Spurious free dynamic range	SFDR	f_{IN} = 10 MHz	4, 6	01	75		dBc
			5		74		
		f_{IN} = 100 MHz	4		62		
			5		74.5		
			6		63		
		f_{IN} = 170 MHz	4		63		
			5		65		
			6		59		
Second harmonic	HD2	f_{IN} = 10 MHz	4	01	75		dBc
			5		74		
			6		76.5		
		f_{IN} = 100 MHz	4		62		
			5		76		
			6		63		
		f_{IN} = 170 MHz	4		63		
			5		65		
			6		59		
Third harmonic	HD3	f_{IN} = 10 MHz	4, 5, 6	01	78.5		dBc
		f_{IN} = 100 MHz	4		72		
			5		74.5		
			6		65		
		f_{IN} = 170 MHz	4		65		
			5		69		
			6		63		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Worst other harmonic/spur (other than HD2 and HD3)	HD	f_{IN} = 10 MHz	4	01	80		dBc
			5		81		
			6		75		
		f_{IN} = 100 MHz	4		74		
			5		78		
			6		69		
		f_{IN} = 170 MHz	4		70		
			5		78		
			6		64		
Total harmonic distortion	THD	f_{IN} = 10 MHz	4	01	74.5		dBc
			5		73		
			6		74		
		f_{IN} = 100 MHz	4		61.5		
			5		73		
			6		60		
		f_{IN} = 170 MHz	4		62		
			5		63.5		
			6		58		
Signal-to-noise + distortion	SINAD	f_{IN} = 10 MHz	4	01	67.7		dBc
			5		66.4		
			6		62.9		
		f_{IN} = 100 MHz	4		62.2		
			5		66.2		
			6		59.4		
		f_{IN} = 170 MHz	4		61.7		
			5		62.9		
			6		57.6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Effective number of bits	ENOB	f_{IN} = 10 MHz	4	01	10.9		Bits
			5		10.7		
			6		10.1		
		f_{IN} = 100 MHz	4		10		
			5		10.7		
			6		9.5		
		f_{IN} = 170 MHz	4		9.9		
			5		10.1		
			6		9.2		
Digital characteristics – LVDS digital outputs							
Differential output voltage	V_{DIFF}		1, 2, 3	01	247	452	mV
Output offset voltage	V_{OFF}		1, 2, 3	01	1.125	1.375	V
Clock to data ready (DRY) section							
Clock rising 50% to data ready rising 50%	t_{C_DR}		9, 10, 11	01	2.7	3.5	ns
Data ready (DRY) / DATA, over range (OVR) section 2/							
Data valid to DRY	$t_{su}(DR)$		9, 10, 11	01	1.5		ns
DRY to invalid data	$t_h(DR)$		9, 10, 11	01	0.9		ns

1/ Unless otherwise specified, sampling rate = 250 MSPS, 50 % clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, -1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock.

2/ Data is updated with clock falling edge or DRY rising edge.

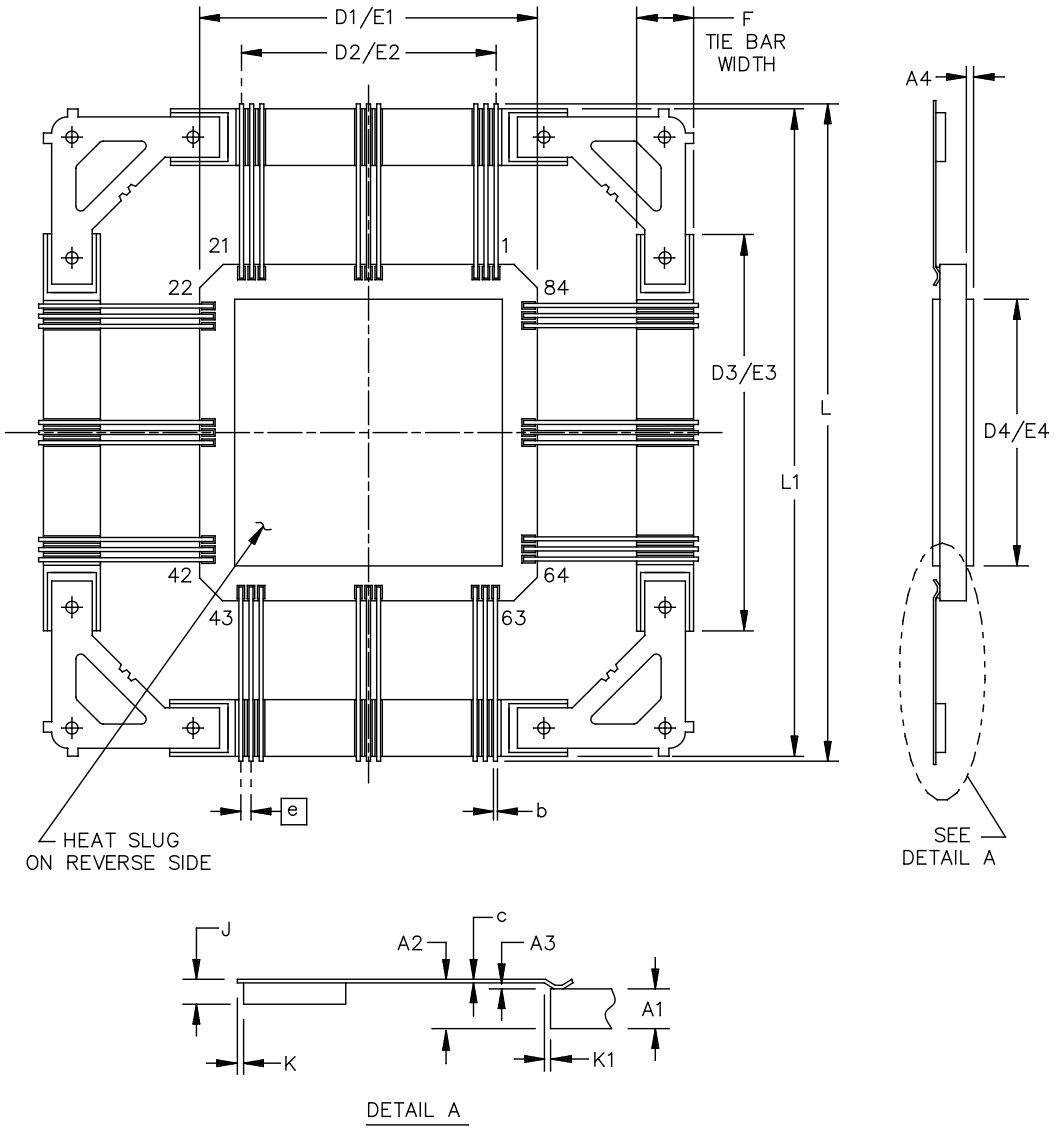


FIGURE 1. Case outline X.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-07207**
		REVISION LEVEL **B**	SHEET **9**

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	---	0.091	---	2.31
A2	---	0.115	---	2.92
A3	0.002	0.014	0.05	0.36
A4	0.03 BSC		0.762 BSC	
b	0.006	0.013	0.15	0.33
c	0.004	0.009	0.10	0.23
D1/E1	0.740	0.760	18.80	19.30
D2/E2	0.500 BSC		12.7 BSC	
D3/E3	1.196	1.222	30.38	31.04
D4/E4	0.629 BSC		15.98 BSC	
e	0.025 BSC		0.64 BSC	
F	0.175	0.225	4.45	5.72
J	0.030	0.040	0.76	1.02
K	---	0.020	---	0.51
K1	---	0.018	---	0.46
L		2.025		51.44
L1	1.980	2.024	50.29	51.41
N	84			

NOTES:
1. Controlling dimensions are inches, millimeter dimensions are given for reference only.
2. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heat sink are connected to GND leads.

FIGURE 1. Case outline X – continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	22	GND	43	GND	64	GND
2	DV_{DD}	23	AV_{DD}	44	$\overline{OVR}$	65	$\overline{D5}$
3	GND	24	GND	45	OVR	66	D5
4	AV_{DD}	25	AV_{DD}	46	NC	67	$\overline{D6}$
5	NC	26	GND	47	NC	68	D6
6	NC	27	AV_{DD}	48	NC	69	GND
7	V_{REF}	28	GND	49	NC	70	DV_{DD}
8	GND	29	AV_{DD}	50	NC	71	$\overline{D7}$
9	AV_{DD}	30	GND	51	NC	72	D7
10	GND	31	NC	52	$\overline{D0}$	73	$\overline{D8}$
11	CLK	32	GND	53	D0	74	D8
12	$\overline{CLK}$	33	AV_{DD}	54	DV_{DD}	75	$\overline{D9}$
13	GND	34	GND	55	GND	76	D9
14	AV_{DD}	35	NC	56	$\overline{D1}$	77	$\overline{D10}$
15	AV_{DD}	36	GND	57	D1	78	D10
16	GND	37	AV_{DD}	58	$\overline{D2}$	79	$\overline{D11}$
17	AIN	38	GND	59	D2	80	D11
18	$\overline{AIN}$	39	AV_{DD}	60	$\overline{D3}$	81	$\overline{D12}$
19	GND	40	GND	61	D3	82	D12
20	AV_{DD}	41	AV_{DD}	62	$\overline{D4}$	83	$\overline{DRY}$
21	GND	42	GND	63	D4	84	DRY

FIGURE 2. Terminal connections.

Terminal symbol	Description
AV_{DD}	Analog power supply
DV_{DD}	Output driver power supply
GND	Ground
V_{REF}	Reference voltage
CLK	Differential input clock (positive). Conversion Initiated on rising edge
$\overline{CLK}$	Differential input clock (negative)
AIN	Differential input signal (positive)
$\overline{AIN}$	Differential input signal (negative)
OVR, $\overline{OVR}$	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, $\overline{D0}$	LVDS digital output pair, least significant bit (LSB)
D1-D4, $\overline{D1}$ - $\overline{D4}$	LVDS digital output pairs
D5-D6, $\overline{D5}$ - $\overline{D6}$	LVDS digital output pairs
D7-D11, $\overline{D7}$ - $\overline{D11}$	LVDS digital output pairs
D12, $\overline{D12}$	LVDS digital output pair, most significant bit (MSB)
DRY, $\overline{DRY}$	Data ready LVDS output pair
NC	No connect

FIGURE 2. Terminal connections – continued.

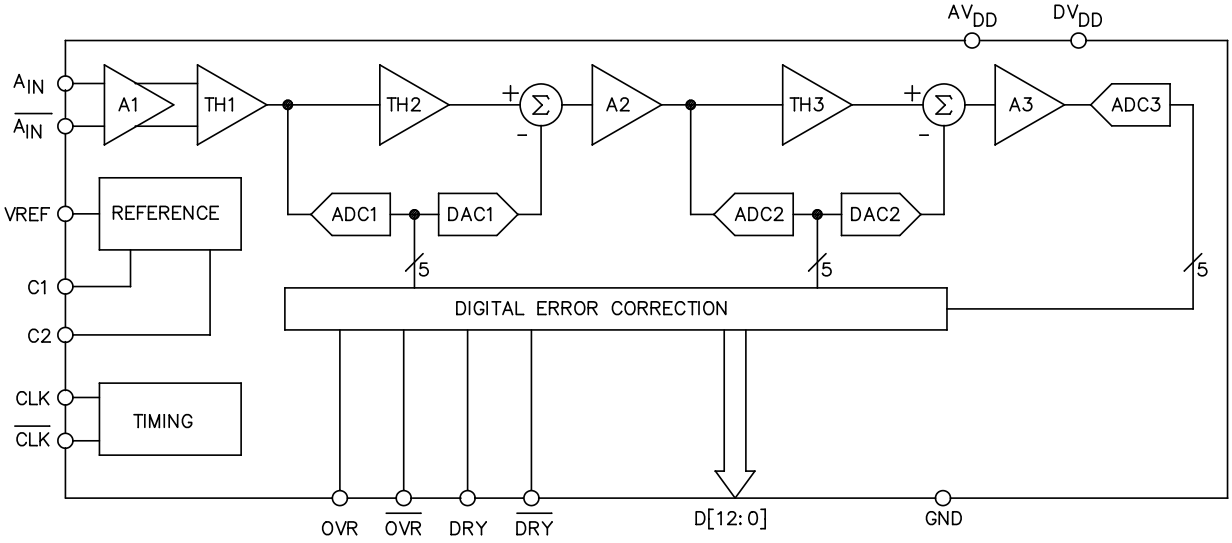


FIGURE 3. Block diagram.

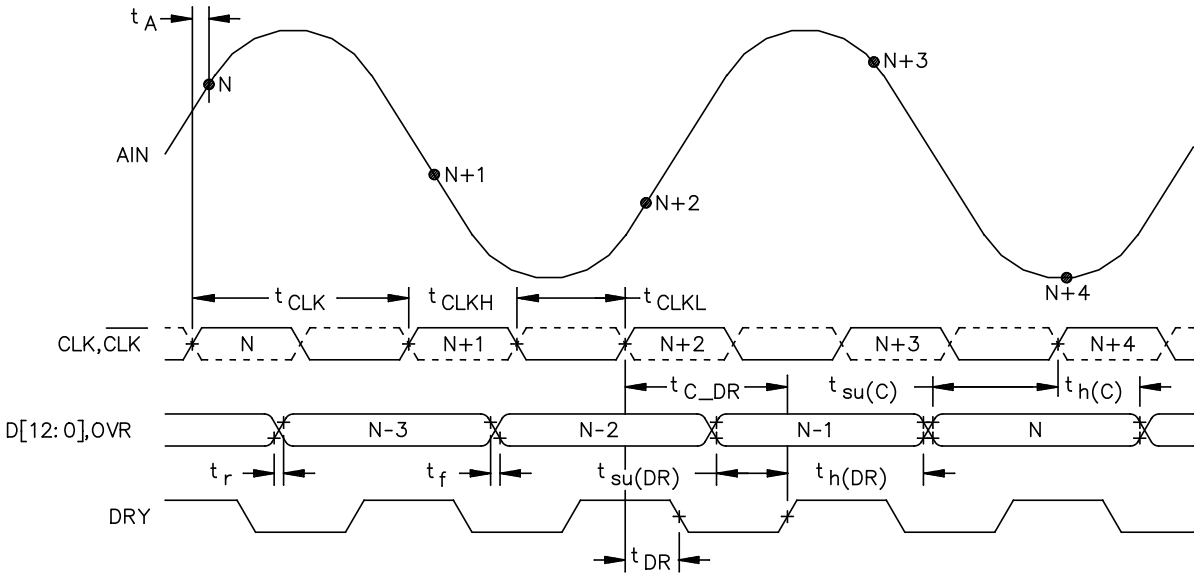


FIGURE 4. Timing waveforms.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 1/ 5, 6, 9, 10, 11	1, 2, 3, 4, 1/, 2/ 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1, 4	1, 4 2/
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	- - -	- - -

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters 1/	Delta limits
V_{REF}, Reference voltage	±10 mV
I_{DRVDD}, Output buffer supply current	±2 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-09-07

Approved sources of supply for SMD 5962-07207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0720701VXC	01295	ADS5444MHFG-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243