REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current MIL-PRF-38535 requirements. – jch	18-03-05	Charles F. Saffle
B	Delete device class M references by making change to paragraph 1.2.5 and removing paragraph 6.1.2. entirely. Update document paragraphs to current MIL-PRF-38535 requirements. - ro	23-05-18	James R. Eschmeyer

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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DRAWING APPROVAL DATE
08-04-22

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

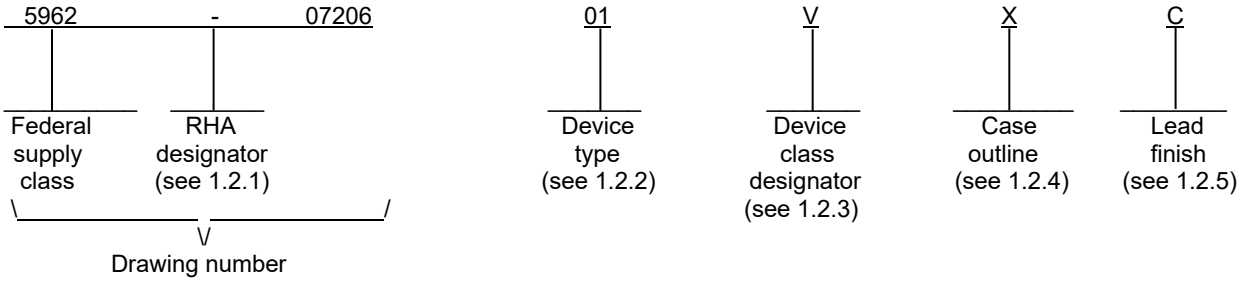
MICROCIRCUIT, DIGITAL-LINEAR, 14-BIT, 105 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE **67268**	**5962-07206**
		SHEET	1 OF 19	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADS5424M	14 bit, 105 MSPS, analog to digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	52	Quad flat pack with non-conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

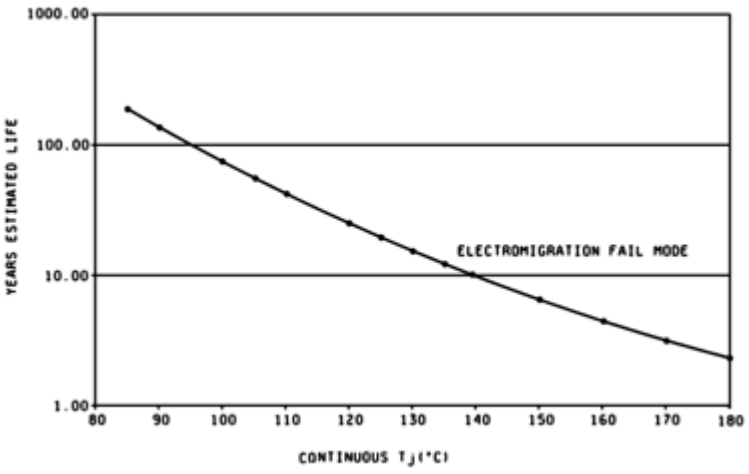
1.3 Absolute maximum ratings. 1/

Supply voltage :	
AV_{DD} to GND	6 V
DRV_{DD} to GND	5 V
Analog input to GND	-0.3 V to AV_{DD} + 0.3 V
Clock input to GND	-0.3 V to AV_{DD} + 0.3 V
CLK to CLK	±2.5 V
Digital data output to GND	-0.3 V to DRV_{DD} + 0.3 V
Maximum junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction-to-ambient (θ_{JA})	21.81° C/W 2/
Thermal resistance, junction-to-case (θ_{JC})	0.849° C/W 3/

1.4 Recommended operating conditions.

Supplies:	
Analog supply voltage (AV_{DD})	4.75 V to 5.25 V
Output driver supply voltage (DRV_{DD})	3 V to 3.6 V
Analog input:	
Differential input range	2.2 V_{PP}
Input common mode voltage (V_{CM})	2.4 V
Digital output:	
Maximum output load	10 pF
Clock input:	
ADCLK input sample rate (sine wave) (1/t_C)	30 MSPS to 105 MSPS
Clock amplitude, sine wave, differential	3 V_{PP}
Clock duty cycle	50 %
Operating case temperature range (T_C)	-55°C to +125°C

Estimated device life at elevated temperatures electromigration fail mode:



1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Heat slug connected to printed circuit board (PCB) thermal plane. Airflow is at 0 LFM (no airflow).
3/ Specified with the thermal bond pad on the backside of the package soldered to a 2 ounce CU plate PCB thermal plane.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal reference volta ges section							
Reference voltage	V_{REF}		1,2,3	01	2.38	2.41	V
Dynamic accuracy sect i on							
Differential linearity error	DNL	f_{IN} = 10 MHz	4,5,6	01	-0.98	1.5	LSB
Integral linearity error	INL	f_{IN} = 10 MHz	4,5	01	-5.0	+5.0	LSB
			6		-6.9	+6.9	
Offset error			4,5,6	01	-1.5	1.5	%FS
Gain error			4,5,6	01	-5	5	%FS
Power supply section							
Analog supply current	I_{AVDD}	F_S = 105 MSPS, V_{IN} = full scale, f_{IN} = 70 MHz	1,2,3	01		410	mA
Output buffer supply current	I_{DRVDD}	F_S = 105 MSPS, V_{IN} = full scale, f_{IN} = 70 MHz	1,2,3	01		55	mA
Power dissipation	P_D	F_S = 105 MSPS, f_{IN} = 70 MHz, total power with 10 pF load on each digital output to ground	1,2,3	01		2.3	W

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteris tics section							
Signal-to-noise ratio	SNR	f_{IN} = 10 MHz	4,6	01	70.5		dBc
			5		71.0		
		f_{IN} = 30 MHz	4,5,6		70.0		
		f_{IN} = 70 MHz	4		68.2		
			5		67.0		
			6		68.0		
Spurious free dynamic range	SFDR	f_{IN} = 10 MHz	4	01	72.0		dBc
			5,6		71.0		
		f_{IN} = 30 MHz	4		77.0		
			5		69.0		
			6		75.0		
		f_{IN} = 70 MHz	4		68.0		
			5		69.0		
			6		67.0		
Signal-to-noise plus distortion	SINAD	f_{IN} = 10 MHz	4	01	68.6		dBc
			5		68.3		
			6		68.2		
		f_{IN} = 30 MHz	4,6		69.4		
			5		67.0		
		f_{IN} = 70 MHz	4		65.8		
			5		64.6		
			6		65.0		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Second harmonic	HD2	f_{IN} = 10 MHz	4	01	72.0		dBc
			5,6		71.0		
		f_{IN} = 30 MHz	4		77.0		
			5		69.0		
			6		75.0		
		f_{IN} = 70 MHz	4		68.0		
			5		69.0		
			6		67.0		
Third harmonic	HD3	f_{IN} = 10 MHz	4	01	72.0		dBc
			5,6		71.0		
		f_{IN} = 30 MHz	4		77.0		
			5		69.0		
			6		75.0		
		f_{IN} = 70 MHz	4		68.0		
			5		69.0		
			6		67.0		
Worst other harmonic / spur (other than HD2 and HD3)		f_{IN} = 10 MHz	4,5,6	01	75.0		dBc
		f_{IN} = 30 MHz	4,6		80.0		
			5		74.0		
		f_{IN} = 70 MHz	4,6		74.0		
			5		72.0		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteris tics section - continued.							
Total harmonic distortion	THD	f_{IN} = 10 MHz	4	01	71.0		dBc
			5,6		70.0		
		f_{IN} = 30 MHz	4		75.0		
			5		68.0		
			6		73.8		
		f_{IN} = 70 MHz	4		67.4		
			5		67.2		
			6		66.4		
Effective number of bits	ENOB	f_{IN} = 10 MHz	4	01	11.1		Bits
			5,6		11.0		
		f_{IN} = 30 MHz	4,6		11.2		
			5		10.8		
		f_{IN} = 70 MHz	4		10.6		
			5		10.4		
			6		10.5		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital characteristics 2/							
Digital outputs section							
Low level output voltage	V_{OL}	C_{LOAD} = 10 pF 3/	1,2,3	01		0.6	V
High level output voltage	V_{OH}	C_{LOAD} = 10 pF 3/	1,2,3	01	2.6		V
Output data voltage midpoint	DMID		1,2,3	01	1.65	1.8	V
Timing characteristics							
Clock to data ready (DRY) section							
Clock rising 50% to data ready falling 50%	t_{DR}		9,10,11	01	2.2	4.7	ns
Clock rising 50% to data ready rising 50% with 50% duty cycle clock	$t_{C\_DR50\%}$		9,10,11	01	7.0	9.5	ns
Clock to DATA, over r ange (OVR) section 4/							
Valid DATA 5/ to clock 50% with 50% duty cycle clock (setup time)	$t_{su}(C)$		9,10,11	01	1.8		ns
Clock 50% to invalid DATA 5/ (hold time)	$t_h(C)$		9,10,11	01	2.6		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Data ready (DRY) / DAT A, over range (OVR) section 4/							
Valid DATA 5/ to data ready 50% with 50% duty cycle clock (setup time)	t_{su}(DR)_50%		9,10,11	01	0.9		ns
Data ready 50% to invalid DATA 5/ with 50% duty cycle clock (hold time)	t_h(DR)_50%		9,10,11	01	3.9		ns

1/ Unless otherwise specified, sampling rate = 105 MSPS, 50 % clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, -1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock.

2/ Unless otherwise specified, AV_{DD} = 5 V and DRV_{DD} = 3.3 V.

3/ Equivalent capacitance to ground of (load + parasitics of transmission lines).

4/ Data is updated with clock rising edge or data ready (DRY) falling edge.

5/ See V_{OH} and V_{OL} levels.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Case X

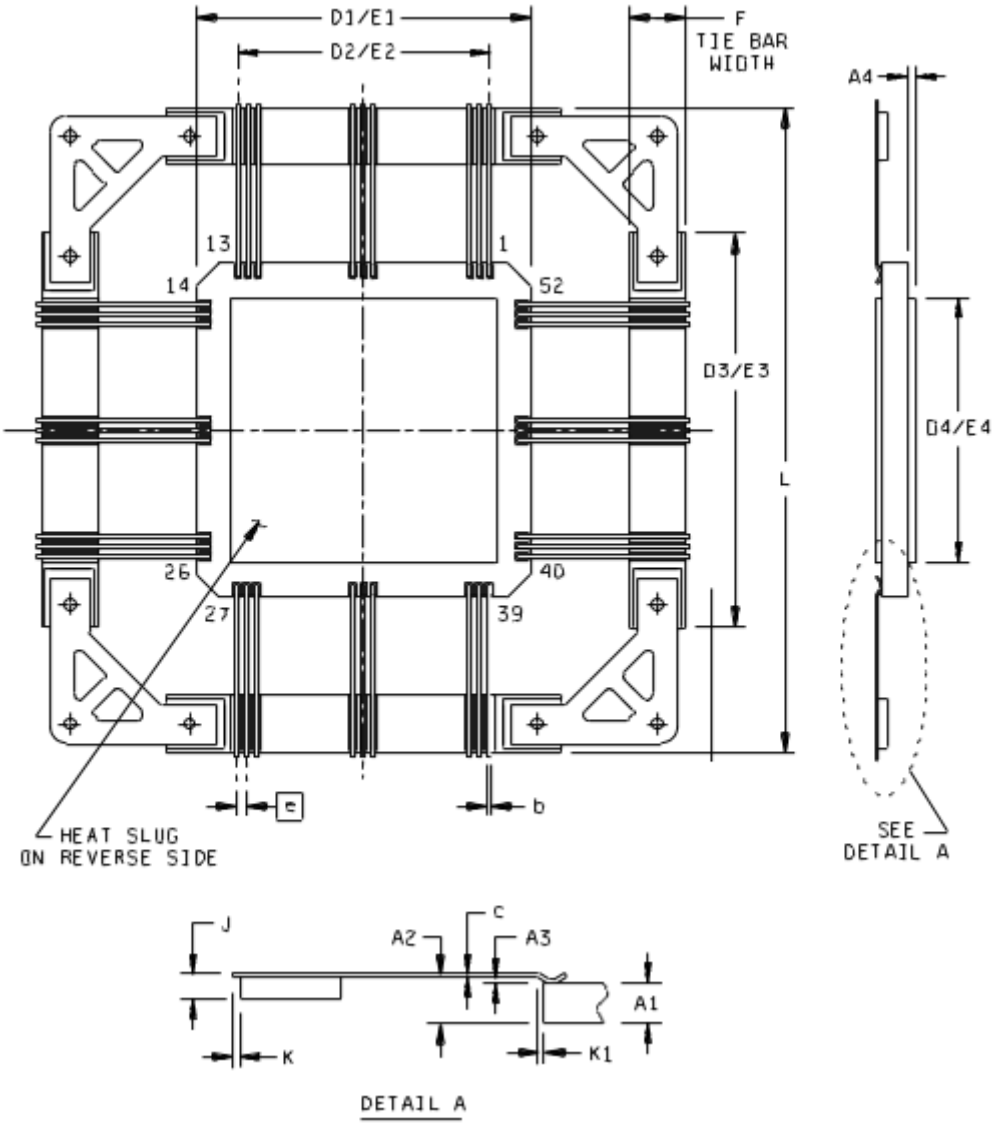


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-07206**
		REVISION LEVEL **B**	SHEET **11**

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	---	0.090	---	2.29
A2	---	0.115	---	2.92
A3	0.002	0.014	0.05	0.36
A4	0.03 BSC		0.762 BSC	
b	0.005	0.011	0.127	0.28
c	0.004	0.008	0.10	0.20
D1/E1	0.740	0.760	18.8	19.3
D2/E2	0.30 BSC		7.62 BSC	
D3/E3	1.198	1.222	30.43	31.04
D4/E4	0.630 BSC		16.0 BSC	
e	0.025 BSC		0.64 BSC	
F	0.175	0.225	4.44	5.72
J	0.029	0.042	0.75	1.05
K	---	0.020	---	0.51
K1	---	0.018	---	0.46
L	1.980	2.024	50.29	51.40
N	52			

NOTES:
1. Controlling dimensions are inches, millimeter dimensions are given for reference only.
2. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heat sink are connected to GND leads.

FIGURE 1. Case outline – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DRV_{DD}	27	GND
2	GND	28	AV_{DD}
3	V_{REF}	29	GND
4	GND	30	AV_{DD}
5	CLK	31	DNC
6	$\overline{CLK}$	32	OVR
7	GND	33	DRV_{DD}
8	AV_{DD}	34	GND
9	AV_{DD}	35	DMID
10	GND	36	D0 (LSB)
11	AIN	37	D1
12	$\overline{AIN}$	38	D2
13	GND	39	D3
14	AV_{DD}	40	D4
15	GND	41	D5
16	AV_{DD}	42	GND
17	GND	43	DRV_{CC}
18	AV_{DD}	44	D6
19	GND	45	D7
20	C1	46	D8
21	GND	47	D9
22	AV_{DD}	48	D10
23	GND	49	D11
24	C2	50	D12
25	GND	51	D13 (MSB)
26	AV_{DD}	52	DRY

FIGURE 2. Terminal connections.

Terminal symbol	Description
DRV_{DD}	3.3 V power supply, digital output stage only.
GND	Ground.
V_{REF}	2.4 V reference. Bypass to ground with 0.1 μF microwave chip capacitor.
CLK	Clock input. Conversion initiated on rising edge.
$\overline{CLK}$	Complemented of CLK, differential input.
AV_{DD}	5 V analog power supply.
AIN	Analog input.
$\overline{AIN}$	Complement of AIN, differential analog input.
C1	Internal voltage reference. Bypass to ground with a 0.1 μF chip capacitor.
C2	Internal voltage reference. Bypass to ground with a 0.1 μF chip capacitor.
DNC	Do not connect.
OVR	Over range bit. A logic level high indicates the analog input exceeds full scale.
DMID	Output data voltage midpoint. Approximately equal to (DV_{CC}) / 2.
D0 (LSB)	Digital output bit (least significant bit); twos complement.
D1 – D5, D6 – D12	Digital output bits in two's complement.
D13 (MSB)	Digital output bit (most significant bit); twos complement.
DRY	Data ready output.

FIGURE 2. Terminal connections – continued.

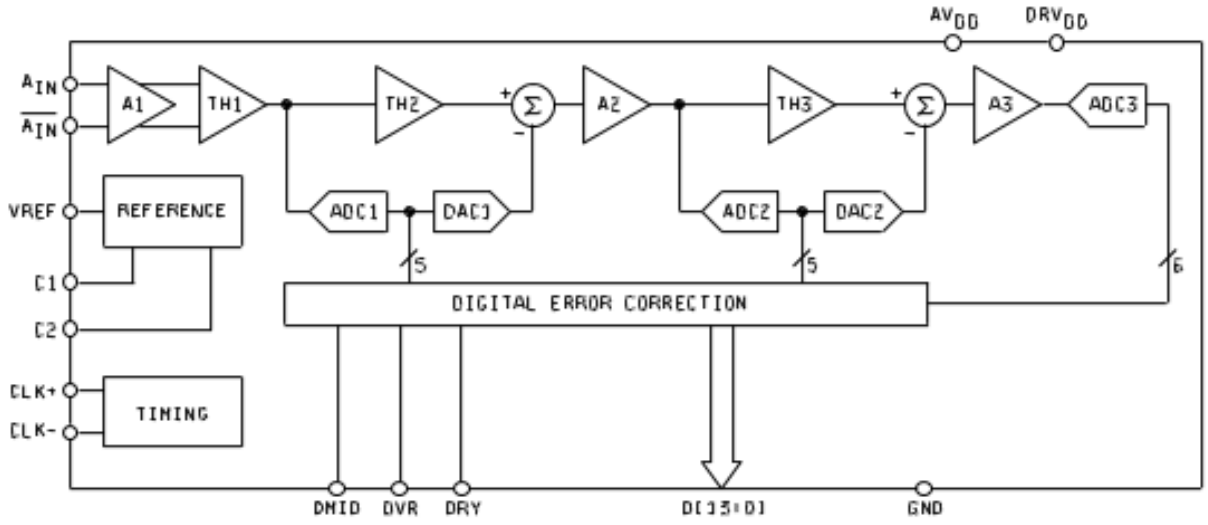


FIGURE 3. Block diagram.

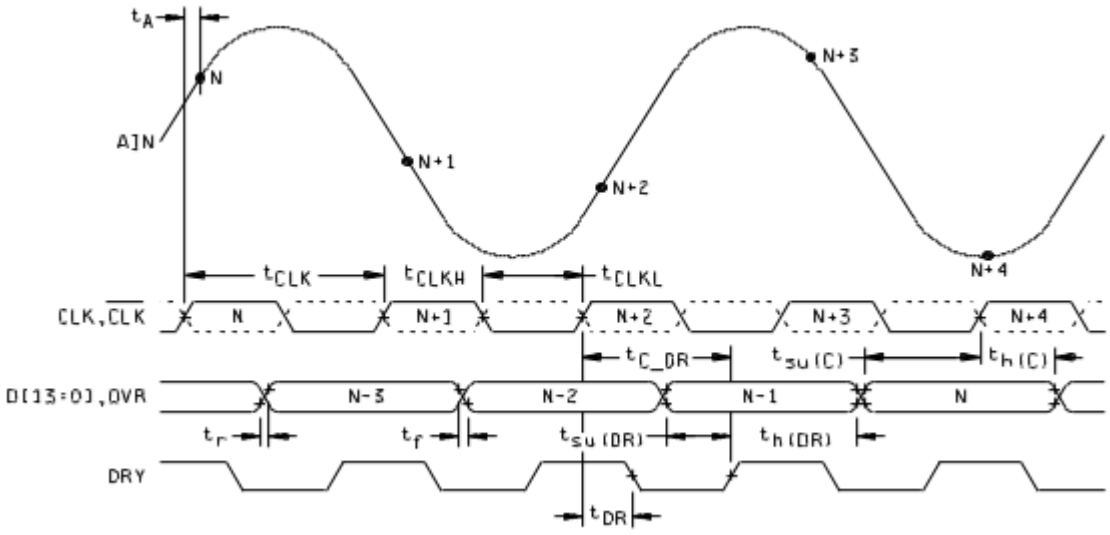


FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3, 4,5,6,9,10,11 1/	1,2,3, 4,5,6,9,10,11 1/ 2/
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1 2/
Group D end-point electrical parameters (see 4.4)	1	1
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.
2 Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters 1/	Symbol	Delta limits
Reference voltage	V_{REF}	±10 mV
Output buffer supply current	I_{DRVDD}	±4 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-05-18

Approved sources of supply for SMD 5962-07206 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0720601VXC	01295	ADS5424MHFG-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243