REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Vendor requested correction to Table IA; parameter (Write disable time - t_{WHWL}) from 1 ns to 2 ns minimum. – ksr	10-07-07	Charles F. Saffle
B	Added device types 05 and 06. Modified paragraphs 1.3, 1.4, and 1.5; also added new footnote for paragraph 1.5 and renumbered existing footnotes. Modified Table IA to incorporate device types 05 and 06. Editorial changes to boilerplate paragraphs. – ksr	11-03-07	Charles F. Saffle
C	Removed footnote from 1.2.2 and re-sequenced footnotes in sections 1.3 through 1.5. Updated RHA parametric limit of SEL and SEU in 1.5 and table IB. Changed minimum limit of t_{AVCL} from 200 ns to 400 ns and added t_{CHAV} and t_{CLAX} to Table IA. Revised EDAC Control register cycle timing waveform and related notes in Figure 5. Updated boilerplate for current requirements and removed all references to class M. – lht	13-05-13	Charles F. Saffle
D	Update radiation features in section 1.5 and SEP table IB. Update drawing to meet current MIL-PRF-38535 requirements. – glg	18-05-11	Charles F. Saffle
E	¶1.3: VEN revised max. voltages. Table I: VEN added t_{AVSK} and t_{AVET2} test conditions w/ new footnotes and added missing overbars to every 'E-controlled' test condition; Figure 5: VEN revised waveforms for SRAM Read Cycles. Re-sequenced table I footnotes, added missing units of measure in Conditions column of table I. update boilerplate to Section 508 Compliance, and current MIL-PRF-38535 requirements. – llb	23-10-03	James R. Eschmeyer
F	VEN editorial corrections to footnotes 10 – 12 of table I. – llb	24-05-02	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	F	F	F	F	F	F																
SHEET	23	24	25	26	27	28																
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
09-02-23

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

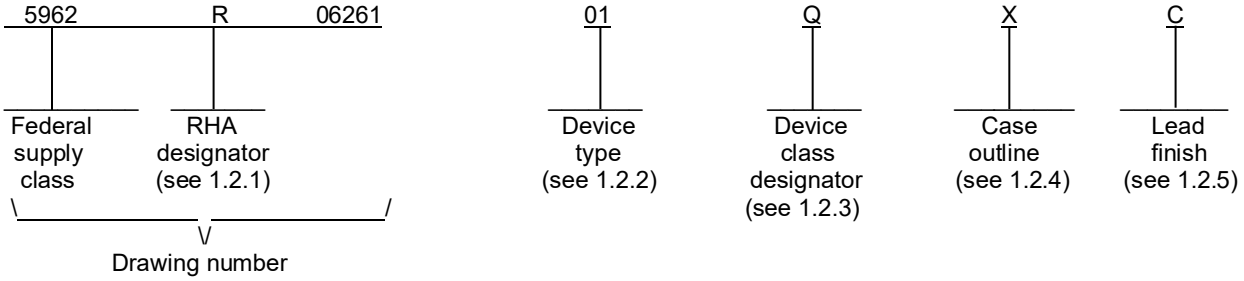
MICROCIRCUIT, MEMORY, DIGITAL, CMOS, RADIATION-HARDENED, 512K X 32-BIT (16MB) WITH EMBEDDED EDAC, LOW VOLTAGE SRAM, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL F	SIZE A	CAGE CODE **67268**	**5962-06261**
		SHEET	1 OF 28	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	UT8ER512K32M	512K X 32-bit CMOS SRAM (MIL-TEMP) master	20 ns
02	UT8ER512K32M	512K X 32-bit CMOS SRAM (EXTENDED-TEMP) master	20 ns
03	UT8ER512K32S	512K X 32-bit CMOS SRAM (MIL-TEMP) slave	20 ns
04	UT8ER512K32S	512K X 32-bit CMOS SRAM (EXTENDED-TEMP) slave	20 ns
05	UT8ER512K32M	512K X 32-bit CMOS SRAM (MIL-TEMP) master	20 ns
06	UT8ER512K32S	512K X 32-bit CMOS SRAM (MIL-TEMP) slave	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range, (V_{DD1})	-0.3 V dc to +2.4 V dc
Supply voltage range, (V_{DD2})	-0.3 V dc to +4.5 V dc
Voltage range on any pin	-0.3 V dc to +4.5 V dc
Input current, dc	± 10 mA
Power dissipation	5 W
Operating case temperature range, (T_C) Devices 01, 03, 05, 06	-55°C to +125°C
Devices 02, 04	-40°C to +125°C
Storage temperature range, (T_{STG})	-65°C to +150°C
Junction temperature, (T_J)	+150°C
Thermal resistance, junction-to-case, (θ_{JC}): Case X	+5°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{DD1})	+1.7 V dc to +1.9 V dc 3/
Supply voltage range, (V_{DD2})	+3.0 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to V_{DD2}
Operating case temperature range, (T_C) Devices 01, 03, 05, 06	-55°C to +125°C
Devices 02, 04	-40°C to +125°C

1.5 Radiation features.

Maximum total dose available:	
For device types 01-04 (dose rate = 50 - 300 rads(Si)/s):	100K Rad(Si) 4/
For device types 05-06 (effective dose rate = 1 rad(Si)/s)	100K Rad(Si) 5/
Single event phenomenon (SEP):	
No SEL at effective LET (see 4.4.4.3 and table IB)	≤ 111 MeV-cm^2/mg 6/ 7/
No SEU occurs at onset LET (see 4.4.4.3 and table IB)	< 0.8 MeV-cm^2/mg 7/ 8/
(Adam's 90% worst case environment SER = 8.1 x 10^{-16} errors/bit-day)	
Neutron irradiation	3.0 x 10^{14} n/cm^2

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values in this drawing are with respect to V_{SS}.
3/ For increased noise immunity, supply voltage (V_{DD1}) can be increased to 2.0 V. The parameters in Table IA, (Electrical performance characteristics) are guaranteed through characterization at V_{DD1} = 2.0 V dc. Unless otherwise specified.
4/ For device types 01 - 04 are irradiated at a dose rate = 50-300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and radiation end point limits for the noted parameters are guaranteed to a maximum total dose specified herein.
5/ For device types 05 - 06 are irradiated at a dose rate = 50-300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and radiation end point limits for the noted parameters are guaranteed to a maximum total dose specified herein. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A section 3.11.2. The total dose specification for these devices only applies to a low dose rate environment.
6/ Contact the device manufacturer for detailed lot information.
7/ Limits are guaranteed by design or process, but not production tested unless specified by customer in purchase order or contract.
8/ Assuming geosynchronous orbit, Adam's 90% worst environment and 152 KHz default scrub rate (97.0% SRAM availability) in terrestrial environment.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit for functional tests shall be as specified on Figure 4.

3.2.5 Tester timing characteristics and timing waveforms. The tester AC timing characteristics and timing waveforms shall be as specified on Figure 5 and applies to capacitance, read cycle, and write cycle measurements unless otherwise specified.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (devices 01, 03, 05, 06) $-40°C \le T_C \le +125°C$ (devices 02, 04) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}		1, 2, 3	All	.7 *V_{DD2}		V
Low-level input voltage	V_{IL}		1, 2, 3	All		.3 *V_{DD2}	V
High-level output voltage	V_{OH}	I_{OH} = -4mA, $V_{DD2} = V_{DD2}$ (min)	1, 2, 3	All	.8 *V_{DD2}		V
Low-level output voltage 2/	V_{OL}	I_{OL} = 8 mA, $V_{DD2} = V_{DD2}$ (min)	1, 2, 3	All		.2 *V_{DD2}	V
Input capacitance 3/	C_{IN}	f = 1 MHz @ 0 V, see 4.4.1e	4	All		12	pF
Bidirectional I/O capacitance 3/	C_{IO}		4	All		12	pF
Input leakage current	I_{IN}	$V_{IN} = V_{DD2}$ and V_{SS}	1, 2, 3	All	-2	2	µA
Three state output leakage current 4/	I_{OZ}	$V_O = V_{DD2}$ and V_{SS}, $V_{DD2} = V_{DD2}$ (max), $\overline{G} = V_{DD2}$ (max)	1, 2, 3	All	-2	2	µA
Short-circuit output current 5/ 6/	I_{OS}	$V_{DD2} = V_{DD2}$ (max), $V_O = V_{DD2}$ $V_{DD2} = V_{DD2}$ (max), $V_O = V_{SS}$	1, 2, 3	All	-100	100	mA
Supply current operating @ 1 MHz 7/ 8/	$I_{DD1}^{(OP1)}$	Inputs: $V_{IL} = V_{SS}$ + 0.2 V $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)	1, 3	All		25	mA
		Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA, $V_{DD2} = V_{DD2}$ (max) V_{DD1} = 1.9 V	2			65 9/	
		V_{DD1} = 2.0 V	2			70 9/ 10/	
Supply current operating @ 50.0 MHz 7/ 8/	$I_{DD1}^{(OP2)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA, $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)	1, 3	All		250	mA
		Inputs: $V_{IL} = V_{SS}$ + 0.2 V $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA, $V_{DD2} = V_{DD2}$ (max) V_{DD1} = 1.9 V	2			270 9/	
		V_{DD1} = 2.0 V	2			300 9/ 10/	
Supply current operating @ 1 MHz 7/ 8/	$I_{DD2}^{(OP1)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA, $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)	1, 2, 3	All		2	mA
Supply current operating @ 50.0 MHz 7/ 8/	$I_{DD2}^{(OP2)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 mA, $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)	1, 2, 3	All		5	mA
Functional test		See 4.4.1c, T_C = 25°C	7, 8A, 8B	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55ºC ≤ T_C ≤ +125ºC (devices 01, 03, 05, 06) -40ºC ≤ T_C ≤ +125ºC (devices 02, 04) +1.7 V ≤ V_{DD1} ≤ +1.9 V +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current standby	I_{DD1}(SB)	CMOS inputs, I_{OUT} = 0 mA, V_{IL} = 0 V,	1, 3	All		25	mA
@ 0 MHz EDAC bypassed		$\overline{E}$ = V_{DD2} -0.2 V, V_{IH} = V_{DD2}(max),	2			70 9/	
	I_{DD2}(SB)	V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	1, 2, 3			2	mA
Supply current standby	I_{DD1}(SB)	CMOS inputs, I_{OUT} = 0 mA, V_{IL} = 0 V,	1, 3	All		25	mA
A(18:0) @ 50.0 MHz		$\overline{E}$ = V_{DD2} -0.2 V, V_{IH} = V_{DD2}(max),	2			70 9/	
EDAC bypassed	I_{DD2}(SB)	V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	1, 2, 3			2	mA
Read cycle time 3/ 11/	t_{AVAV}	See figures 4 and 5 as applicable	9, 10, 11	All	20		ns
Address valid to address valid skew time 12/	t_{AVSK}		9, 10, 11	05, 06		4	ns
Read access time	t_{AVQV}		9, 10, 11	All		20	ns
Output hold time 13/	t_{AXQX}		9, 10, 11	All	3		ns
$\overline{G}$-controlled output enable time 3/ 13/	t_{GLQX}		9, 10, 11	All	2		ns
$\overline{G}$-controlled read access time	t_{GLQV}		9, 10, 11	All		8	ns
$\overline{G}$-controlled output three-state time 13/	t_{GHQZ}		9, 10, 11	All	2	6	ns
$\overline{E}$-controlled output enable time 13/ 14/	t_{ETQX}		9, 10, 11	All	5		ns
$\overline{E}$-controlled address setup time for read 12/	t_{AVET2}		9, 10, 11	05, 06	-4		ns
$\overline{E}$-controlled accessed time 14/	t_{ETQV}		9, 10, 11	All		20	ns
$\overline{E}$-controlled output three-state time 15/	t_{EFQZ}		9, 10, 11	All	2	7	ns
Address to error flag valid	t_{AVMV}		9, 10, 11	All		20	ns
Address to error flag hold time from address change 13/	t_{AXMX}		9, 10, 11	All	3		ns
$\overline{G}$-controlled error flag enabled time 13/	t_{GLMX}		9, 10, 11	All	2		ns
$\overline{G}$-controlled error flag valid	t_{GLMV}		9, 10, 11	All		7	ns
$\overline{E}$-controlled error flag enable time 14/	t_{ETMX}		9, 10, 11	All	5		ns
$\overline{E}$-controlled error flag time 14/	t_{ETMV}		9, 10, 11	All		20	ns
$\overline{G}$-controlled error flag three-state time 13/	t_{GHMZ}		9, 10, 11	All	2	6	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55ºC ≤ T_C ≤ +125ºC (devices 01, 03, 05, 06) -40ºC ≤ T_C ≤ +125ºC (devices 02, 04) +1.7 V ≤ V_{DD1} ≤ +1.9 V +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time 16/	t_{AVAV2}	See figure 4 and 5 as applicable, $\overline{G}$ = V_{DD2}	9, 10, 11	All	10		ns
Device enable to end of write 14/	t_{ETWH}	See figures 4 and 5 as applicable	9, 10, 11	All	10		ns
Address set-up time for write ($\overline{E}$-controlled) 14/	t_{AVET}		9, 10, 11	All	0		ns
Address set-up time for write ($\overline{W}$-controlled)	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width 16/	t_{WLWH}		9, 10, 11	All	8		ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	All	0		ns
Address hold time for device enable ($\overline{E}$-controlled) 15/	t_{EFAX}		9, 10, 11	All	0		ns
$\overline{W}$-controlled three-state time 13/	t_{WLQZ}		9, 10, 11	All		7	ns
$\overline{W}$-controlled output enable time 13/	t_{WHQX}		9, 10, 11	All	3		ns
Device enable pulse width ($\overline{E}$-controlled) 14/ 15/	t_{ETEF}		9, 10, 11	All	10		ns
Data set-up time	t_{DVWH}		9, 10, 11	All	5		ns
Data hold time	t_{WHDX}		9, 10, 11	All	2		ns
Device enable controlled write pulse width 15/ 16/	t_{WLEF}		9, 10, 11	All	8		ns
Data set-up time 15/	t_{DVEF}		9, 10, 11	All	5		ns
Data hold time 15/	t_{EFDX}		9, 10, 11	All	2		ns
Address valid to end of write	t_{AVWH}		9, 10, 11	All	10		ns
Write disable time 16/	t_{WHWL}	See figure 4 and 5 as applicable, $\overline{G}$ = V_{DD2}	9, 10, 11	All	2		ns
Master mode AC characteristics							
User programmable BUSY low to $\overline{SCRUB}$ low 17/	t_{BLSL}	See figures 4 and 5 as applicable	9, 10, 11	All	50n	90n +1	ns
$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	t_{SLSH1}		9, 10, 11	All	200	350	ns
$\overline{SCRUB}$ high to $\overline{BUSY}$ high	t_{SHBH}		9, 10, 11	All	50	85	ns
Scrub rate period 18/	t_{SCRT}		9, 10, 11	All	2^n50 +200	2^n90 +350	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (devices 01, 03, 05, 06) $-40°C \le T_C \le +125°C$ (devices 02, 04) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slave mode AC characteristics							
$\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave)	t_{SLSH2}	See figures 4 and 5 as applicable	9, 10, 11	All	200		ns
$\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave) 19/	t_{SHSL}		9, 10, 11	All	400		ns
EDAC control register AC characteristics							
Address valid to address valid for control register cycle	t_{AVAV3}	See figures 4 and 5 as applicable	9, 10, 11	All	200		ns
Address valid to control low	t_{AVCL}		9, 10, 11	All	400		ns
Address valid to enable valid	t_{AVEX}		9, 10, 11	All	200		ns
Address to data valid control register read	t_{AVQV3}		9, 10, 11	All		400	ns
MBE high to address valid	t_{CHAV}		9, 10, 11	All	0		ns
MBE low to address invalid	t_{CLAX}		9, 10, 11	All	0		ns
MBE control EDAC disable time 13/	t_{MLQX}		9, 10, 11	All	3		ns
Output tri-state time 13/	t_{GHQZ3}		9, 10, 11	All	2	9	ns
MBE low to output enable 19/	t_{MLGL}		9, 10, 11	All	85		ns

1/ Devices Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.
2/ The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for the master device (device types 01, 02, and 05) are tested functionally for V_{OL} specification.
3/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in Table IA.
4/ The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for the master device (device types 01, 02, and 05) are guaranteed by design, but neither tested nor characterized.
5/ Supplied as a design limit but not guaranteed or tested.
6/ Not more than one output may be shorted at a time, for a maximum duration of one second.
7/ EDAC enabled. Default Scrub Rate Period applicable to master device (device types 01, 02, and 05) only.
8/ Operating current limit includes standby current.
9/ Specified post-irradiation value.
10/ Limit for V_{DD1} (max) = 2.0 V reference note 4/ section 1.4 herein.
11/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation.
12/ Guaranteed by design.
13/ Three-state is defined as a 300mV change from steady-state output voltage.
14/ The ET (enable true) notation refers to the latter active edge of $\overline{E1}$ or E2. SEU immunity does not affect the read parameters.
15/ The EF (enable false) notation refers to the leading de-active edge of $\overline{E1}$ or E2. SEU immunity does not affect the read parameters.

TABLE IA. Electrical performance characteristics – Continued.

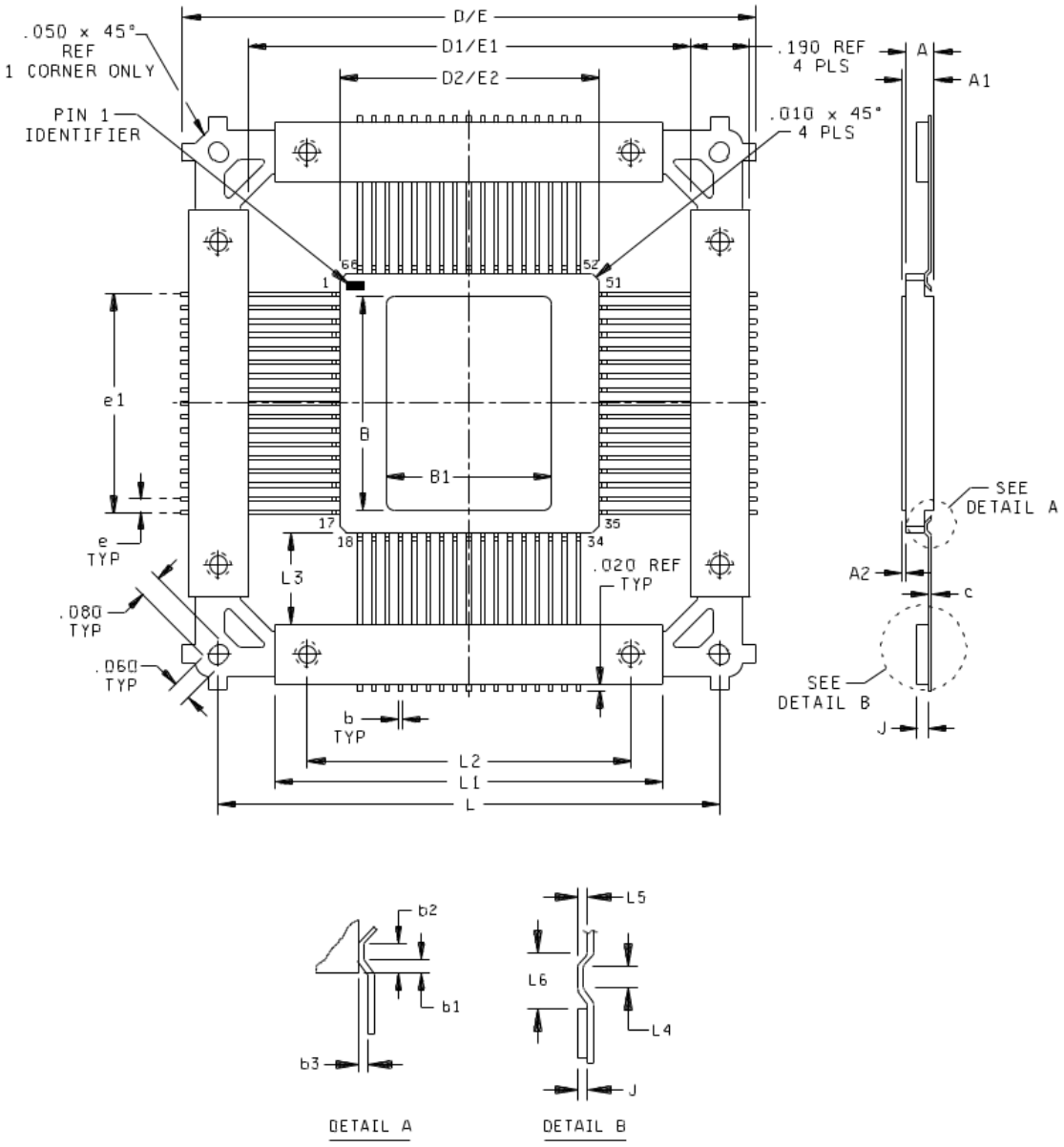
16/ Test performed with $\overline{G}$ high.
17/ The value n is decimal equivalent of hexadecimal value 0x0 through 0xF programmed into control register address bits A_4-A_7 by user. Default value for n = 10.
18/ The value n is decimal equivalent of hexadecimal value 0x3 through 0xF programmed into control register address bits A_0-A_3 by user. Default value for n = 7.
19/ Guaranteed by design, neither tested nor characterized.

Table IB. SEP test limits 1/ 2/ 3/

Device type	Single Event Upset 4/ V_{DD1} = 1.7 V, V_{DD2} = 3.0 V		Single Event Latch-up 5/ Bias V_{DD1} = 2.0 V, V_{DD2} = 3.6 V
	Onset LET No upsets 6/ [MeV/(mg/cm^2)]	Maximum device Cross section	Effective LET No latch-up [MeV/(mg/cm^2)]
All	LET < 0.8	7.5 x10^{-8} cm^2	LET ≤ 111

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Heavy ion SEE test performed at fluence level=1 x 10^7 ions/cm2 under worst case conditions at an angle of incidence from normal (0°) to maximum 60°. For detailed SEE test information contact the device manufacturer.
4/ Worst case test temperature T_A = +25°C ±10°C.
5/ Worst case test temperature T_A = +125°C ±10°C.
6/ Soft error rate = 8.1 x 10^{-16} error/bit-day assuming Adam's 90% worst case environment, geosynchronous orbit, 100 mil aluminum shielding, and a default scrub frequency of 156khz. Contact the device manufacturer for detailed information.

Case outline X



Notes follow dimension table.

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-06261**
		REVISION LEVEL F	SHEET **11**

Case outline X – Continued.

Symbol	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.26	2.54	2.82	.089	.100	.111
A1	2.54	2.92	3.30	.100	.115	.130
A2	0.30	0.38	0.46	.012	.015	.018
B		20.65			.813	
B1		20.65			.813	
b		0.38			.015 Typ.	
b1		0.46			.018 Ref.	
b2		0.76			.030 Ref.	
b3		0.20			.008	
c		0.20			.008	
c1	0.76	0.89	1.02	.030	.035	.040
D/E			51.99			2.047
D1/E1	40.13	40.64	41.15	1.580	1.600	1.620
D2/E2	24.66	24.89	25.12	.971	.980	.989
e		1.27			0.050	
e1		20.32			0.800	
J	0.76	0.89	1.02	.030	.035	.040
L	45.03	45.47	45.90	1.773	1.790	1.807
L1		35.81			1.410 Ref.	
L2	30.20	30.48	30.76	1.189	1.200	1.211
L3		7.87			.310 Typ.	
L4		1.27 Ref.			.050 Ref.	
L5			0.89			.035
L6			2.54			.100

1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over nickel.
3. Package lid is electrically connected to V_{SS} for package X.
4. Tie bar measurements are for reference only.
5. Package may be shipped with repaired leads (see detail B).

FIGURE 1. Case outline – Continued.

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DQ0	35	DQ31
2	DQ1	36	DQ30
3	DQ2	37	DQ29
4	DQ3	38	DQ28
5	DQ4	39	DQ27
6	DQ5	40	DQ26
7	DQ6	41	DQ25
8	DQ7	42	DQ24
9	V_{SS}	43	V_{SS}
10	DQ8	44	DQ23
11	DQ9	45	DQ22
12	DQ10	46	DQ21
13	DQ11	47	DQ20
14	DQ12	48	DQ19
15	DQ13	49	DQ18
16	DQ14	50	DQ17
17	DQ15	51	DQ16
18	V_{DD1}	52	V_{DD1}
19	A11	53	A10
20	A12	54	A9
21	A13	55	A8
22	A14	56	A7
23	A15	57	A6
24	A16	58	$\overline{W}$
25	$\overline{E1}$	59	A18
26	$\overline{G}$	60	V_{SS}
27	E2	61	A17
28	V_{DD2}	62	A5
29	V_{SS}	63	A4
30	$\overline{SCRUB}$	64	A3
31	$\overline{BUSY}$	65	A2
32	MBE	66	A1
33	V_{DD2}	67	A0
34	V_{SS}	68	V_{SS}

FIGURE 2. Terminal connections.

SRAM Device Control Operation Truth Table

$\overline{G}$	$\overline{W}$	E2	$\overline{E1}$	I/O Mode	Mode
X	X	X	H	DQ(31:0) 3-state	Standby
X	X	L	X	DQ(31:0) 3-state	Standby
L	H	H	L	DQ(31:0) Data Out	Word Read
H	H	H	L	DQ(31:0) All 3-state	Word Read (see note 2)
X	L	H	L	DQ(31:0) Data In	Word Write

Notes:
1. X is defined as a “don’t care” condition.
2. Device active; outputs disabled.

EDAC Control Pin Operation Truth Table

MBE	$\overline{SCRUB}$	$\overline{BUSY}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

Notes:
1. X is defined as a “don’t care” condition.
2. $\overline{BUSY}$ signal is a NC for slave device and is an X (don’t care).

FIGURE 3. Truth Tables.

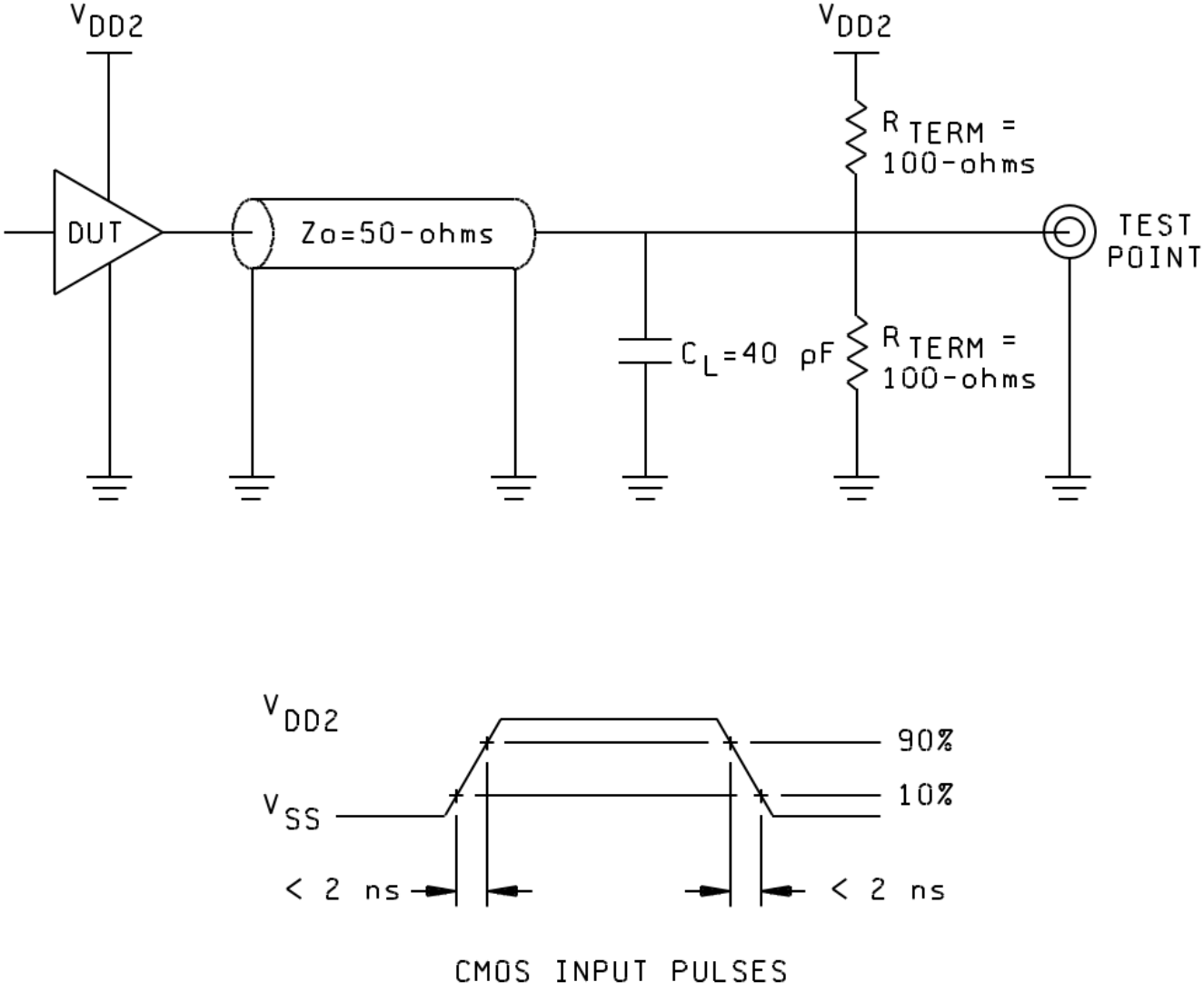
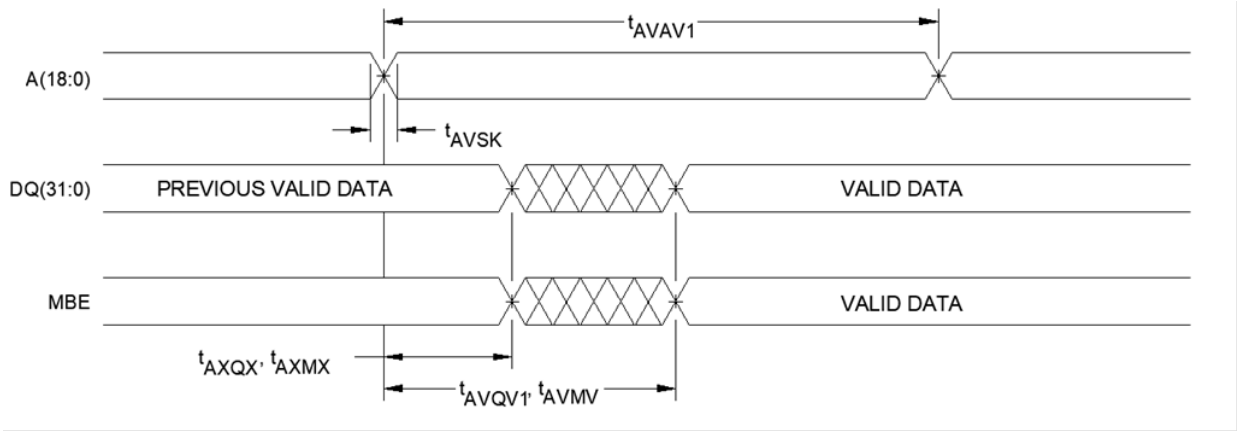
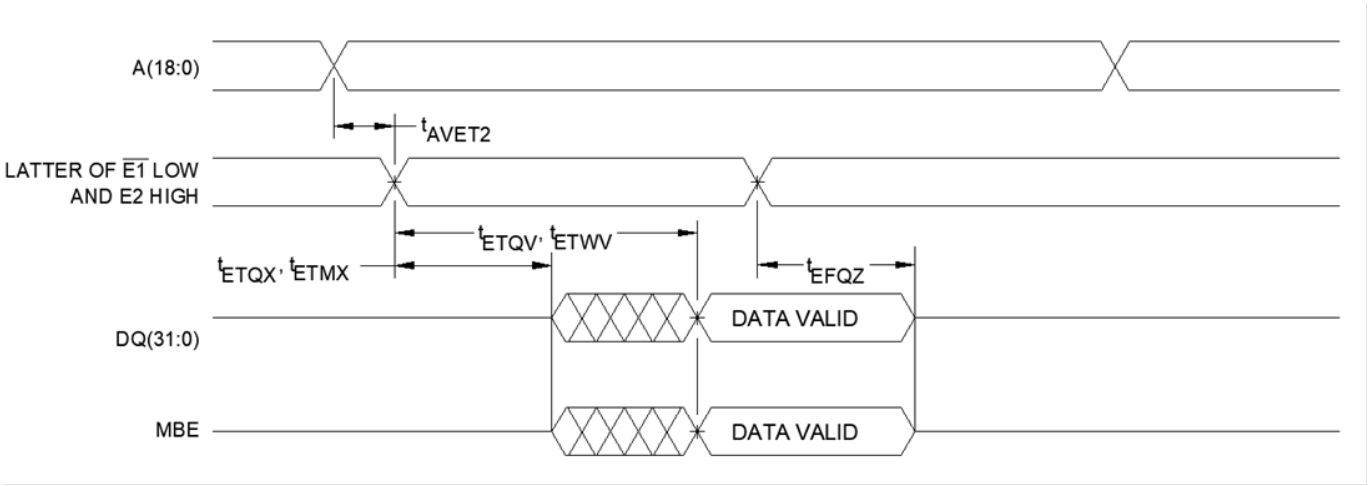


FIGURE 4. AC Test Load Circuit and Input Waveform.



1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

SRAM read cycle 1: Address Access

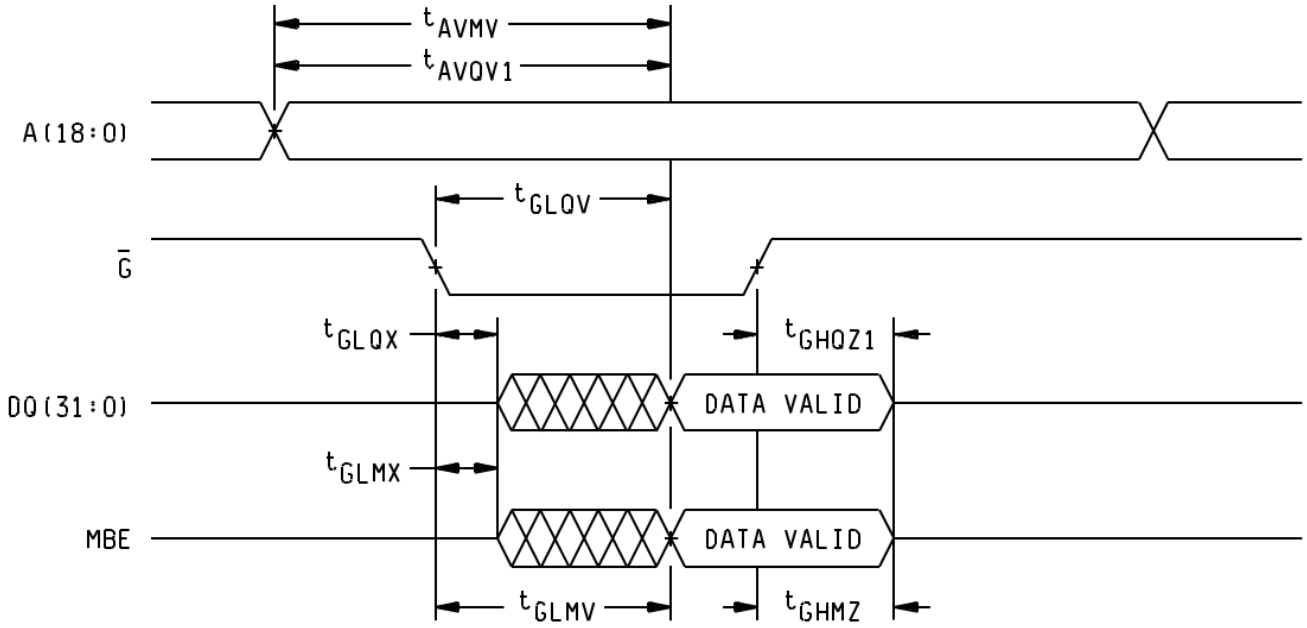


Notes:

1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

SRAM read cycle 2: Chip enable Access

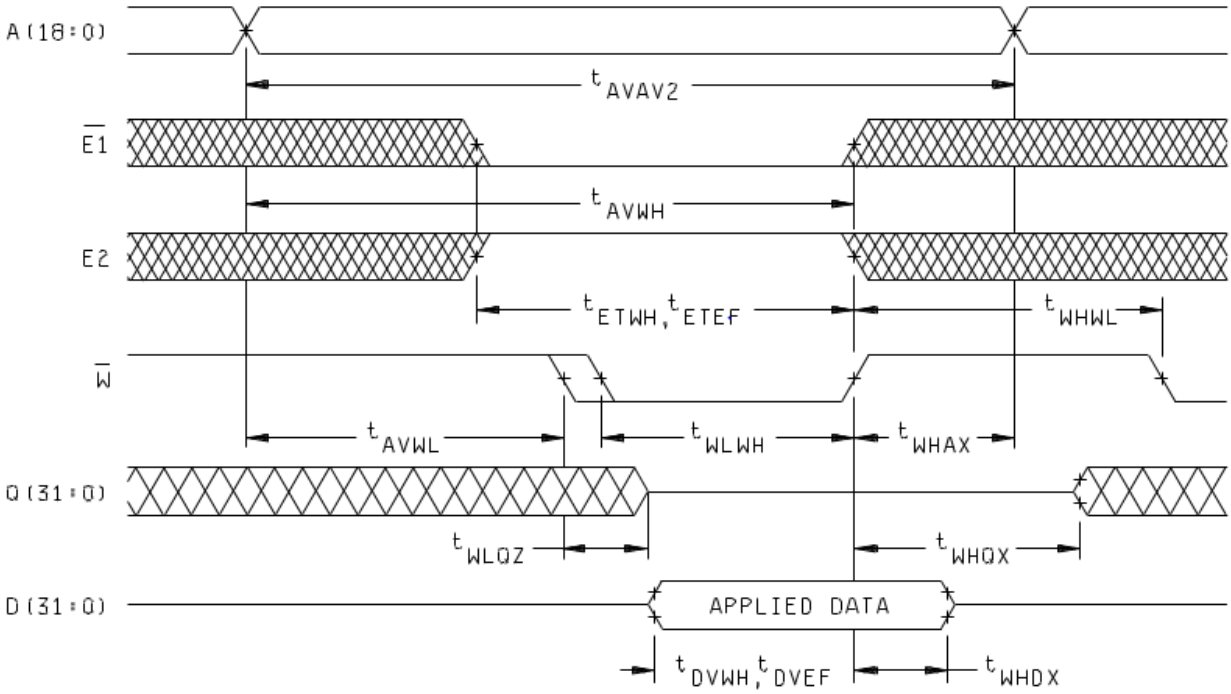
FIGURE 5. Timing waveforms.



Notes:
1. $\overline{E1} \le V_{IL}$ (max) and E2 and $\overline{W} \ge V_{IH}$ (min)
2. $\overline{SCRUB} \ge V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

SRAM read cycle 3: Output Enable Access.

FIGURE 5. Timing waveforms – Continued.

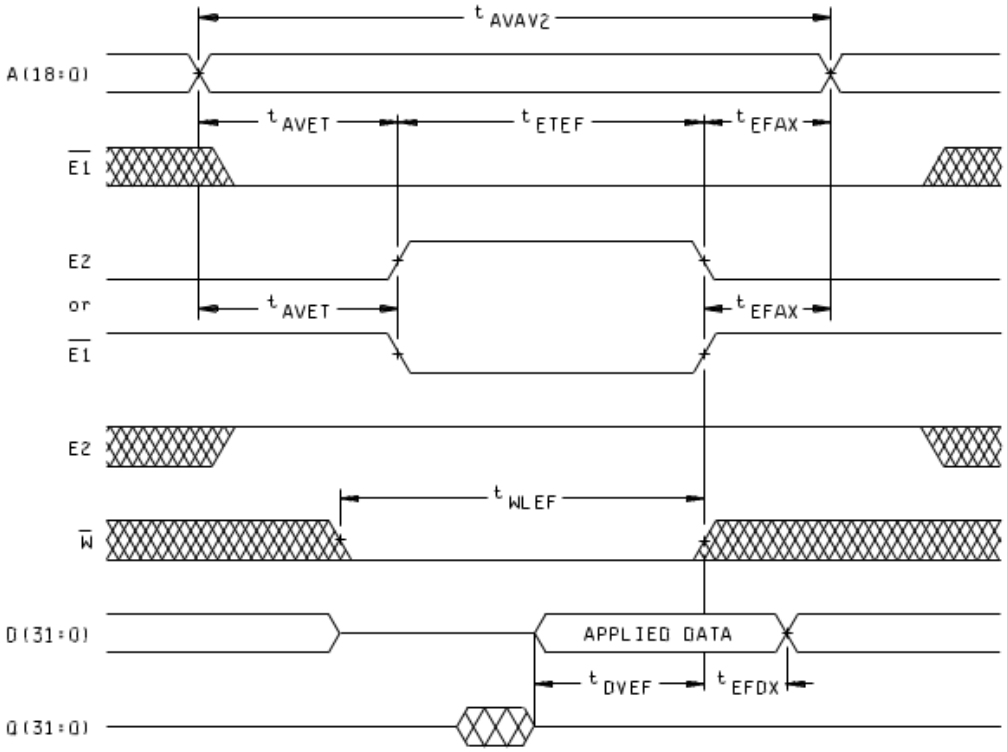


Notes:

1. $\overline{G} \le V_{IL}$ (max) (If $\overline{G} \ge V_{IH}$ (min) then Q(31:0) and MBE will be three-state for the entire cycle)
2. $\overline{SCRUB} \ge V_{OH}$ (min)

SRAM write cycle 1: $\overline{W}$-controlled Access

FIGURE 5. Timing waveforms – Continued.

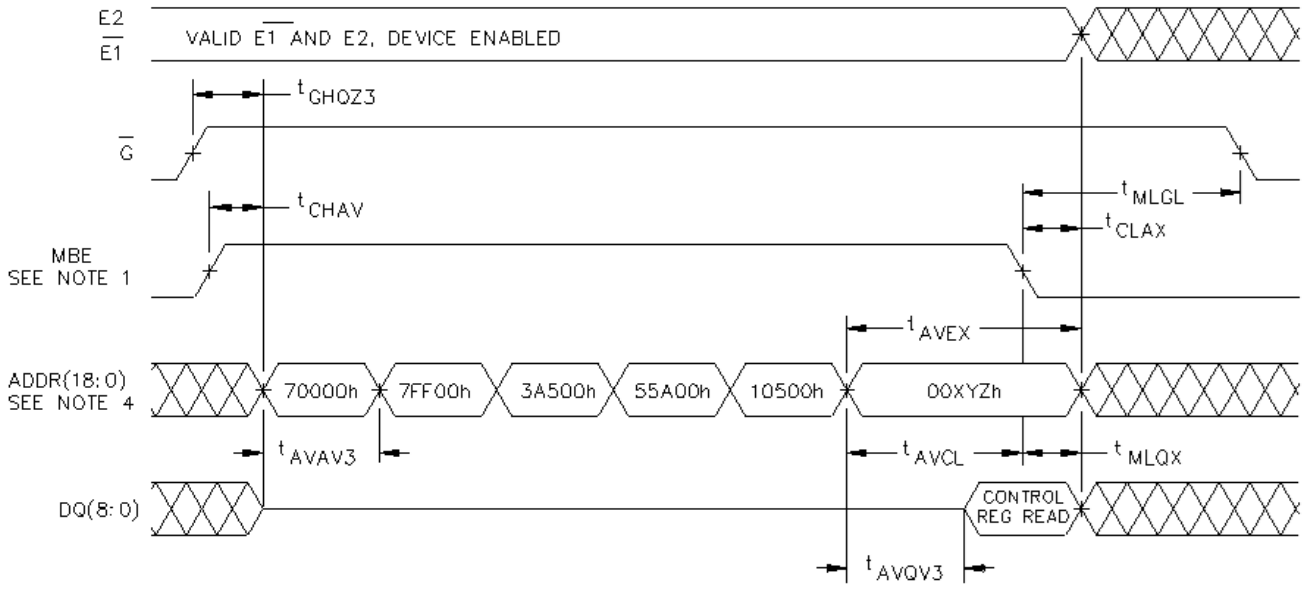


Notes:

1. $\overline{G} \leq V_{IL}$ (max) (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be three-state for the entire cycle)
2. Either $\overline{E1}$ / E2 scenario can occur.
3. $\overline{SCRUB} \geq V_{OH}$ (min)

SRAM write cycle 2: Enabled-controlled Access

FIGURE 5. Timing waveforms – Continued.

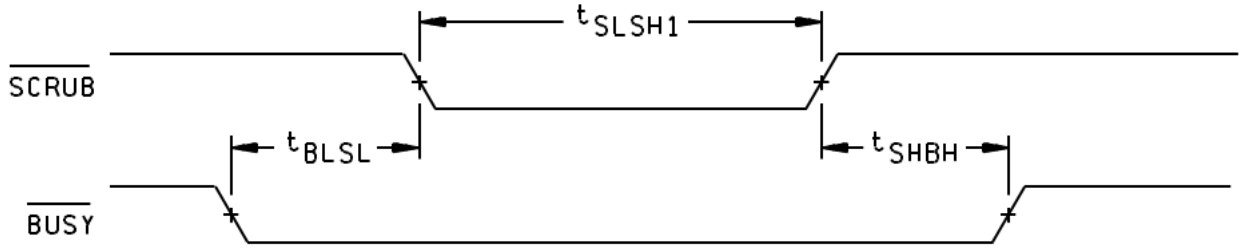


Notes:

1. MBE is driven high by the user.
2. Lower 10 bits of the last address are used to read or configure the control register (see vendor data sheet).
3. $\overline{\text{SCRUB}} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{\text{SCRUB}}$ during configuration cycle.
4. Device must see a transition to address 70000h coincident or subsequent to MBE assertion.

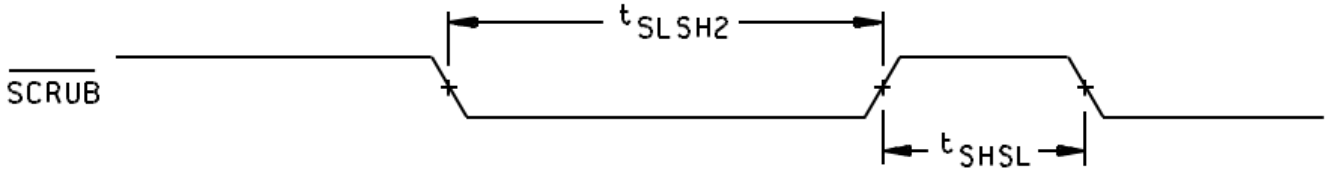
EDAC Control register cycle

FIGURE 5. Timing waveforms – Continued.



Note: The conditions pertain to Read or Write.

Master mode SCRUB cycle

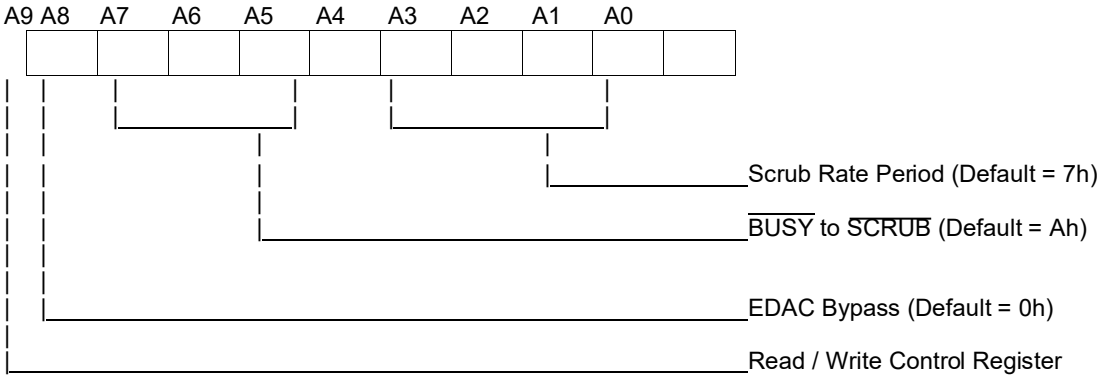


Note: The conditions pertain to both Read or Write.

Slave mode SCRUB cycle

FIGURE 5. Timing waveforms – Continued.

EDAC Control Register



EDAC Programming Configuration table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 – 3)	Scrub Rate Period [1, 2, 3]	3 – 15 Note: 0 -2 reserved	As SCRUB rate changes from 0 – 15, then the interval between SCRUB cycles will change as follows: 3 = 0.6 μs 8 = 13.0 μs 12 = 205 μs 4 = 1.0 μs 9 = 25.8 μs 13 = 410 μs (see note 4) 5 = 1.8 μs 10 = 51.4 μs 14 = 819 μs (see note 4) 6 = 3.4 μs 11 = 102.6 μs 15 = 1.64 ms (see note 4) 7 = 6.6 μs
A (4 – 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ [2, 3, 5]	0 - 15	If $\overline{\text{BUSY}}$ changes from 0 – 15, then the interval t_{BLSL} between $\overline{\text{SCRUB}}$ and BUSY will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250 ns
A (8)	Bypass EDAC Bit [6]	0, 1	If 0, then normal EDAC operation will occur If 1, then EDAC will be bypassed
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

Notes:

1. Default Scrub Rate Period is 6.6 μs.
2. Values based on minimum specification limits. For guaranteed ranges of Scrub Rate Period (t_{SCRT}) and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ t_{BLSL} reference the Master mode AC characteristic tables.
3. Scrub Rate Period and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$, applicable to master device types 01, 02, and 05 only.
4. Period below test capability.
5. The default for t_{BLSL} is 500 ns.
6. The default state for A8 is 0.

FIGURE 6. EDAC Configuration.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Static burn-in (method 1015)	Not required	Required
Interim electrical parameters (see 4.2)		1*, 7* Δ
Dynamic burn-in (method 1015)	Required	Required
Interim electrical parameters (see 4.2)		1*, 7* Δ
Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limit	Unit
Supply current standby at 0 MHz EDAC bypassed $I_{DD1(SB)}$ and $I_{DD2(SB)}$	± 10% or 35 μA whichever is greater 2/	mA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ If device is tested at or below 35 μA, no deltas are required.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A for devices 01 – 04; and for device types 05 and 06 total dose irradiation performed at condition A and section 3.11.2 of method 1019 and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019 condition A for devices 01 – 04; and condition A with Extended Room Temperature Anneal, for devices 05 and 06, and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C

4.4.4.2 Neutron testing. When specified in the purchase order or contract, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., 0° ≤ angled ≤ 60 degrees). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2

c. The flux shall be between 10^2 and 10^6 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature +125°C.

f. Bias conditions shall be V_{DD1} = 1.7 V and V_{DD2} = 3.0 V dc for the upset measurements; V_{DD1} = 2.0 V and and V_{DD2} = 3.6 V dc for the latch-up measurements.

g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test condition of (SEP).

b. Number of upsets (SEU).

c. Occurrence of latch-up (SEL).

APPENDIX A
Appendix A forms a part of SMD 5962-06261

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-02

Approved sources of supply for SMD 5962-06261 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0626101QXA	3/	UT8ER512K32M-21WCA
5962R0626101QXC	3/	UT8ER512K32M-21WCC
5962R0626101VXA	3/	UT8ER512K32M-21WCA
5962R0626101VXC	3/	UT8ER512K32M-21WCC
5962R0626102QXA	3/	UT8ER512K32M-21WWA
5962R0626102QXC	3/	UT8ER512K32M-21WWC
5962R0626102VXA	3/	UT8ER512K32M-21WWA
5962R0626102VXC	3/	UT8ER512K32M-21WWC
5962R0626103QXA	3/	UT8ER512K32S-21WCA
5962R0626103QXC	3/	UT8ER512K32S-21WCC
5962R0626103VXA	3/	UT8ER512K32S-21WCA
5962R0626103VXC	3/	UT8ER512K32S-21WCC
5962R0626104QXA	3/	UT8ER512K32S-21WWA
5962R0626104QXC	3/	UT8ER512K32S-21WWC
5962R0626104VXA	3/	UT8ER512K32S-21WWA
5962R0626104VXC	3/	UT8ER512K32S-21WWC
5962R0626105QXA	65342	UT8ER512K32M-21WCA
5962R0626105QXC	65342	UT8ER512K32M-21WCC
5962R0626105VXA	65342	UT8ER512K32M-21WCA
5962R0626105VXC	65342	UT8ER512K32M-21WCC
5962R0626106QXA	65342	UT8ER512K32S-21WWA
5962R0626106QXC	65342	UT8ER512K32S-21WWC
5962R0626106VXA	65342	UT8ER512K32S-21WWA
5962R0626106VXC	65342	UT8ER512K32S-21WWC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Frontgrade Colorado Springs LLC 4350 Centennial Blvd. Colorado Springs, CO 80907-7370