REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes on sheet 6 test I_{DDQ} and sheet 7 test ΔI_{DDQ}. - LTG	07-04-17	Thomas M. Hess
B	Update figure 5 switching waveforms to data sheet. - LTG	09-07-08	Thomas M. Hess
C	Update electrical test requirements in table IIA for group C and D. Update radiation features in section 1.5 and table IB. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - MAA	11-06-23	David J. Corbett
D	Add equivalent test circuits and footnote 2 to figure 5. Delete class M requirements per updated boilerplate paragraphs. - MAA	12-11-08	Thomas M. Hess
E	Update vendor CAGE 65342 information. Update boilerplate to MIL-PRF-38535 requirements. - DRH	21-09-22	Muhammad A. Akbar

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
06-12-21

REVISION LEVEL
E

SIZE
A

CAGE CODE
67268

5962-06240

SHEET 1 OF 23

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

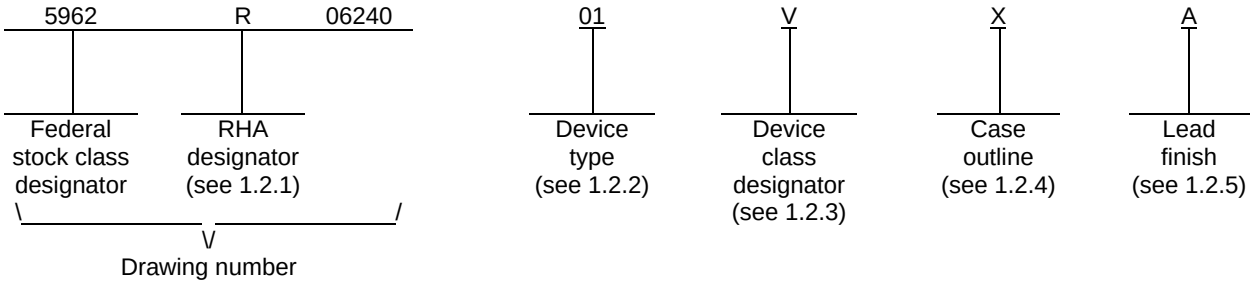
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, RADIATION HARDENED, 9-BIT LATCHABLE TRANSCEIVER WITH PARITY GENERATOR/ CHECKER WITH NON-INVERTING THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND OUTPUTS, MONOLITHIC SILICON

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTS899	9-bit latchable transceiver with parity generator/checker with non-inverting three-state outputs, TTL compatible inputs and outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1.	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +6.0 V dc
Voltage on any pin during operation ($V_{I/O}$)	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current (I_{IN})	±10 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J)	+175°C
Thermal resistance junction-to-case (θ_{JC})	20°C/W
Maximum power dissipation (P_D)	220 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage on any pin (V_{IN})	0.0 V dc to V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time (t_r, t_f)	20 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 to 300 rad(Si)/s)	100 Krad (Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.5)	≤ 108 MeV/(mg/cm^2) 2/
No SEU occurs at effective LET (see 4.4.4.5)	≤108 MeV/(mg/cm^2) 2/
Neutron fluence	1.0x10^{14} n/cm^2 2/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM F1192- Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org/.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JESD 78 – IC Latch-Up Test

(Copies of these documents are available online at https://www.jedec.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Function table. The function table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level input voltage 2/	V_{IH}			1, 2, 3	All	2.0		V
Low level input voltage 2/	V_{IL}			1, 2, 3	All		0.8	V
Positive input clamp Voltage	V_{IC+}	For input under test I_{IN} = +18 mA, V_{DD} = 0.0 V		1, 2, 3	All	0.4	1.5	V
Negative input clamp Voltage	V_{IC-}	For input under test I_{IN} = -18 mA, V_{DD} = open		1, 2, 3	All	-1.5	-0.4	V
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}		1, 2, 3	All	-1.0	1.0	µA
High level output voltage	V_{OH1}	V_{IN} = 2.0 V or 0.8 V	I_{OH} = -24 mA	1, 3	All	V_{DD} – 0.64		V
			I_{OH} = -24 mA	2		V_{DD} – 0.8		
			I_{OH} = -100 µA	1, 2, 3		V_{DD} – 0.2		
High level output voltage 3/	V_{OH2}	I_{OH} = -50 mA V_{IN} = 2.0 V or 0.8 V V_{DD} = 5.5 V		1, 3	All	V_{DD} -1.1		V
				2		V_{DD} -1.25		
Low level output voltage	V_{OL1}	V_{IN} = 2.0 V or 0.8 V	I_{OL} = 24 mA	1, 3	All		0.4	V
			I_{OL} = 24 mA	2			0.5	
			I_{OL} = 100 µA	1, 2, 3			0.2	
Low level output voltage 3/	V_{OL2}	I_{OL} = 50 mA V_{IN} = 2.0 V or 0.8 V V_{DD} = 5.5 V		1, 3	All		0.8	V
				2			1.0	
Three-state output leakage current	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS}		1, 2, 3	All	-10	10	µA
Short circuit output current 4/ 5/	I_{OS}	$V_{OUT} = V_{DD}$ or V_{SS}		1, 2, 3	All	-600	600	mA
Standby supply current V_{DD}	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5 V		1	All		10	µA
		$\overline{OE} = V_{DD}$		2, 3			160	µA
			M, D, P, L, R	1			160	µA
Quiescent supply current delta, TTL input level	ΔI_{DDQ}	For input under test $V_{IN} = V_{DD} - 2.1$ V For other inputs, $V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5 V		1, 2, 3	All		1.6	mA
			M, D, P, L, R	1			1.6	
Power dissipation 6/ 7/ 8/	P_D	C_L = 20 pF		1, 2, 3	All		1.0	mW/ MHz
Input capacitance	C_{IN}	f = 1 MHz at 0 V, See 4.4.1b		4	All		21	pF
Output capacitance	C_{OUT}	f = 1 MHz at 0 V, See 4.4.1b		4	All		21	pF
Functional tests		See 4.4.1c		7, 8	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, An, Bn to Bn, An	t_{PHL1}, t_{PLH1}	See figure 5.	9, 10, 11	All	4.0	11.5	ns
Propagation delay time, APAR, BPAR to BPAR APAR	t_{PHL2}, t_{PLH2}		9, 10, 11	All	4.0	11.5	ns
Propagation delay time, An, Bn to BPAR, APAR	t_{PHL3}, t_{PLH3}		9, 10, 11	All	5.0	12.0	ns
Propagation delay time, An, Bn to $\overline{ERRA}$, $\overline{ERRB}$	t_{PHL4}, t_{PLH4}		9, 10, 11	All	5.0	12.0	ns
Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	t_{PHL5}, t_{PLH5}		9, 10, 11	All	4.0	9.0	ns
Propagation delay time, ODD/$\overline{EVEN}$ to APAR, BPAR	t_{PHL6}, t_{PLH6}		9, 10, 11	All	4.0	9.0	ns
Propagation delay time, APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	t_{PHL7}, t_{PLH7}		9, 10, 11	All	4.0	9.0	ns
Propagation delay time, $\overline{SEL}$ to APAR, BPAR	t_{PHL8}, t_{PLH8}		9, 10, 11	All	3.5	8.5	ns
Propagation delay time, LEA, LEB to Bn, An	t_{PHL9}, t_{PLH9}		9, 10, 11	All	3.5	8.5	ns
Propagation delay time, LEA, LEB to BPAR, APAR	t_{PHL10}, t_{PLH10}	See figure 5.	9, 10, 11	All	4.0	9.0	ns
Propagation delay time, LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	t_{PHL11}, t_{PLH11}		9, 10, 11	All	5.0	12.0	ns
Propagation delay time, output enable, $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	t_{PZH1}, t_{PZL1}		9, 10, 11	All	3.5	9.5	ns
Propagation delay time, output enable, $\overline{GBA}$ or $\overline{GAB}$ to BPAR or APAR	t_{PZH2}, t_{PZL2}		9, 10, 11	All	3.5	9.5	ns
Propagation delay time, output disable, $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	t_{PHZ1}, t_{PLZ1}		9, 10, 11	All	2.0	6.0	ns
Propagation delay time, output disable, $\overline{GBA}$ or $\overline{GAB}$ to BPAR to APAR	t_{PHZ2}, t_{PLZ2}		9, 10, 11	All	2.0	6.0	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, high or low, An, Bn, APAR, BPAR to LEA, LEB	t_S	See figure 5.	9, 10, 11	All	1.0		ns
Hold time, high or low, An, Bn, APAR, BPAR to LEA, LEB	t_h	See figure 5.	9, 10, 11	All	1.5		ns
Pulse width for LEA, LEB 9/	t_w	See figure 5.	9, 10, 11	All	4.0		ns
Maximum clock frequency 9/	f_{MAX}	See figure 5.	9, 10, 11	All		80	MHz

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Functional tests are conducted in accordance with the MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$ (min) +20%, -0%; $V_{IL} = V_{IL}$ (max) +0%, -50%; as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).

3/ Transmission driving tests are performed at $V_{DD} = 5.5$ V, only one output loaded at a time with a duration not to exceed 2 ms. The test is guaranteed, if not tested, for $V_{IN} = V_{IH}$ minimum or V_{IL} maximum.

4/ Not more than one output may be shorted at a time for maximum duration of one second.

5/ Supplied as design limit, but not guaranteed or tested.

6/ Power dissipation specified per switching output.

7/ Guaranteed by characterization.

8/ Power does not include power contribution of any CMOS output sink current.

9/ Verified by functional test.

TABLE IB. SEP test limits . 1/ 2/ 3/

Device Type	$V_{DD} = 4.5$ V	Bias for SEL test $V_{DD} = 5.5$ V
	Effective LET No SEU	No SEL occurs at effective LET
All	LET ≤ 108 [MeV/(mg/cm2)]	LET ≤ 108 [MeV/(mg/cm2)]

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A. For SEP test conditions, see 4.4.4.5 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature for latchup test $T_A = +125°C \pm 10°C$ and $T_A = 25°C \pm 10°C$ for SEU test.

Case outline X

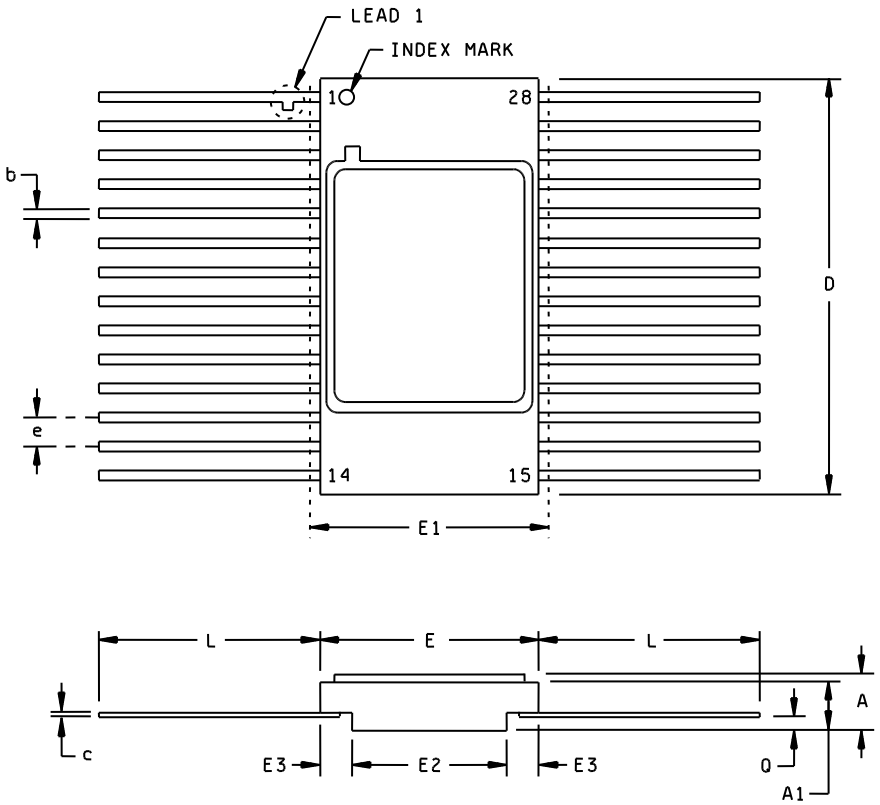


FIGURE 1. Case outline.

Case outline X

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		2.69		0.106
A1	2.01	2.46	0.079	0.097
b	0.38	0.51	0.015	0.020
c	0.13	0.20	0.005	0.008
D	17.93	18.29	0.706	0.720
e	1.27 BSC		0.050 BSC	
E	9.40	9.65	0.370	0.380
E1		10.41		0.410
E2	6.48	6.73	0.255	0.265
E3	0.76		0.030	
L	9.40	9.91	0.370	0.390
Q	0.76	0.97	0.030	0.038

FIGURE 1. Case outline – Continued.

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	ODD/$\overline{\text{EVEN}}$	15	$\overline{\text{ERRB}}$
2	$\overline{\text{ERRA}}$	16	$\overline{\text{SEL}}$
3	LEA	17	LEB
4	A0	18	BPAR
5	A1	19	B7
6	A2	20	B6
7	A3	21	B5
8	A4	22	B4
9	A5	23	B3
10	A6	24	B2
11	A7	25	B1
12	APAR	26	B0
13	$\overline{\text{GBA}}$	27	$\overline{\text{GAB}}$
14	V_{SS}	28	V_{DD}

Pin description

Inputs	Outputs
A0-A7	A bus data inputs/data outputs
B0-B7	B bus data inputs/data outputs
APAR, BPAR	A and B bus parity inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ parity select, active low for EVEN parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output enables for A or B bus, active low
$\overline{\text{SEL}}$	Select pin for feed-through or generate mode, low for generate mode
LEA, LEB	Latch enables for A and B latches, high for transparent mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error signals for checking generated parity with parity in, low if error occurs

FIGURE 2. Terminal connections.

Inputs					Operation
$\overline{GAB}$	$\overline{GBA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	Busses A and B are Tri-state (input A and B simultaneously)
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{E}$. Generated parity -- >APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{E}$. Generated parity -- > APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as ERRA.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{E}$. Generated parity --> APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	X	H	BPAR/B[0:7] -- > APAR/A[0:7] feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	H	H	BPAR/B[0:7] -- > APAR/A[0:7] feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$. APAR/A[0:7] fed back through the A latch for generate/check as $\overline{ERRA}$
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{E}$. Generated parity -- >BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	L	H	H	Generates parity for A[0:7] based on O/$\overline{E}$. Generated parity -- >BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as ERRB
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{E}$. Generated parity --> BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	L	APAR/A[0:7] -- > BPAR/B[0:7] feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	H	APAR/A[0:7] -- > BPAR/B[0:7] feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$. BPAR/B[0:7] fed back through the B latch for generate/check as $\overline{ERRB}$
L	L	X	X	X	Output to A bus and B bus (Not allowed).

O/$\overline{E}$ = ODD/$\overline{EVEN}$
H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 3. Function table.

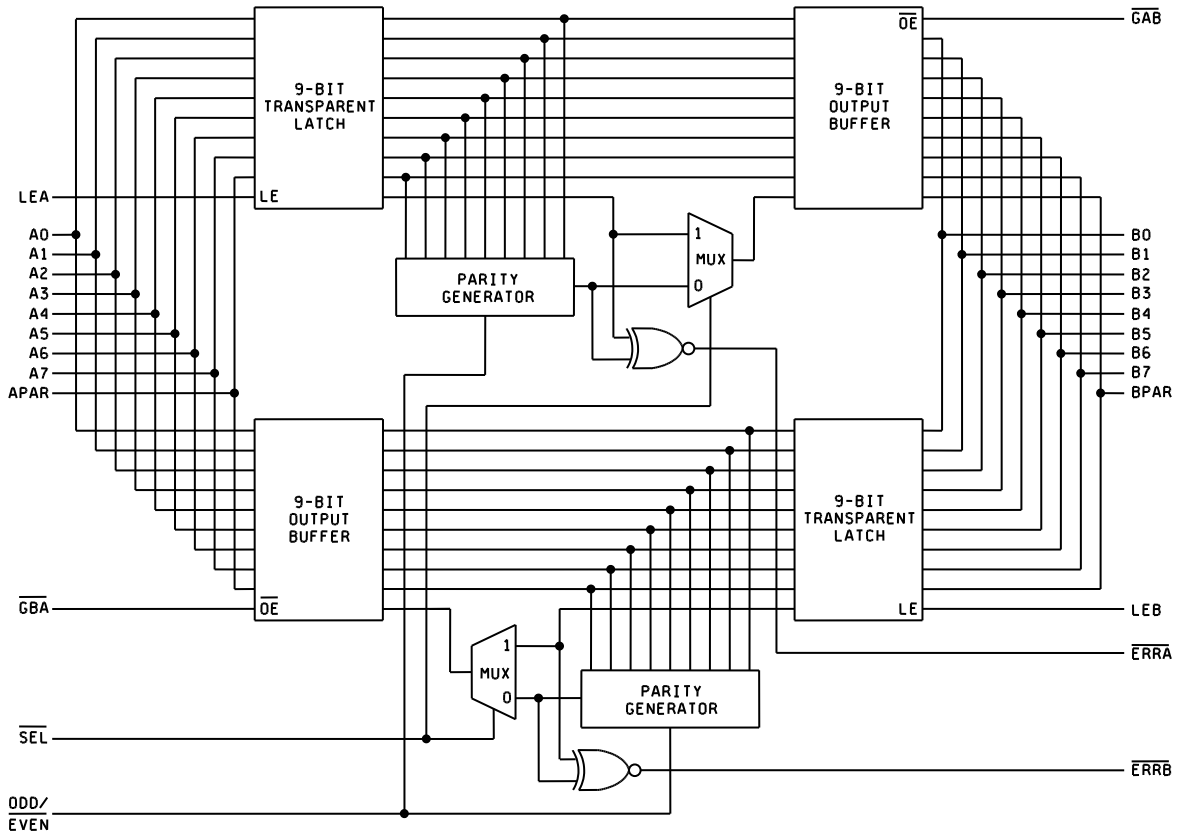
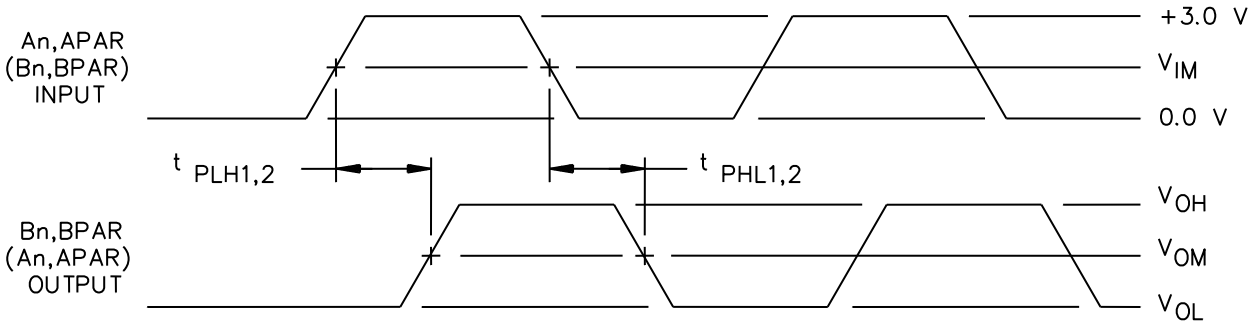
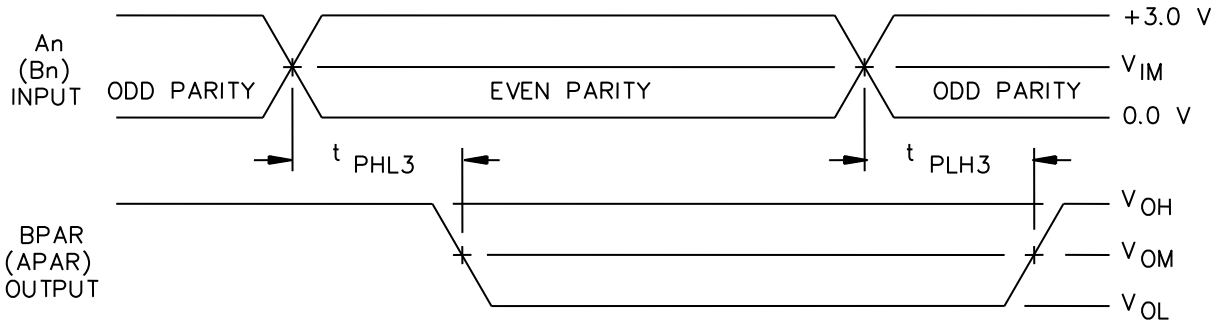


FIGURE 4. Logic diagram.



An to Bn,Bn to An,APAR to BPAR,BPAR to APAR

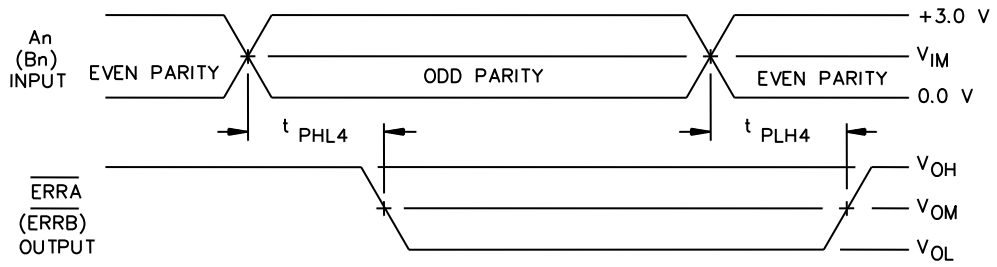
NOTES:
1. V_{IM} = 1.5 V, V_{OM} = $V_{DD}/2$
2. $\overline{SEL}$ = 3.0 V



An to BPAR,or Bn to BPAR (WITH EVEN PARITY MODE SHOWN)

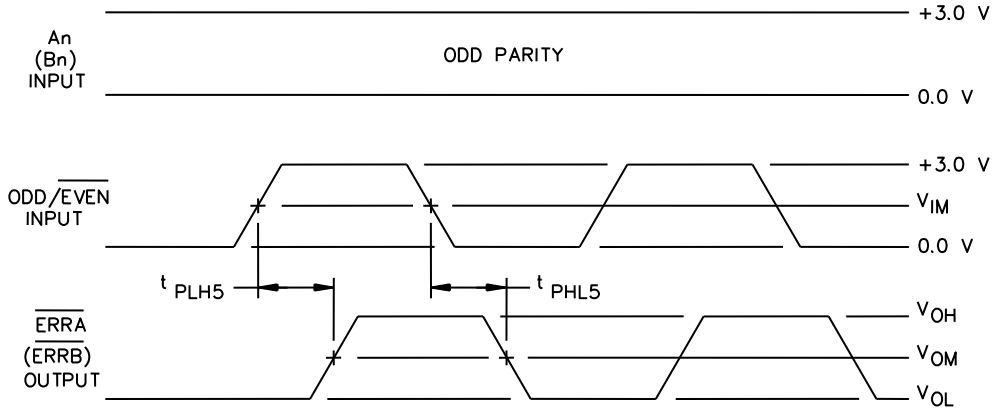
NOTES:
1. V_{IM} = 1.5 V, V_{OM} = $V_{DD}/2$
2. $\overline{SEL}$ = ODD/$\overline{EVEN}$ = V_{SS}
3. LEA (LEB) = 3.0 V

FIGURE 5. Switching waveforms and test circuit.



An to $\overline{\text{ERRA}}$ or Bn to $\overline{\text{ERRB}}$ (WITH EVEN PARITY MODE SHOWN)

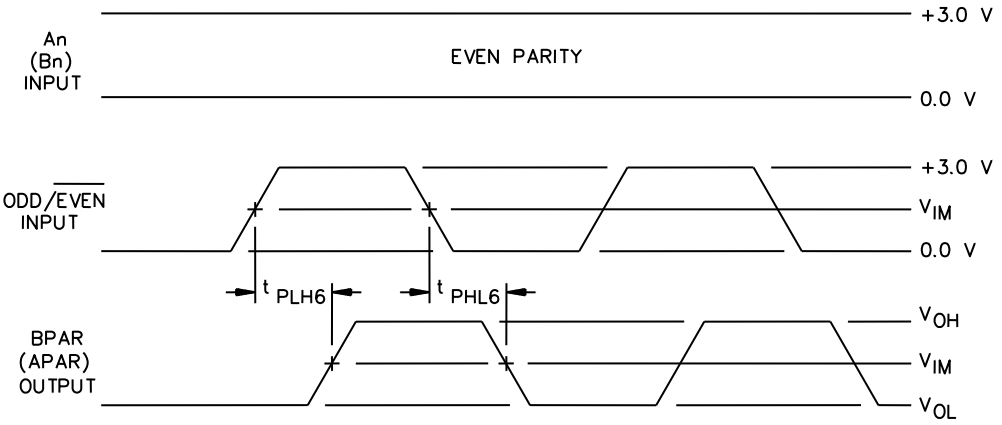
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. APAR (BPAR) = ODD/$\overline{\text{EVEN}}$ = V_{SS}
3. LEA (LEB) = 3.0 V



ODD/$\overline{\text{EVEN}}$ to $\overline{\text{ERRA}}$ or ODD/ $\overline{\text{EVEN}}$ to $\overline{\text{ERRB}}$

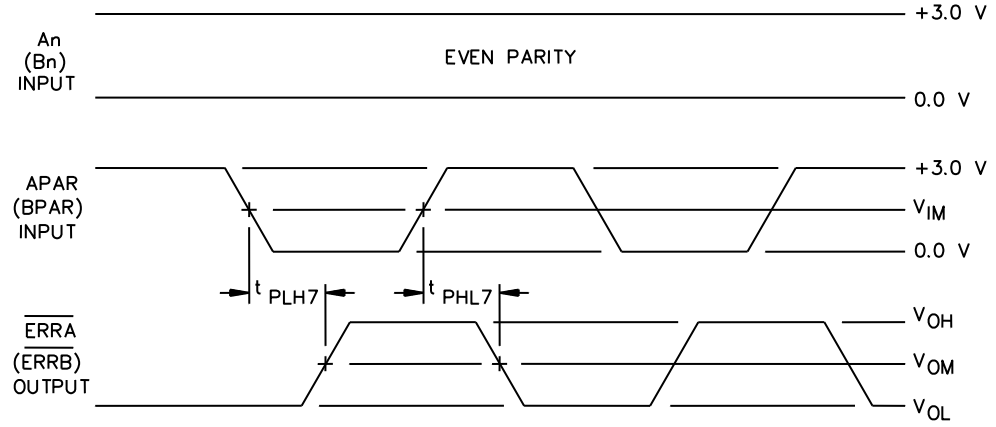
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. APAR (BPAR) = V_{SS}

FIGURE 5. Switching waveforms and test circuit – Continued.



ODD/$\overline{\text{EVEN}}$ to APAR or ODD/ $\overline{\text{EVEN}}$ to BPAR (WITH EVEN PARITY MODE SHOWN)

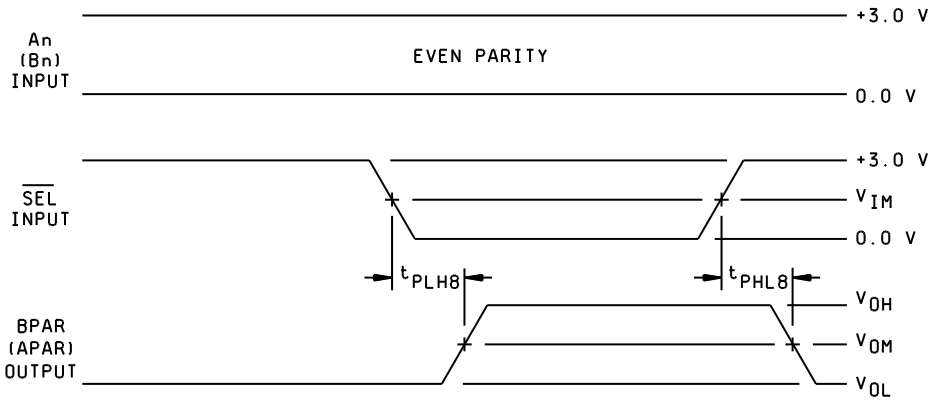
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. $\overline{SEL}$ = APAR (BPAR) = V_{SS}



APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$
(WITH EVEN PARITY MODE SHOWN WITH EVEN DATA PARITY.
ODD PARITY MODE WOULD CAUSE INVERTED OUTPUT.)

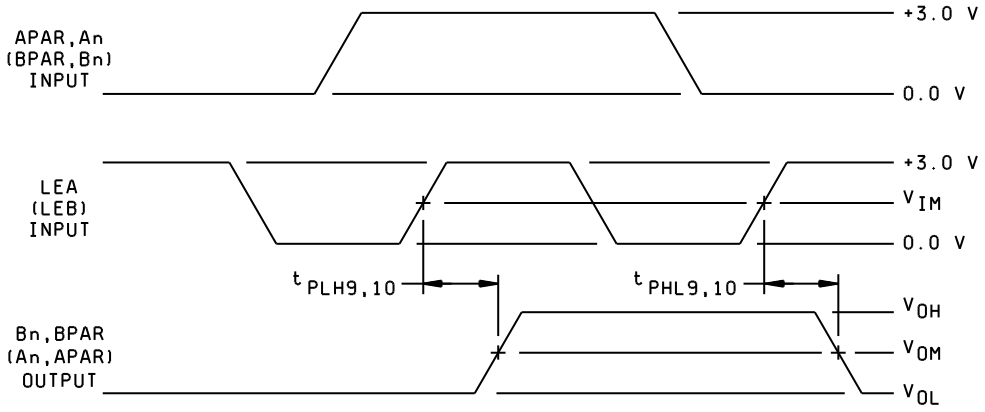
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. ODD/$\overline{\text{EVEN}}$ = V_{SS}

FIGURE 5. Switching waveforms and test circuit – Continued.



SEL to BPAR or SEL to APAR
(WITH ODD PARITY MODE SHOWN WITH EVEN DATA PARITY.
EVEN PARITY MODE WOULD CAUSE INVERTED OUTPUT.)

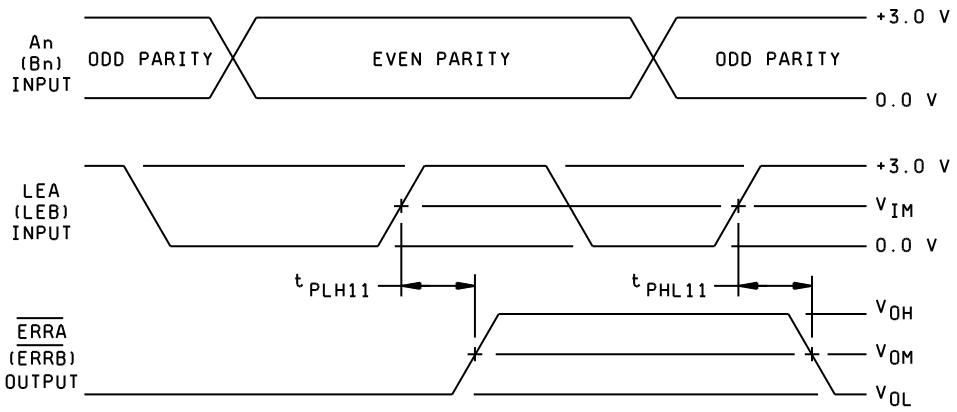
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. ODD/EVEN = 3.0 V
3. APAR (BPAR) = V_{SS}



LEA to BPAR or LEB to APAR,LEA to Bn or LEB to An

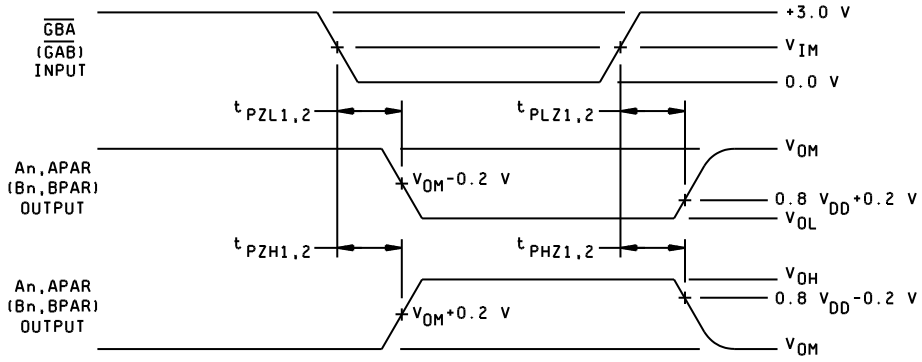
NOTES:
1 V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2 SEL = 3.0 V

FIGURE 5. Switching waveforms and test circuit – Continued.



LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$ (WITH ODD PARITY MODE SHOWN)

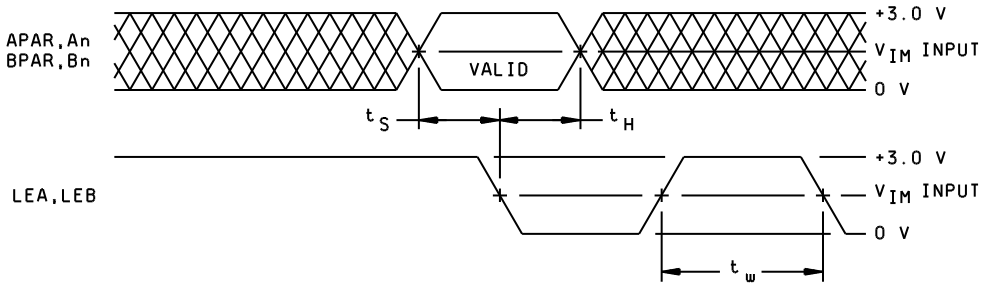
NOTES:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$
2. APAR (BPAR) = ODD/$\overline{\text{EVEN}}$ = 3.0 V



3-STATE OUTPUT ENABLE TIME AND OUTPUT DISABLE TIME

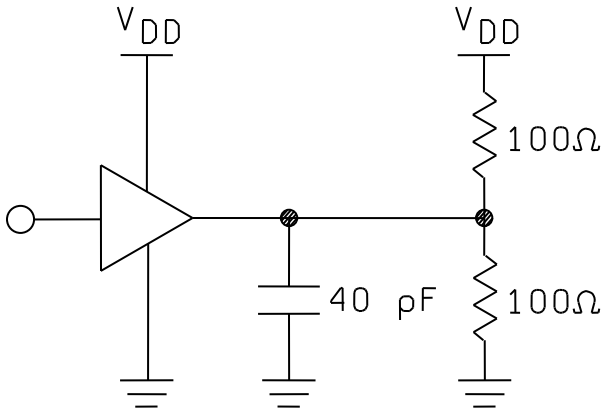
NOTE:
1. V_{IM} = 1.5 V, $V_{OM} = V_{DD}/2$

FIGURE 5. Switching waveforms and test circuit – Continued.



DATA SETUP AND HOLD TIMES,PULSE WIDTH HIGH

NOTE:
1. V_{IM} = 1.5 V, V_{OM} = V_{DD}/2



TEST CIRCUIT A or EQUIVALENT

NOTES:

1. C_L includes test jig and probe capacitance.
2. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	- - - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in Table IIB herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Condition	Limits 2/ 3/
Standby supply current	I_{DDQ}	T_A = 25°C	10 µA 4/
Quiescent supply current delta	ΔI_{DDQ}		± 10% of measured value or 100 µA whichever is greater

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.
3/ When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.
4/ I_{DDQ} limits were tightened from 100µA to 10µA for pre/post burn-in to determine the delta at 25°C. These tighter limits were implemented to more effectively screen out marginal parts upstream from group A and allow elimination of Deltas.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 (condition A) and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-09-22

Approved sources of supply for SMD 5962-06240 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0624001QXA	65342	UT54ACTS899-UCA
5962R0624001QXC	65342	UT54ACTS899-UCC
5962R0624001VXA	65342	UT54ACTS899-UCA
5962R0624001VXC	65342	UT54ACTS899-UCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, Colorado 80907-3486