REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical change for I_{DDQ} test in table IA. – LTG	07-04-17	Thomas M. Hess
B	Add die requirements with appendix A. Update boilerplate paragraphs as specified in the current MIL-PRF-38535 requirements. – MAA	09-02-11	Charles F. Saffle
C	Add subgroups to table IIA in groups C and D. - LTG	11-06-23	David J. Corbett
D	Add equivalent test circuits and footnote 2 to figure 5. Delete class M requirements per updated boilerplate paragraphs. - MAA	12-11-08	Thomas M. Hess
E	Update devices supplier CAGE 65342 information to bulletin page. Update boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - TTM	21-08-27	Muhammad A. Akbar

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E	E	E							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Larry T. Gauder

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
06-12-21

REVISION LEVEL
E

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

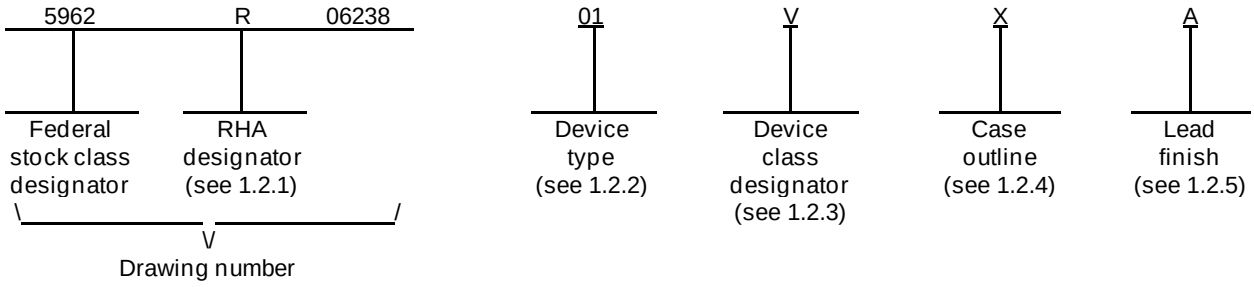
SIZE	CAGE CODE	
A	**67268**	**5962-06238**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS299E	8-bit universal shift/storage register with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.3 V dc to +6.0 V dc
Voltage on any pin during operation ($V_{I/O}$)	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current (I_{IN})	±10 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J)	+175°C
Thermal resistance junction-to-case (θ_{JC})	20°C/W
Maximum power dissipation (P_D)	200 mW

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+3.0 V dc to +5.5 V dc
Input voltage range on any pin (V_{IN})	0.0 V dc to V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time (t_r, t_f)	20 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 to 300 rad(Si)/s)	100 krad(Si) 4/
Single event phenomenon (SEP) :	
No single event latchup (SEL) occurs at effective LET (see 4.4.4.5)	≤ 108 MeV-mg/cm^2 5/
No onset single event upset (SEU) occur at effective LET at 4.5 V	≤ 95 MeV-mg/cm^2 5/
No onset single event upset (SEU) occur at effective LET at 3.0 V	≤ 48 MeV-mg/cm^2 5/
Neutron fluence	1X10^{14} n/cm^2 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to V_{SS}.

3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.

4/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 condition A. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).

5/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS devices.

JESD78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org/.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Function table. The function table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage 2/	V_{IH}	V_{DD} = 3.0 V to 5.5 V	1, 2, 3	All	$0.7V_{DD}$		V
Low level input voltage 2/	V_{IL}	V_{DD} = 3.0 V to 5.5 V	1, 2, 3	All		$0.3V_{DD}$	V
Positive input clamp voltage	$V_{IC}+$	For input under test I_{IN} = +18 mA, V_{DD} = 0.0 V	1, 2, 3	All	0.4	1.5	V
Negative input clamp voltage	$V_{IC}-$	For input under test I_{IN} = -18 mA, V_{DD} = open	1, 2, 3	All	-1.5	-0.4	V
High level output voltage	V_{OH1}	I_{OH} = -12 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 3.0 V to 3.6 V	1, 2, 3	All	V_{DD} – 0.6 V		V
		I_{OH} = -100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 3.0 V to 3.6 V			V_{DD} – 0.2 V		
	V_{OH2}	I_{OH} = -24 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	1, 3	All	V_{DD} – 0.64 V		V
		I_{OH} = -24 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	2		V_{DD} – 0.8 V		
		I_{OH} = -100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	1, 2, 3		V_{DD} – 0.2 V		
	V_{OH3} 3/	I_{OH} = -50 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 5.5 V	1, 3	All	V_{DD} – 1.1 V		V
			2		V_{DD} – 1.25 V		
Low level output voltage	V_{OL1}	I_{OL} = +12 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 3.0 V to 3.6 V	1, 2, 3	All		0.4	V
		I_{OL} = +100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 3.0 V to 3.6 V				0.2	
	V_{OL2}	I_{OL} = +24 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	1, 3	All		0.36	V
		I_{OL} = +24 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	2			0.5	
		I_{OL} = +100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V	1, 2, 3			0.2	
	V_{OL3} 3/	I_{OL} = +50 mA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 5.5 V	1, 3	All		0.8	V
			2			1.0	
Three-state output leakage current	I_{OZ}	V_{DD} = 3.0 V to 5.5 V $V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-10	10	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{IN}	V_{DD} = 3.0 V to 5.5 V $V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-1	1	µA
Short circuit output current 4/ 5/	I_{OS}	V_{DD} = 3.0 V to 5.5 V $V_{OUT} = V_{DD}$ or V_{SS}	1, 2, 3	All	-600	600	mA
Power dissipation 6/ 7/ 8/	P_{TOTAL}	C_L = 20 pF V_{DD} = 3.0 V to 5.5 V	1, 2, 3	All		0.5	mW/ MHz
Standby supply current, V_{DD}	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS} V_{DD} = 5.5 V $\overline{OE}n = V_{DD}$	1	All		10	µA
			2, 3			80	
		M, D, P, L, R	1			80	
Input capacitance	C_{IN}	f = 1 MHz at 0 V V_{DD} = 3.0 V to 5.5 V See 4.4.1c	4	All		17	pF
Output capacitance	C_{OUT}	f = 1 MHz at 0 V V_{DD} = 3.0 V to 5.5 V See 4.4.1c	4	All		17	pF
Functional tests		See 4.41d	7, 8	All			
Propagation delay time, CP to Q_0 or Q_7 (shift left or right)	t_{PLH1}, t_{PHL1}	V_{DD} = 3.3 V ±0.3 V See figure 4	9, 10, 11	All	4.5	10.5	ns
Propagation delay time, CP to IOn	t_{PLH2}, t_{PHL2}		9, 10, 11	All	5.0	14.0	ns
Propagation delay time, $\overline{MR}$ to Q_0 or Q_7	t_{PHL3}		9, 10, 11	All	6.0	11.0	ns
Propagation delay time, $\overline{MR}$ to IOn	t_{PHL4}		9, 10, 11	All	7.0	15.5	ns
Propagation delay time, output enable, $\overline{OE}$ to IOn	t_{PZL}, t_{PZH}		9, 10, 11	All	4.0	10.5	ns
Propagation delay time, output disable, $\overline{OE}$ to IOn	t_{PLZ}, t_{PHZ}		9, 10, 11	All	3.0	6.5	ns
Pulse width, CP 9/	t_{W1}	V_{DD} = 3.3 V ±0.3 V See figure 4.	9, 10, 11	All	5.5		ns
Pulse width, $\overline{MR}$ 9/	t_{W2}		9, 10, 11	All	5.5		ns
Setup time, high or low, Sn to CP	t_{S1}	V_{DD} = 3.3 V ±0.3 V See figure 4.	9, 10, 11	All	3.0		ns
Hold time, high or low, Sn to CP	t_{h1}		9, 10, 11	All	0.5		ns

See footnotes at end of table

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, high or low, DSn to CP	t_{s2}	V_{DD} = 3.3 V ±0.3 V See figure 4.	9, 10, 11	All	1.0		ns
Hold time, high or low, DSn to CP	t_{h2}		9, 10, 11	All	0.5		ns
Setup time, high or low, IOn to CP	t_{s3}		9, 10, 11	All	1.5		ns
Hold time, high or low, IOn to CP	t_{h3}		9, 10, 11	All	0.5		ns
Recovery time, $\overline{MR}$ to CP	t_{REC}		9, 10, 11	All	1.0		ns
Maximum frequency, CP 9/	f_{MAX}		9, 10, 11	All		70	MHz
Propagation delay time, CP to Q_0 or Q_7 (shift left or right)	t_{PLH1}, t_{PHL1}	V_{DD} = 5.0 V ±10% See figure 4.	9, 10, 11	All	4.0	8.0	ns
Propagation delay time, CP to IOn	t_{PLH2}, t_{PHL2}		9, 10, 11	All	4.5	9.0	ns
Propagation delay time, $\overline{MR}$ to Q_0 or Q_7	t_{PHL3}		9, 10, 11	All	5.0	9.0	ns
Propagation delay time, $\overline{MR}$ to IOn	t_{PHL4}		9, 10, 11	All	5.5	11.0	ns
Propagation delay time, output enable, to $\overline{OE}$ IOn	t_{PZL}, t_{PZH}		9, 10, 11	All	3.0	7.0	ns
Propagation delay time, output disable, $\overline{OE}$ to IOn	t_{PLZ}, t_{PHZ}		9, 10, 11	All	3.0	6.0	ns
Pulse width, CP 9/	t_{w1}	V_{DD} = 5.0 V ±10% See figure 4.	9, 10, 11	All	5.0		ns
Pulse width, $\overline{MR}$ 9/	t_{w2}		9, 10, 11	All	5.0		ns
Setup time, high or low, Sn to CP	t_{s1}		9, 10, 11	All	2.0		ns
Hold time, high or low, Sn to CP	t_{h1}		9, 10, 11	All	0.5		ns
Setup time, high or low, DSn to CP	t_{s2}		9, 10, 11	All	1.0		ns
Hold time, high or low, DSn to CP	t_{h2}		9, 10, 11	All	0.5		ns

See footnotes at end of table

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, high or low, IOn to CP	t_{s3}	V_{DD} = 5.0 V ±10% See figure 4.	9, 10, 11	All	1.0		ns
Hold time, high or low, IOn to CP	t_{h3}		9, 10, 11	All	0.5		ns
Recovery time, $\overline{MR}$ to CP	t_{REC}		9, 10, 11	All	0.5		ns
Maximum frequency, CP 9/	f_{MAX}		9, 10, 11	All		90	MHz

1/ Devices supplied to this drawing are characterized at all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Functional tests are conducted in accordance with the MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$ (min) +20%, -0%; $V_{IL} = V_{IL}$ (max) +0%, -50%; as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).

3/ Transmission driving test are performed at V_{DD} = 5.5 V, only one output loaded at a time with a duration not to exceed 2 ms. The test is guaranteed, if not tested, for $V_{IN} = V_{IH}$ minimum or V_{IL} maximum.

4/ Not more than one output may be shorted at a time for a maximum duration of one second.

5/ Supplied as a design limit, but not guaranteed or tested.

6/ Guaranteed by characterization.

7/ Power does not include power contribution of any CMOS output sink current.

8/ Power dissipation specified per switching output.

9/ Verified at speed by functional testing.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C	Bias V_{DD} = 3.0 V and 4.5 V For single event upsets (SEU)		Bias V_{DD} = 5.5 V for SEL test
		No SEU occurs at effective LET [MeV-mg/cm^2/)]	Maximum device cross section (Cm^2)	No SEL occurs at effective LET [MeV-mg/cm^2/)
All	3/	LET ≤ 95 at 4.5 V LET ≤ 48 at 3.0 V	8.1E-10 at 4.5 V 9.4E-9 at 3.0 V	LET ≤ 108

1/ For SEP test conditions, see 4.4.4.5 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature for latchup test T_A = +125°C ±10°C. Test temperature for SEU test T_A = +25°C ±10°C.

Case outline X

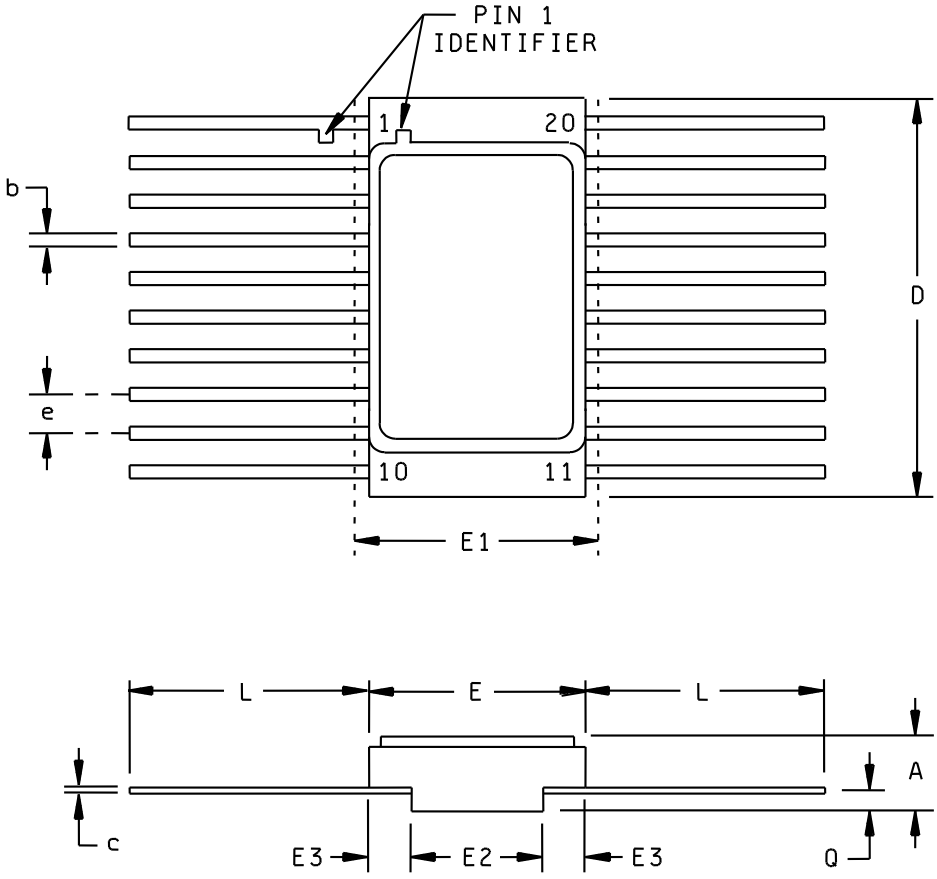


FIGURE 1. Case outline.

Case outline X

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.102	.122	2.5908	3.0988
b	.015	.020	0.381	0.508
c	.005	.008	0.127	0.2032
D	.509	.521	12.9286	13.2334
E	.290	.300	7.366	7.62
E1	---	.330	---	8.382
E2	.207	.217	5.2578	5.5118
E3	.030	---	0.762	---
e	.050 BSC		1.27 BSC	
L	.380	.400	9.652	10.16
Q	.026	.045	0.6604	1.143

FIGURE 1. Case outline – Continued.

Device type	All
Case outline	X
Terminal number	Terminal symbol
1	S0
2	$\overline{OE}1$
3	$\overline{OE}2$
4	IO6
5	IO4
6	IO2
7	IO0
8	Q0
9	$\overline{MR}$
10	V_{SS}
11	DS0
12	CP
13	IO1
14	IO3
15	IO5
16	IO7
17	Q7
18	DS7
19	S1
20	V_{DD}

Pin names	Pin description
CP	Clock pulse input
DS0	Serial data input for right shift
DS7	Serial data input for left shift
S0, S1	Mode select inputs
$\overline{MR}$	Asynchronous master reset
$\overline{OE}1$, $\overline{OE}2$	Three-state output enable inputs
IO0-IO7	Parallel data inputs or three-state parallel outputs
Q0, Q7	Serial outputs

FIGURE 2. Terminal connections.

Inputs						Operation
$\overline{MR}$	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	
L	X	L	X	L	L	Q0 = Q7 = Low, asynchronous reset
L	L	X	X	L	L	Q0 = Q7 = Low, asynchronous reset
L	H	H	X	X	X	Q0 = Q7 = Low, I/O = High impedance, asynchronous reset
H	H	H	↑	X	X	Parallel load; IOn > Qn
H	L	H	↑	L	L	Shift right; DS0 > Q0, Q0 > Q1, etc.
H	H	L	↑	L	L	Shift left; DS7 > Q7,Q7 > Q6, etc.
H	L	L	X	L	L	Hold

H = High voltage level
L = Low voltage level
↑ = Low-to-high clock transition
X = Irrelevant

FIGURE 3. Function table.

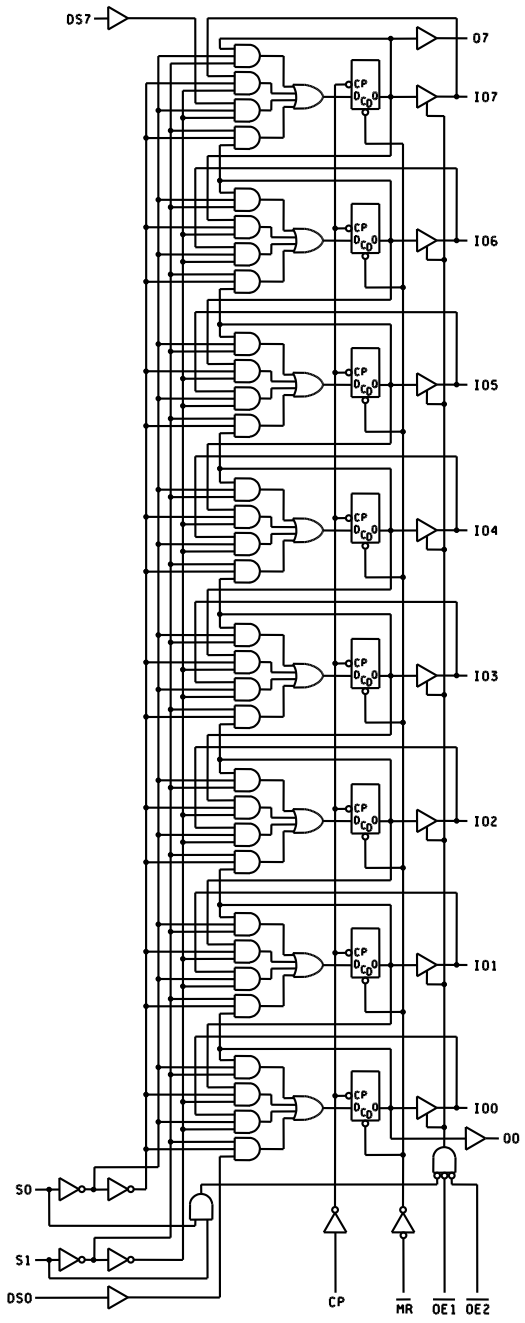


FIGURE 4. Logic diagram.

3.3 V operation

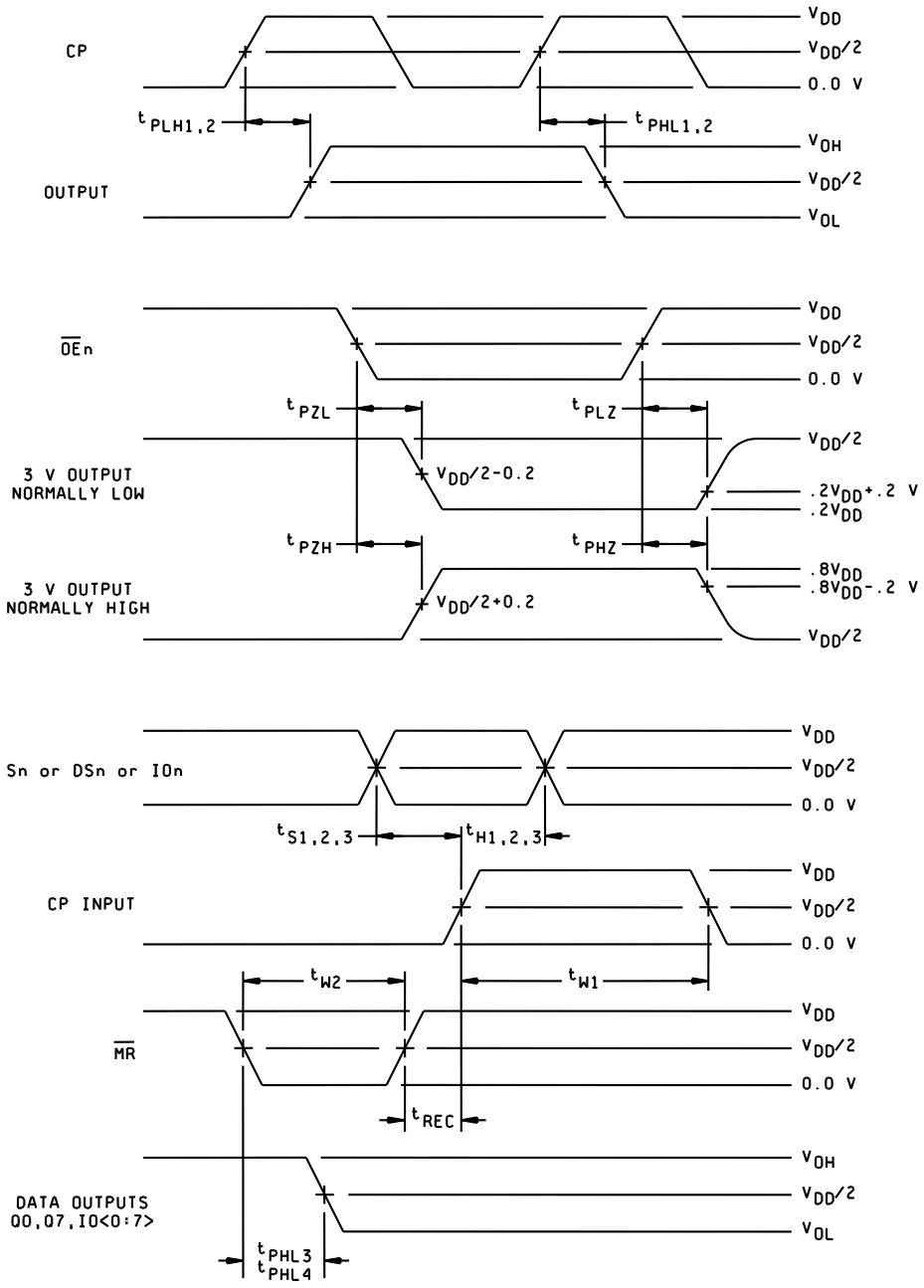


FIGURE 5. Switching waveforms and test circuit.

5.0 V operation

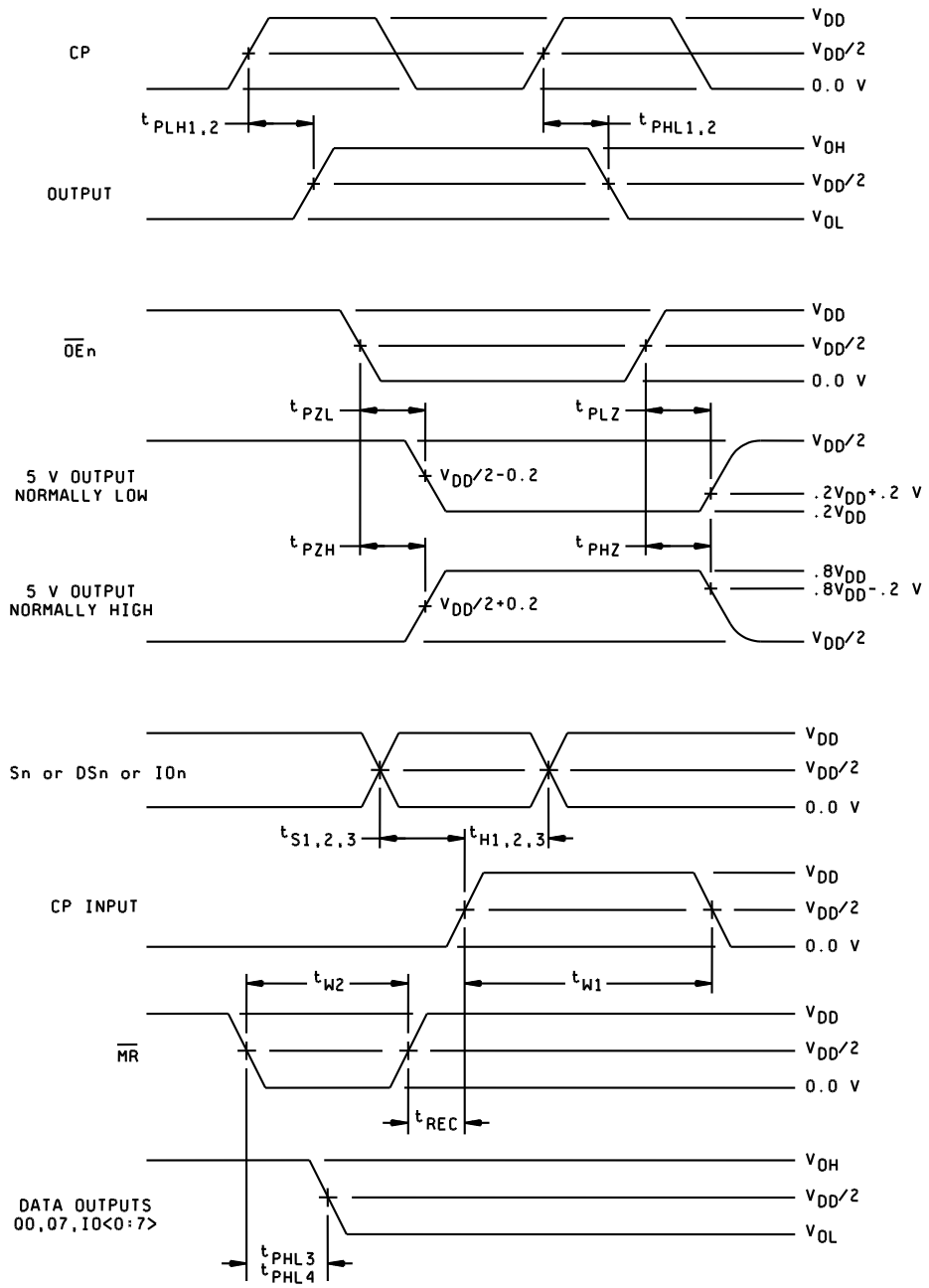
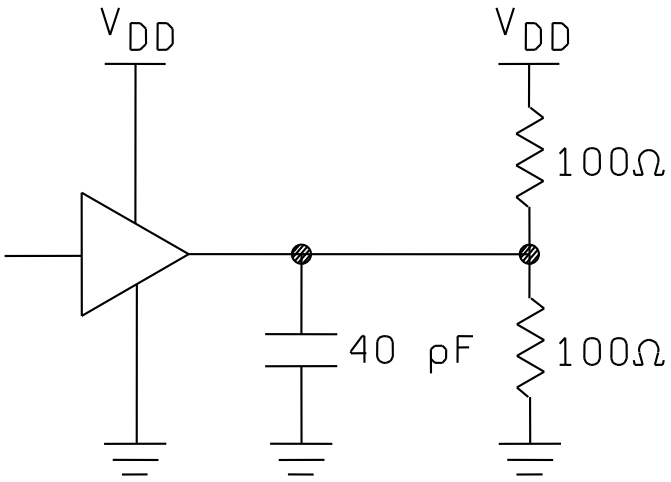


FIGURE 5. Switching waveforms and test circuit - Continued.



TEST CIRCUIT A or EQUIVALENT

NOTES:

1. C_L includes test jig and probe capacitance.
2. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	- - - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in table IIB herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter 1/	Symbol	Condition	Delta limit 2/ 3/
Standby supply current	I_{DDQ}	T_A = 25°C	10 µA 4/

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.
3/ When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.
4/ IDDQ limits were tightened from 100µA to 10µA for pre/post burn-in to determine the delta at 25°C. These tighter limits were implemented to more effectively screen out marginal parts upstream from group A and allow elimination of Deltas.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 (condition A) and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ±5°C after an exposure of 2×10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

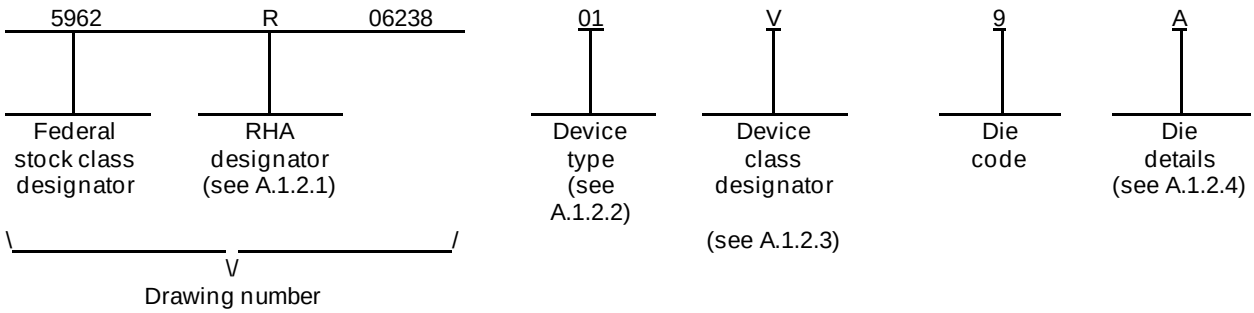
c. Number of transients (SET).

d. Occurrence of latch up (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS299E	8-bit universal shift/storage register with three-state outputs

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883 method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 method 2010 or the alternate procedures allowed in MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

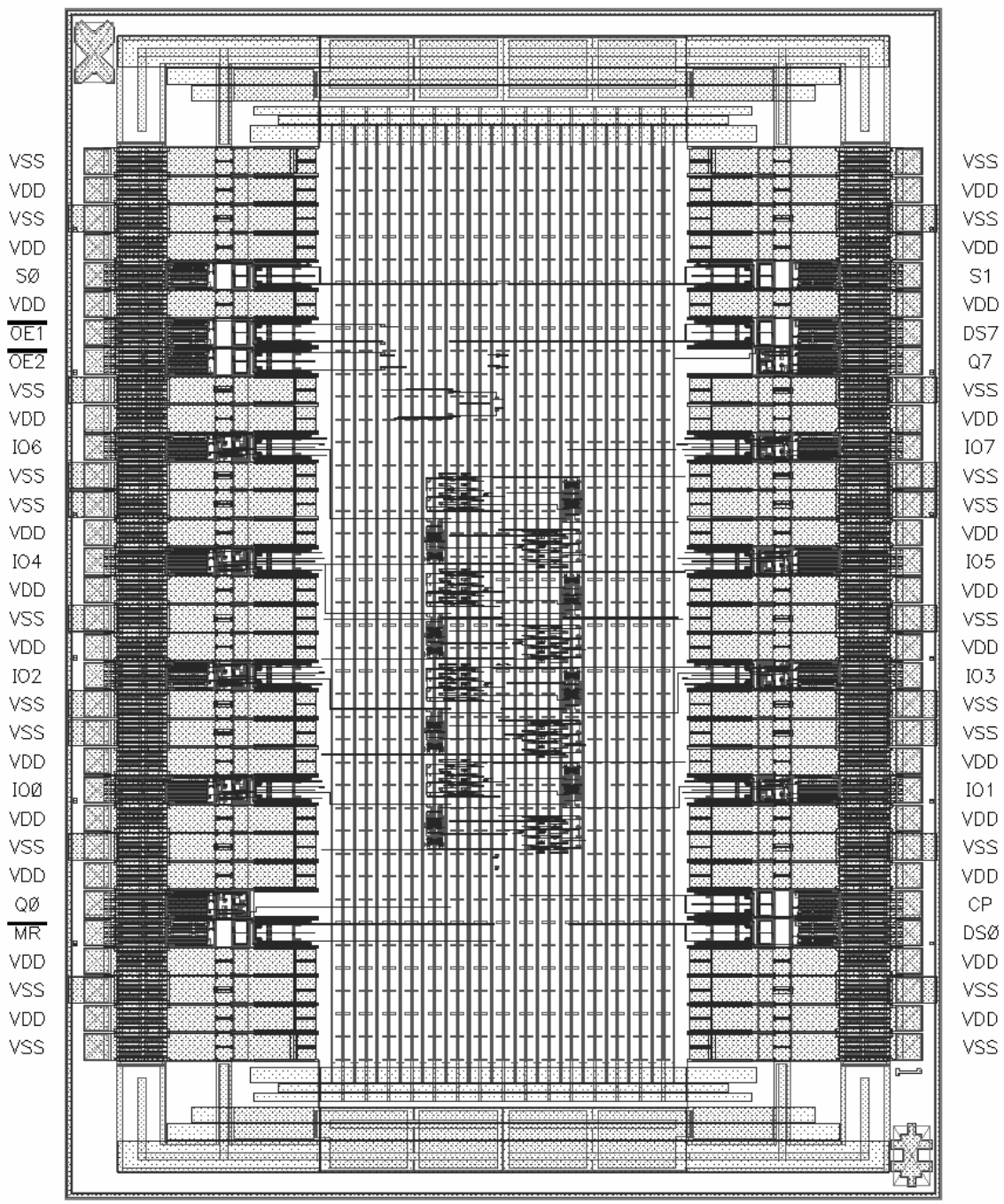
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Note: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	112 x 152 mils
Die thickness:	17 ± 1 mil

Interface materials.

Top metallization:	Si Al Cu 9.0 kÅ – 12.5 kÅ
Backside metallization:	None

Glassivation:

Type:	Nitride
Thickness:	9.0 kÅ – 11.0 kÅ

Substrate: Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to Vss
Special assembly instructions:	Bond a Vss pad first.

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-08-27

Approved sources of supply for SMD 5962-06238 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0623801QXA	65342	UT54ACS299EUCA
5962R0623801QXC	65342	UT54ACS299EUCC
5962R0623801VXA	65342	UT54ACS299EUCA
5962R0623801VXC	65342	UT54ACS299EUCC
5962R0623801Q9A	65342	UT54ACS299E-Q-DIE
5962R0623801V9A	65342	UT54ACS299E-V-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486