

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct the IOH and IOL currents for VOH and VOL respectively in table I. Correct the maximum limits for the Transmitter/Receiver Characteristics in table I on sheet 7. - CFS	06-09-25	Thomas M. Hess
B	Increased input voltage range to "All other terminals" in paragraph 1.3. – LTG	07-03-14	Thomas M. Hess
C	Update thermal note on sheet 10 for case outline. - LTG	08-01-24	Thomas M. Hess
D	Change definitions for: ENABLE, LCKREFN, RKMSB in table III. - PHN	12-02-23	Thomas M. Hess
E	Update footnote 2/ for pin TKLSB and TKMSB to table III. Delete class M requirements throughout - MAA	13-04-16	Thomas M. Hess
F	Add devices performance footnote 3/ to section 1.3. – MAA	14-02-24	Thomas M. Hess
G	Update input voltage rating to section 1.3. Add figure 5f and 5g for power-on/reset timing diagram. Update terminal pin ENABLE and LCKREFN features description to table III. Add notes for power-on/ reset application to table III for terminal features. - MAA	14-08-25	Thomas M. Hess

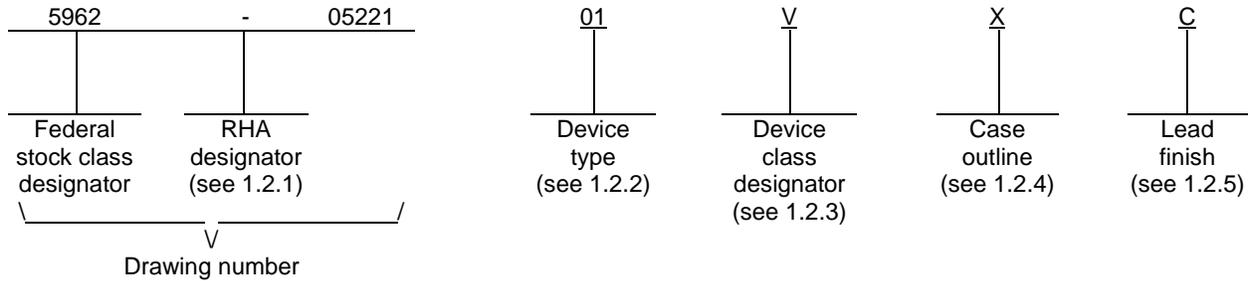
REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Charles F. Saffle	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles F. Saffle																		
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, DIGITAL, 1.6 TO 2.5 GBPS BIDIRECTIONAL TRANSCEIVER, MONOLITHIC SILICON																	
	DRAWING APPROVAL DATE 06-06-20																		
	REVISION LEVEL G	SIZE A	CAGE CODE 67268	5962-05221															
SHEET 1 OF 22																			

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	TLK2711	1.6 to 2.5 GBPS transceiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1.	68	Ceramic quad flat pack with non-conductive tie-bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +3 V dc 2/
Input voltage range:	
TXD0 to TXD15, ENABLE, TXCLK, TKMSB, TKLSB, LOOPEN, PRBSEN, LCKREFN, PRE, TESTEN	-0.3 V dc to +4 V dc
RXD0 TO RXD15, RKMSB, RKLSB, RXCLK.....	-0.30 V dc to $V_{DD} + 0.35$ V dc
DINRXP, DINRXN, DOUTTXP, DOUTTXN	-0.35 V dc to $V_{DDA} + 0.35$ V dc
Power dissipation (P_D)	550 mW
Storage temperature range (T_{stg})	-65°C to +150°C
Electrostatic discharge:	
Human Body Model (HBM)	2 kV
Operating case temperature range (T_c).....	-55°C to +125°C
Maximum cumulative exposure of unpowered receiver to external inputs	10 hours 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{DD})	
1.6Gbps to 2.0Gbps operation	2.375 V dc to 2.7 V dc
2.0Gbps to 2.5Gbps operation	2.5 V dc to 2.7 V dc
Supply current (I_{CC}):	
Frequency = 1.6 Gbps, PRBS pattern.....	110 mA (nominal)
Frequency = 2.5 Gbps, PRBS pattern.....	160 mA (nominal)
Power dissipation (P_D):	
Frequency = 1.6 Gbps, PRBS pattern.....	275 mW (nominal)
Frequency = 2.5 Gbps, PRBS pattern.....	400 mW (nominal)
Frequency = 2.5Gbps, PRBS pattern.....	550 mW (maximum)
Shutdown current (ENABLE = 0 V dc, V_{DD} and V_{DDA} = 2.7 V dc)	3 mA (nominal)
PLL startup lock time (V_{DD} and V_{DDA} = 2.375 V dc).....	0.4 ms (maximum)
Data acquisition time	1024 Bits (nominal)
Operating case temperature range (T_c).....	-55°C to +125°C

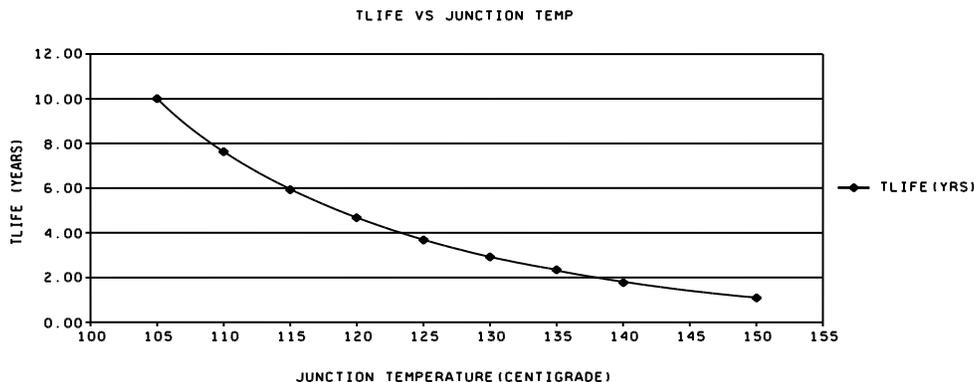


FIGURE 1. Impact of elevated temperature on device life.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Extended operation at the maximum levels may degrade performance and affect device reliability.
- 2/ All voltage values, except differential I/O bus voltages, are stated with respect to network ground.
- 3/ Characterization was performed using maximum supply voltage V_{DD} and minimum frequency and typical V_{CM} from recommended operating conditions for the specified period of times. This device (TLK2711-SP) shows no performance degradation when an external powered transmitter sends a signal to an unpowered receiver for short period of time (up to 10 hours of life time of the device).
- 4/ Extended use at maximum recommended operating temperature may result in reduction of overall device life. See figure 1 above for impact of elevated temperature on device life.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Block diagram. The block diagram shall be as specified on figure 4.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 5a – 5e.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

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3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	

Reference Clock (TXCLK) timing Requirements

Frequency		Receiver Data Rate/20		All	-100	+100	ppm
Frequency tolerance					-100	100	ppm
Duty cycle					40%	60%	
Jitter time		Peak-to-peak.				40	ps

TTL Input Electrical Characteristics ^{2/}

High-level input voltage	V _{IH}	See figure 5a.	1, 2, 3	All	1.7		V	
Low-level input voltage	V _{IL}	See figure 5a.				0.8	V	
High-level input current	I _{IH}	V _{DD} = 2.7 V, V _{IN} = 2 V				40	μA	
Low-level input current	I _{IL}	V _{DD} = 2.7 V, V _{IN} = 0.4 V				-40	μA	
Receiver input capacitance	C _i	See 4.4.1c	4			6 TYP		pF
Functional tests		See 4.4.1b	7, 8					
Rise time, TXCLK, TKMSB, TKLSB, TXD[0..15]	t _r	See figure 5a. 0.7 V to 1.9 V, C _L = 5 pF	9, 10, 11			1 TYP		ns
Fall time, TXCLK, TKMSB, TKLSB, TXD[0..15]	t _f	See figure 5a. 1.9 V to 0.7 V, C _L = 5 pF				1 TYP		ns
Setup time, TXD[0..15], TKMSB, TKLSB setup to ↑ TXCLK	t _{su}	See figure 5a. ^{3/}			1.5		ns	
Hold time, TXD[0..15], TKMSB, TKLSB hold to ↑ TXCLK		See figure 5a. ^{3/}			0.4		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TTL Output Switching Characteristics							
High-level output voltage	V _{OH}	I _{OH} = -2 mA, V _{DD} = 2.3 V	1, 2, 3	All	2.1		V
Low-level output voltage	V _{OL}	I _{OL} = 2 mA, V _{DD} = 2.3 V					0.5
Slew rate (rising), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15]	t _{r(slew)}	See figure 5b. 0.8 V to 2 V, C _L = 5 pF	9, 10, 11		0.5		V/ns
Slew rate (falling), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15]	t _{f(slew)}	See figure 5b. 2 V to 0.8 V, C _L = 5 pF			0.5		V/ns
Setup time, RXD[0..15], RKMSB, RKLSB setup to ↑ RXCLK	t _{su}	See figure 5b. 50% voltage swing TXCLK = 80 MHz ^{3/}			3		ns
		See figure 5b. 50% voltage swing TXCLK = 125 MHz ^{3/}			2.5		
Hold time, RXD[0..15], RKMSB, RKLSB hold to ↑ RXCLK	t _h	See figure 5b. 50% voltage swing TXCLK = 80 MHz ^{3/}	3		ns		
		See figure 5b. 50% voltage swing TXCLK = 125 MHz ^{3/}	2				
Transmitter/Receiver Characteristics							
Preemphasis VOD, direct, V _{OD(p)} = V _{TXP} - V _{TXN}	V _{OD(p)}	See figure 5c. R _t = 50 Ω, PREM = high, dc-coupled		All	655	1100	mV
		See figure 5c. R _t = 50 Ω, PREM = low, dc-coupled			590	1050	
Differential, peak-to-peak output voltage with preemphasis	V _{OD(pp-p)}	See figure 5c. R _t = 50 Ω, PREM = high, dc-coupled			1310	2200	mV _{p-p}
		See figure 5c. R _t = 50 Ω, PREM = low, dc-coupled			1180	2100	
Deemphasis output voltage V _{TXP} - V _{TXN}	V _{OD(d)}	See figure 5c. R _t = 50 Ω, dc-coupled			540	950	mV
Differential, peak-to-peak output voltage with deemphasis	V _{OD(pp-d)}	See figure 5c. R _t = 50 Ω, dc-coupled			1080	1900	mV _{p-p}

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transmitter/Receiver Characteristics							
Transmit common mode voltage range, (VTXP + VTXN)/2	V _(cmt)	See figure 5c. R _t = 50 Ω		All	1000	1400	mV
Receiver input voltage differential, VRXP – VRXN (Single Ended)	V _{ID} <u>3/</u>				220	1600	mV
Receiver common mode voltage range, (VRXP + VRXN)/2	V _(cmr) <u>3/</u>				1000	2250	mV
Receiver input leakage current	I _{lkg}				-10	10	μA
Receiver input capacitance	C _I	See 4.4.1c			4 TYP		pF
Serial data total jitter (peak-to-peak)		Differential output jitter at 2.5 Gbps, random + deterministic, PRBS pattern			0.28 TYP		UI <u>4/</u>
		Differential output jitter at 1.6 Gbps, random + deterministic, PRBS pattern			0.32 TYP		
Differential output signal rise and fall time (20% to 80%)	t _r , t _f	See figure 5c. R _L = 50 Ω, C _L = 5 pF			150 TYP		ps
Jitter tolerance eye closure		Differential input jitter, random + deterministic, PRBS pattern at zero crossing			0.40		UI <u>3/</u> <u>4/</u>
Tx latency	t _d (Tx latency)	See figure 5d.			34	38	bits
Rx latency	t _d (Rx latency)	See figure 5e.			76	107	bits

Thermal Characteristics

Junction-to-free-air thermal resistance	R _{θJA}	Board-mounted, per JESD51-5 Methodology.		All	31.5 TYP	°C/W
Junction-to-case thermal resistance	R _{θJC}	MIL-STD-883 Test Method 1012.			2.96 TYP	°C/W

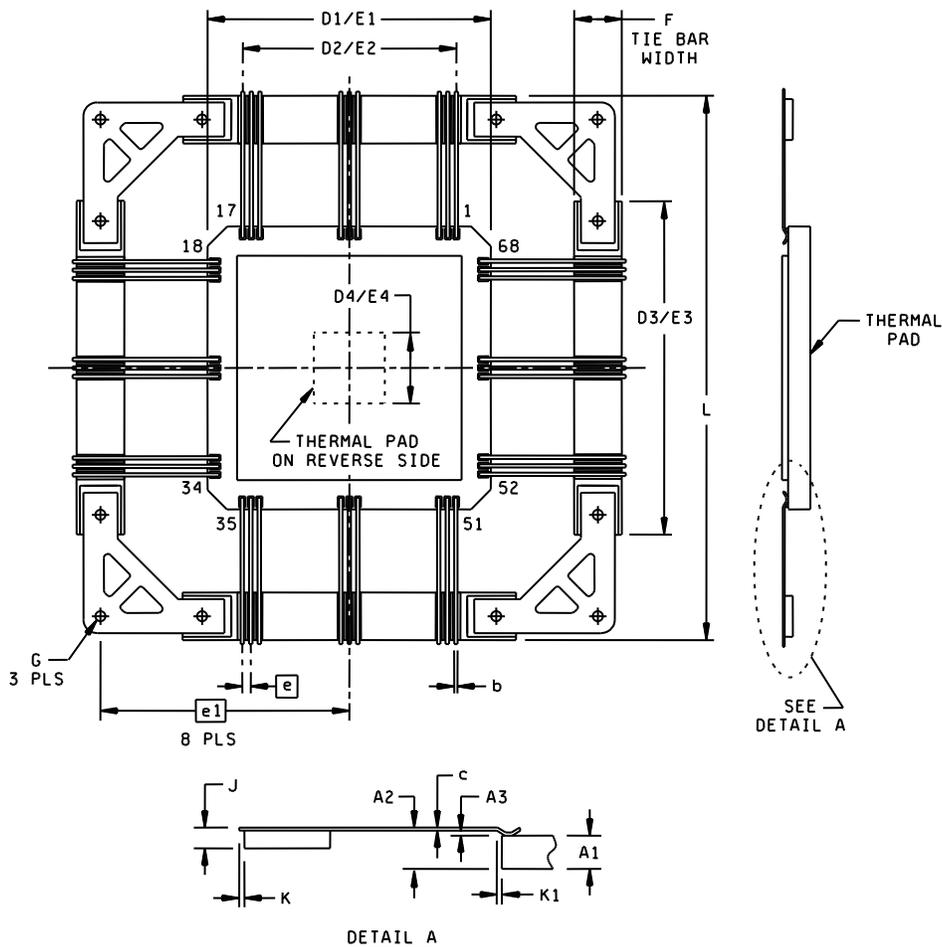
^{1/} Over recommended operating conditions (unless otherwise specified).

^{2/} TTL signals: TXD0 – TXD15, TXCLK, LOOPEN, LCKREFN, ENABLE, PRBS_EN, TKLSB, TKMSB, PRE

^{3/} Characterized parameter, not production tested.

^{4/} UI is the time interval of one serialized bit.

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Thermal note: This package has built in vias which electrically and thermally connect the bottom of the die to a pad on the bottom of the package. In order to efficiently remove heat and provide a low impedance ground path, a thermal land is required on the surface of the printed circuit board directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package will be soldered to this thermal land creating an efficient thermal path.

Normally, the printed circuit board thermal land will have a number of thermal vias within it that provide a thermal path to internal copper areas, or to the opposite side of the printed circuit board, that provide for more efficient heat removal.

An 11.9 mm x 11.9 mm board mount thermal pad with a 4.2 mm x 4.2 mm solder mask defined pad attach opening is recommended. This allows maximum area for thermal dissipation while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically grounded potential.

FIGURE 2. Case outline.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	---	0.090	---	2.29
A2	---	0.105	---	2.68
A3	0.002	0.014	0.05	0.36
b	0.006	0.010	0.15	0.25
c	0.004	0.008	0.10	0.20
D1/E1	0.542	0.558	13.77	14.17
D2/E2	0.400 NOM		10.16 NOM	
D3/E3	0.940	0.960	23.88	24.38
D4/E4	0.165 NOM		4.191 NOM	
e	0.025 NOM		0.64 NOM	
e1	0.73 NOM		18.52 NOM	
F	0.125	0.145	3.18	3.68
G	0.059	0.063	1.50	1.60
J	0.030	0.040	0.76	1.02
K	---	0.020	---	0.51
K1	---	0.018	---	0.46
L	1.584	1.616	40.23	41.05

NOTES:

1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
4. This package is hermetically sealed with a metal lid.
5. The leads are gold plated and can be solder dipped.
6. All leads are not shown for clarity purposes.
7. Thermal dissipation enhancement provided by vias to external bottom pad.
8. Lid and thermal pad are connected to GND leads.
9. Pin 1 corner has a larger chamfer.

FIGURE 2. Case outline - Continued.

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Case outline: X			
Terminal number	Terminal name	Terminal number	Terminal name
1	V _{DD}	35	GND
2	TXD3	36	RXD13
3	TXD4	37	RXD12
4	TXD5	38	RXD11
5	GND	39	RXD10
6	TXD6	40	V _{DD}
7	TXD7	41	RXD9
8	GTX_CLK	42	RXD8
9	V _{DD}	43	RX_CLK
10	TXD8	44	RXD7
11	TXD9	45	GND
12	TXD10	46	RXD6
13	GND	47	RXD5
14	TXD11	48	RXD4
15	TXD12	49	RXD3
16	TXD13	50	V _{DD}
17	GND	51	GND
18	TXD14	52	RXD2
19	GND	53	RXD1
20	TXD15	54	RXD0
21	TKMSB	55	GND
22	LOOPEN	56	DINRXN
23	TKLSB	57	DINRXP
24	V _{DD}	58	GND
25	ENABLE	59	V _{DDA}
26	LCKREFN	60	PRE
27	PRBSEN	61	V _{DDA}
28	TESTEN	62	GND
29	GND	63	DOU _{TTXN}
30	RKLSB	64	DOU _{TTXP}
31	RKMSB	65	GND
32	RXD15	66	TXD0
33	RXD14	67	TXD1
34	GND	68	TXD2

FIGURE 3. Terminal connections.

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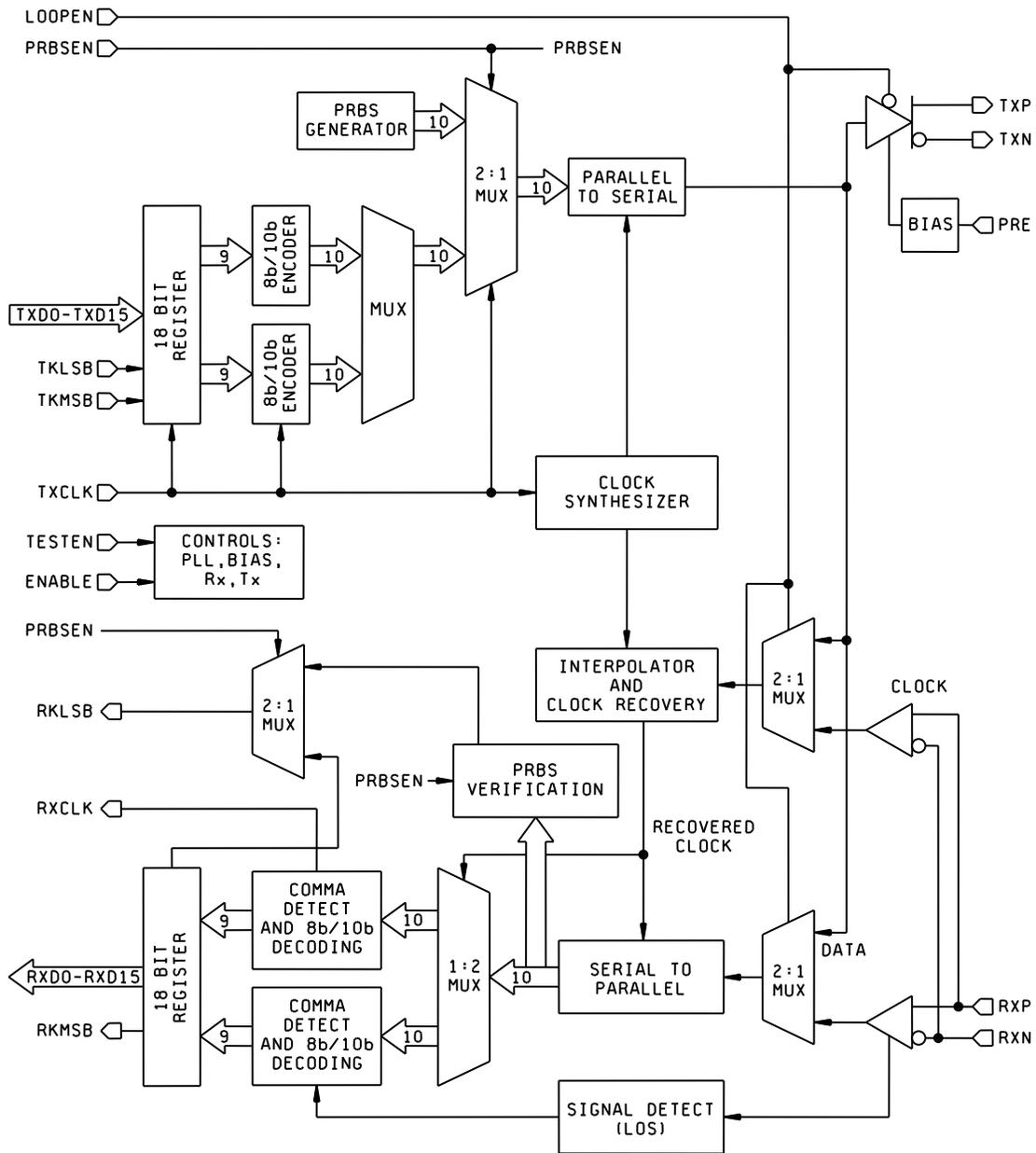


FIGURE 4. Block diagram.

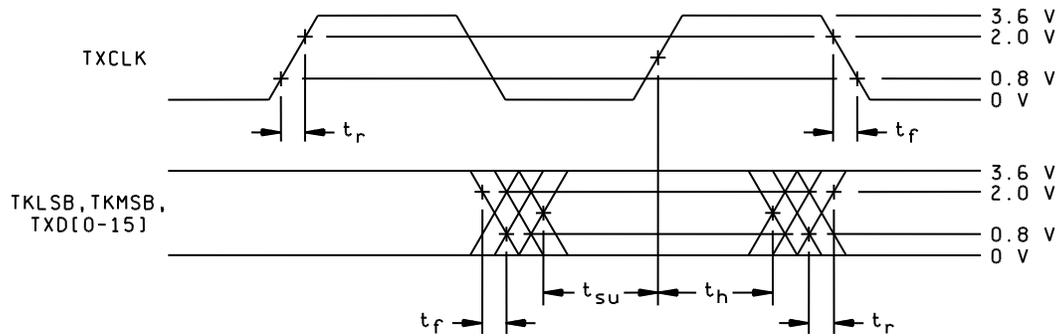
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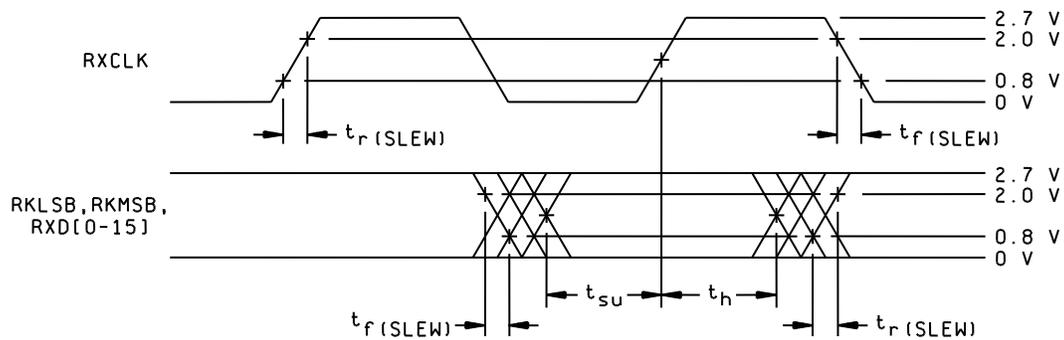
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TTL DATA INPUT VALID LEVELS FOR AC MEASUREMENTS

FIGURE 5a. Switching waveforms.



TTL DATA OUTPUT VALID LEVELS FOR AC MEASUREMENTS

FIGURE 5b. Switching waveforms.

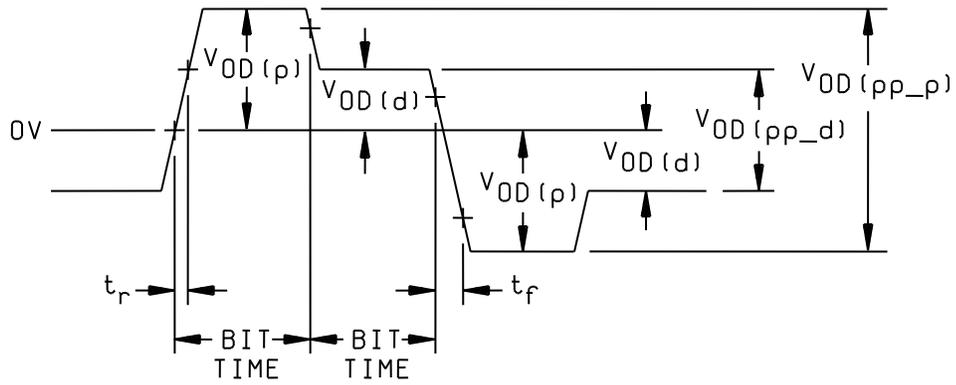
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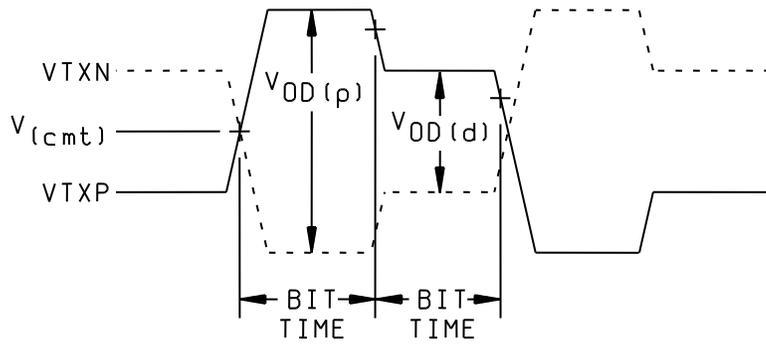
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DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGE



COMMON MODE OUTPUT VOLTAGE DEFINITIONS

FIGURE 5c. Switching waveforms.

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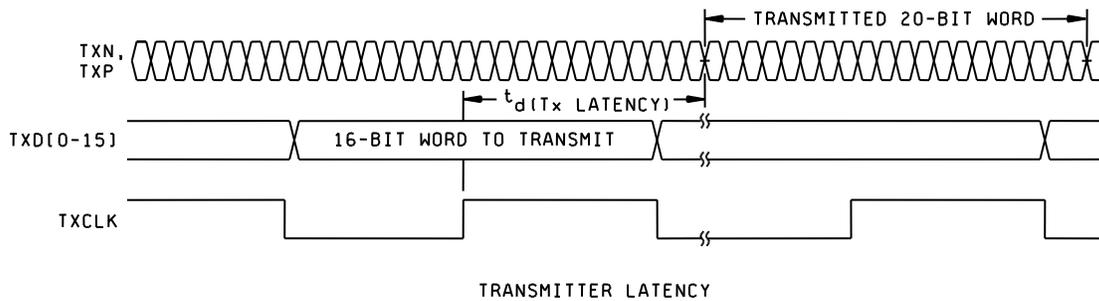


FIGURE 5d. Switching waveforms.

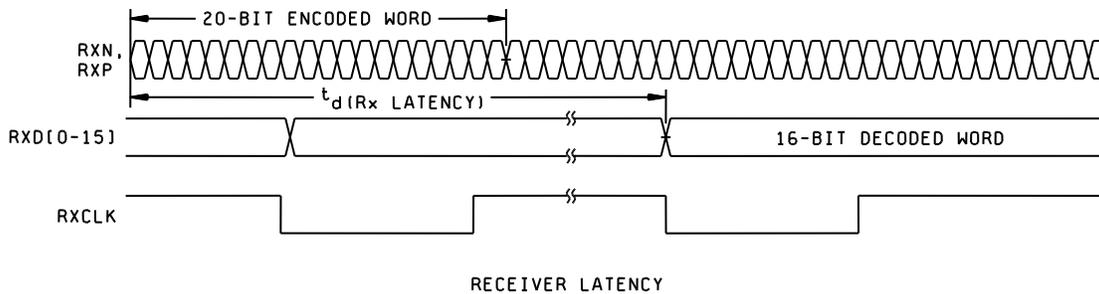


FIGURE 5e. Switching waveforms.

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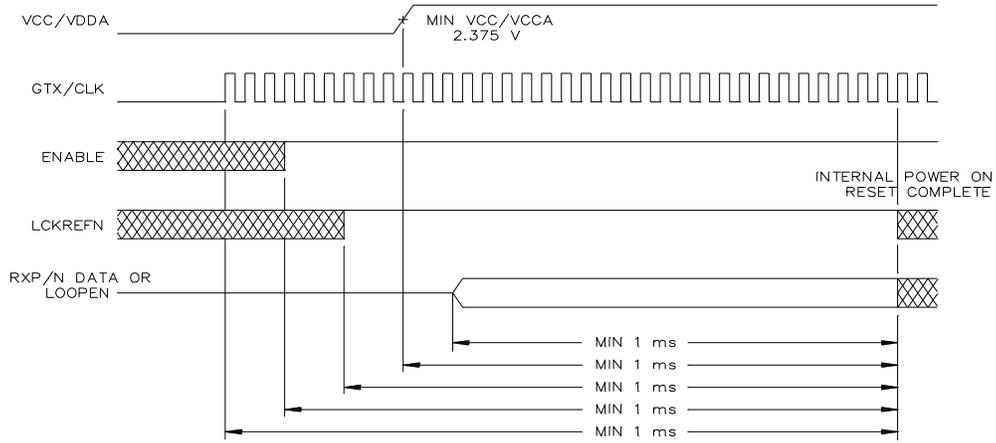


FIGURE 5f. Switching waveforms for power-on/reset mode(option 1).

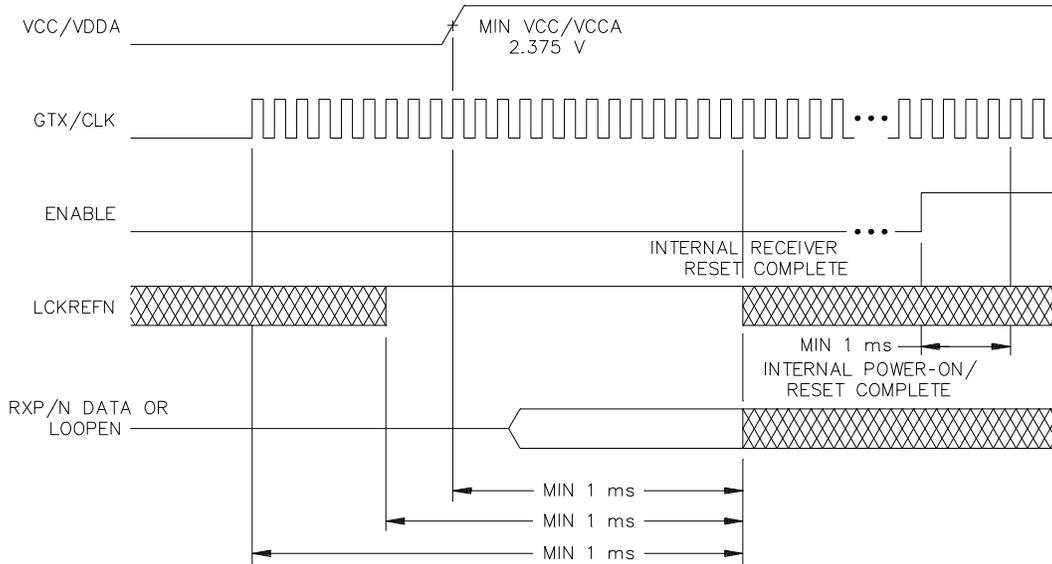


FIGURE 5g. Switching waveforms for power-on/reset mode (option 2).

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C_i measurement) shall be measured only for initial test and after process or design changes which may affect input capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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TABLE III. Terminal Functions.

Terminal Name	Terminal Number	I/O	Description
ENABLE	25	I <u>1</u> /	<u>Device enable.</u> When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When in power down mode, RKMSB will output the status of signal detect circuit (LOS). When asserted high while the device is in power-down mode, the transceiver is reset before beginning normal operation.
GND	5, 13, 17, 19, 29, 34, 35, 45, 51, 55, 58, 62, 65		<u>Analog and Digital logic ground.</u> Provides a ground for the logic circuits, digital I/O buffers, and the high-speed analog circuits.
LCKREFN	26	I <u>1</u> /	<u>Lock to reference.</u> When LCKREFN is low, the receiver clock is frequency locked to TXCLK. This places the device in a transmit-only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals (RXD0–RXD15, RXCLK, RKLSB, and RKMSB) are in a high-impedance state if device is enabled (ENABLE = H). If device is disabled (ENABLE = L), then RKMSB will output the status of the LOS detector (active low = LOS). All other receive outputs will remain high-impedance. When LCKREFN is deasserted high, the receiver is locked to the received data stream. LCKREFN must be deasserted to a high state during power-on reset (see power-on reset timing diagram figure 5f and 5g and notes under power-on reset for power up)
LOOPEN	22	I <u>2</u> /	<u>Loop enable.</u> When LOOPEN is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRE	60	I <u>2</u> /	<u>Preemphasis control.</u> Selects the amount of preemphasis to be added to the high speed serial output drivers. Left low or unconnected, 5% preemphasis is added. Pulled high, 20% preemphasis is added.
PRBSEN	27	I <u>2</u> /	<u>PRBS test enable.</u> When asserted high results of pseudo random bit stream (PRBS) tests can be monitored on the RKLSB terminal. A high on RKLSB indicates that valid PRBS is being received.
RKLSB	30	O	<u>K-Code indicator/PRBS test results.</u> When RKLSB is asserted high, an 8-bit/10-bit K code was received and is indicated by data bits RXD0-RXD7. When RKLSB is asserted low an 8-bit/10-bit D code is received and is presented on data bits RXD0-RXD7. When PRBSEN is asserted high this pin is used to indicate status of the PRBS test results (high = pass).
RKMSB	31	O	<u>K-code indicator.</u> When RKMSB is asserted high an 8-bit/10-bit K code was received and is indicated by data bits RXD8–RXD15. When RKMSB is asserted low an 8-bit/10-bit D code was received and is presented on data bits RXD8–RXD15. If the differential signal on RXN and RXP drops below 200 mV, RXD0–RXD15, RKLSB, and RKMSB are all asserted high. When device is disabled (ENABLE = L), RKMSB will output the status of LOS. Active low = LOS detected.
RXCLK, RX_CLK	43	O	<u>Recovered clock.</u> Output clock that is synchronized to RXD[0..9], RKLSB, and RKMSB. RXCLK is the recovered serial data rate clock divided by 20. RXCLK is held low during power-on reset.

See footnotes at end of table.

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TABLE III. Terminal Functions - Continued.

Terminal Name	Terminal Number	I/O	Description
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15	54 53 52 49 48 47 46 44 42 41 39 38 37 36 33 32	O	<u>Received data bus.</u> These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RXCLK. The data is valid on the rising edge of RXCLK. These terminals are in high-impedance state during power-on reset.
DINRXN, DINRXP	56, 57	I	<u>Serial receive inputs.</u> RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
TESTEN	28	I <u>2/</u>	<u>Test mode enable.</u> This terminal should be left unconnected or tied low.
TKLSB	23	I <u>2/</u>	<u>K-code generator (LSB).</u> When TKLSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD0-TXD7. When TKLSB is low an 8-bit/10-bit D code is transmitted as controlled by data bits TXD0-TXD7.
TKMSB	21	I <u>2/</u>	<u>K-code generator (MSB).</u> When TKMSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD8-TXD15. When TKMSB is low an 8-bit/10-bit D code is transmitted as controlled by data bits TXD8-TXD15.
TXCLK, GTX_CLK	8	I	<u>Reference clock.</u> TXCLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB, and TXD[0..15]. The frequency range of TXCLK is 80 MHz to 135 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data TXD[0..15] for serialization.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15	66 67 68 2 3 4 6 7 10 11 12 14 15 16 18 20	I	<u>Transmit data bus.</u> These inputs carry 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of TXCLK.

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TABLE III. Terminal Functions - Continued.

Terminal Name	Terminal Number	I/O	Description
DOU _{TXN} , DOU _{TXP}	63, 64	O	<u>Serial transmit outputs.</u> TXP and TXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the TXCLK value. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset, these terminals are high-impedance.
V _{DD}	1, 9, 24, 40, 50		<u>Digital logic power.</u> Provides power for all digital circuitry and digital I/O buffers.
V _{DDA}	59, 61		<u>Analog power.</u> V _{DDA} provides a supply reference for the high-speed analog circuits, receiver and transmitter.

1/ Internal 10 kΩ pull-up.

2/ Internal 10 kΩ pull-down.

NOTES: Upon application of minimum valid power and valid GTX_CLK with device enabled (ENABLE = HIGH), the TLK2711-SP generates a power-on reset. During the power-on reset the RXD0 to RXD15, RKLSB, and RKMSB signal pins go to a high-impedance state. The RXCLK is held low. LCKREFN must be deasserted (logic high state) with active transitions on the receiver during the power-on reset period. Active transitions on receiver can be accomplished with transitions on RXP/N or by assertion of LOOPEN. For TX-only applications, LOOPEN and LCKREFN can be driven logic high together. The receiver circuit requires this to properly reset. After power-up reset period, LCKREFN can be asserted for transmit only applications. The length of the power-on reset cycle depends on the TXCLK frequency, but is less than 1 ms. See figure 5f for power up option 1. Option 1 shows timing requirements when ENABLE = HIGH at power up. See figure 5g for power up option 2. Option 2 resets the receiver circuit immediately at power up without enabling complete device with ENABLE = LOW. The complete reset of device occurs after ENABLE is asserted HIGH. LCKREFN does not need to continue to be logic high after the initial 1-ms reset period. Vendor recommends that the receiver be reset immediately after power up using options 1 or 2. In some conditions, it is possible for the receiver circuit to power up in state with internal contention.

If LCKREFN cannot be deasserted high during or for the complete power-on reset period, it can be deasserted high at the end of or after the power-on reset period for minimum of 1 μS with active transitions on receiver to properly complete reset of receiver.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-08-25

Approved sources of supply for SMD 5962-05221 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0522101VXC	01295	TLK2711-SP
		TLK2711M <u>3/</u>

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from approved source of supply.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of Contact:

U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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