REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Changed Table I parameters for Supply current operating @ 1 MHz from 40 mA to 70 mA, Supply current operating @ 58.8 MHz from 100 mA to 122 mA. Changed Supply current standby @ 0 MHz and 58.8 MHz the symbol is $I_{DD1}^{(SB)}$ on Table I from 35 mA to 65 mA. Changed Supply current standby @ 0 MHz and 58.8 MHz the symbol is $I_{DD2}^{(SB)}$ on Table I from 5 µA to 8 µA. Changed Data retention current for subgroup 2 from 30 mA to 55 mA, and for subgroups 1 and 3; from 500 µA to 700 µA. - ksr	05-11-29	Raymond Monnin
C	Section 1.3, changed supply voltage range high end (V_{DD1}) to 2.1V, changed T_A to T_C. Section 1.4 changed T_A to T_C, added new footnote 4/. Renumbered footnotes in section 1.5. Made significant change to max value in Table I for Operating supply current I_{DD1} and Supply current standby I_{DD1}. New footnote 2/ added, other footnotes renumbered. Made changes to Figure 1 case outline X for dimensions b through c1, D1, and E1. – ksr	09-09-15	Charles Saffle
D	Update drawing to meet current MIL-PRF-38535 requirements. Removed class M references. – glg	17-04-20	Charles Saffle
E	Update Figure 1, Case Outline X to include detail A, lead length, and unformed lead dimensions. – glg	18-10-23	Charles Saffle
F	VEN EOL RHA level F devices and add RHA level R devices. Update to current MIL-PRF-38535 requirements. – llb	20-10-15	James Eschmeyer
G	Update to section 1.5 to clarify that RHA level F devices are discontinued. – llb	21-09-23	James Eschmeyer

REV																				
SHEET																				
REV	G	G	G	G	G	G	G													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
05-03-31

REVISION LEVEL
G

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K x 32-BIT (16 M), RADIATION-HARDENED, DUAL VOLTAGE SRAM, MULTICHIP MODULE

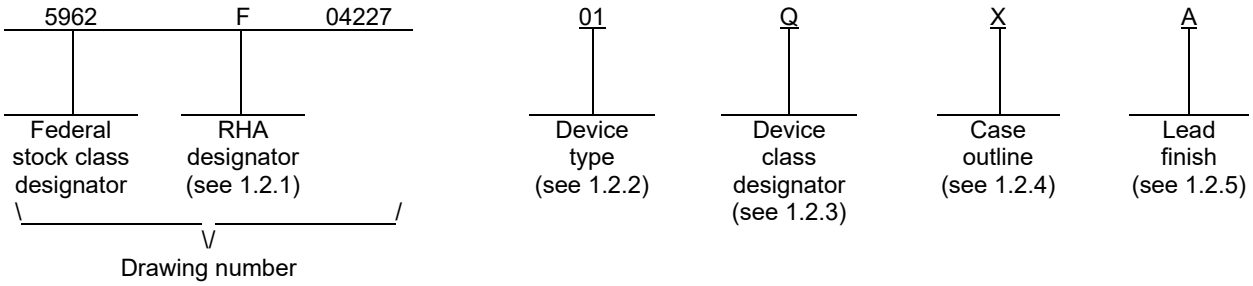
SIZE	CAGE CODE	
A	**67268**	**5962-04227**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	8CR512K32	512K X 32-bit rad-hard SRAM (Mil Temp)	17 ns
02	8CR512K32	512K X 32-bit rad-hard SRAM (Extended Temp)	17 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{DD1})	-0.3 V dc to +2.4 V dc
Supply voltage range, (V_{DD2})	-0.3 V dc to +4.5 V dc
Voltage range on any pin	-0.3 V dc to +4.5 V dc
Input current, dc	± 5 mA
Power dissipation	1.2 W
Case temperature range, (T_C) Device 01	-55°C to +125°C
Device 02	-40°C to +125°C
Storage temperature range, (T_{STG})	-65°C to +150°C
Junction temperature, (T_J)	+150°C
Thermal resistance, junction-to-case, (θ_{JC}): Case X	+5°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{DD1})	+1.7 V dc to +1.9 V dc 4/
Supply voltage range, (V_{DD2})	+3.0 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to V_{DD2}
Case temperature range, (T_C) Device 01	-55°C to +125°C
Device 02	-40°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 1 rad(Si)/s)	300 krad(Si) 5/ 6/
Maximum total dose available (dose rate = 1 rad(Si)/s)	100 krads(Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4)	≤ 100 MeV-cm^2/mg 7/
No SEU occurs at on set LET (see 4.4.4)	≤ 9 MeV-cm^2/mg 7/
Dose rate upset	1 x 10^9 rad(Si)/s 7/
Dose rate latch-up	1.2 x 10^{12} rad(Si)/s 7/

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltage values in this drawing are with respect to V_{SS}.

4/ For increase noise immunity, supply voltage (V_{DD1}) can be increased to 2.0 V. The parameters in Table IA, (Electrical performance characteristics) are guaranteed through characterization at V_{DD1} = 2.0 V dc.

5/ Contact the device manufacturer for detailed lot information.

6/ RHA level F devices have been discontinued.

7/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 – Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 – IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Device 01) $-40°C \le T_C \le +125°C$ (Device 02) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD1} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
High-level input voltage	V_{IH}		1, 2, 3	All	$.7*V_{DD2}$		V
Low-level input voltage	V_{IL}		1, 2, 3	All		$.3*V_{DD2}$	V
High-level output voltage	V_{OH1}	I_{OH} = -4 mA, $V_{DD2} = V_{DD2}$(min)	1, 2, 3	All	$.8*V_{DD2}$		V
Low-level output voltage	V_{OL1}	I_{OL} = 8 mA, $V_{DD2} = V_{DD2}$(min)	1, 2, 3	All		$.2*V_{DD2}$	V
Input capacitance 3/	C_{IN}	f = 1 MHz @ 0 V, see 4.4.1e	4	All		44	pF
Bidirectional I/O capacitance 3/	C_{IO}		4	All		21	pF
Input leakage current	I_{IN}	$V_{IN} = V_{DD2}$ and V_{SS}	1, 2, 3	All	-2	2	µA
Three state output leakage current	I_{OZ}	$V_O = V_{DD2}$ and V_{SS}, $V_{DD2} = V_{DD2}$(max), $\overline{G} = V_{DD2}$(max)	1, 2, 3	All	-2	2	µA
Short-circuit output current 4/ 5/	I_{OS}	$V_{DD2} = V_{DD2}$(max), $V_O = V_{DD2}$, V_{DD1} = 1.9 V, $V_O = V_{SS}$	1, 2, 3	All	-100	100	mA
Supply current operating @ 1 MHz	$I_{DD1}^{(OP1)}$	Inputs: $V_{IL} = V_{SS}$ + 0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 V_{DD1} = 1.9 V, $V_{DD2} = V_{DD2}$(max)	1, 2, 3	All		70	mA
		Inputs: $V_{IL} = V_{SS}$ + 0.2 V $V_{IH} = V_{DD2}$ – 0.2 V, I_{OUT} = 0 V_{DD1} = 2.0 V, $V_{DD2} = V_{DD2}$(max)				76	
Supply current operating @ 58.8 MHz	$I_{DD1}^{(OP2)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 V_{DD1} = 1.9 V, $V_{DD2} = V_{DD2}$(max)	1, 2, 3	All		122	mA
		Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0 V_{DD1} = 2.0 V, $V_{DD2} = V_{DD2}$(max)				150	
Supply current operating @ 1 MHz	$I_{DD2}^{(OP1)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V, $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0, $V_{DD1} = V_{DD1}$(max), $V_{DD2} = V_{DD2}$(max)	1, 2, 3	All		.35	mA
Supply current operating @ 58.8 MHz	$I_{DD2}^{(OP2)}$	Inputs: $V_{IL} = V_{SS}$ +0.2 V $V_{IH} = V_{DD2}$ -0.2 V, I_{OUT} = 0, $V_{DD1} = V_{DD1}$(max), $V_{DD2} = V_{DD2}$(max)	1, 2, 3	All		11	mA
Functional test		See 4.4.1c, T_C = 25°C	7, 8A, 8B	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Device 01) $-40°C \le T_C \le +125°C$ (Device 02) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD1} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Supply current standby @ 0 MHz	$I_{DD1}^{(SB)}$	CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = 1.9\ V$, $V_{DD2} = V_{DD2}(max)$	1, 2, 3	All		65	mA
		CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = 2.0\ V$, $V_{DD2} = V_{DD2}(max)$				72	
	$I_{DD2}^{(SB)}$	CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = V_{DD1}(max)$, $V_{DD2} = V_{DD2}(max)$				8	µA
Supply current standby A(18:0) @ 58.8 MHz	$I_{DD1}^{(SB)}$	CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = 1.9\ V$, $V_{DD2} = V_{DD2}(max)$	1, 2, 3	All		65	mA
		CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = V_{DD1}(max)$, $V_{DD2} = V_{DD2}(max)$				72	
	$I_{DD2}^{(SB)}$	CMOS inputs: $I_{OUT} = 0$, $V_{IL} = 0$, $\overline{E} = V_{DD2} - 0.2\ V$, $V_{IH} = V_{DD2}(max)$, $V_{DD1} = V_{DD1}(max)$, $V_{DD2} = V_{DD2}(max)$				8	µA
Data retention current	I_{DDR}		1	All		700	µA
			2			55	mA
			3			700	µA
V_{DD1} for data retention	V_{DR}		1, 2, 3	All	1		V
Chip deselect to data Retention time	t_{EFR}	$\overline{E} = V_{DD2}$ all other inputs = V_{DD2} or V_{SS}; $V_{DD2} = 0\ V$ to $V_{DD2}(max)$	9, 10, 11	All	0		ns
Operation recovery time	t_R		9, 10, 11	All	t_{AVAV}		ns
Read cycle time 3/ 10/	t_{AVAV}	See figures 4 and 5 as applicable	9, 10, 11	All	17		ns
Address valid to address valid skew time 9/	t_{AVSK}		9, 10, 11	All		4	ns
Read access time	t_{AVQV}		9, 10, 11	All		17	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Device 01) $-40°C \le T_C \le +125°C$ (Device 02) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD1} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Output hold time 6/	t_{AXQX}	See figures 4 and 5 as applicable	9, 10, 11	All	3		ns
$\overline{G}$-controlled output enable time 3/ 6/	t_{GLQX}		9, 10, 11	All	0		ns
$\overline{G}$-controlled read access time	t_{GLQV}		9, 10, 11	All		7	ns
$\overline{G}$-controlled output three-state time 6/	t_{GHQZ}		9, 10, 11	All		7	ns
E-controlled output enable time 6/ 7/	t_{ETQX}		9, 10, 11	All	5		ns
E-controlled address setup time for read 9/	t_{AVET2}		9, 10, 11	All	-4		ns
E-controlled access time 7/	t_{ETQV}		9, 10, 11	All		17	ns
E-controlled output three-state time 8/	t_{EFQZ}		9, 10, 11	All		10	ns
Write cycle time	t_{AVAV}	See figures 4 and 5 as applicable $\overline{G} = V_{DD2}$	9, 10, 11	All	17		ns
Device enable to end of write	t_{ETWH}	See figures 4 and 5 as applicable	9, 10, 11	All	12		ns
Address set-up time for write ($\overline{E}$-controlled)	t_{AVET}		9, 10, 11	All	0		ns
Address set-up time for write ($\overline{W}$-controlled)	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	All	12		ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	All	2		ns
Address hold time for device enable ($\overline{E}$-controlled)	t_{EFAX}		9, 10, 11	All	0		ns
$\overline{W}$-controlled three-state time 6/	t_{WLQZ}		9, 10, 11	All		5	ns
$\overline{W}$-controlled output enable time 6/	t_{WHQX}		9, 10, 11	All	4		ns
Device enable pulse width ($\overline{E}$-controlled)	t_{ETEF}		9, 10, 11	All	12		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Device 01) $-40°C \le T_C \le +125°C$ (Device 02) $+1.7\ V \le V_{DD1} \le +1.9\ V$ $+3.0\ V \le V_{DD1} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Data set-up time	t_{DVWH}	See figures 4 and 5 as applicable	9, 10, 11	All	7		ns
Data hold time	t_{WHDX}		9, 10, 11	All	2		ns
Device enable controlled write pulse width	t_{WLEF}		9, 10, 11	All	12		ns
Data set-up time	t_{DVEF}		9, 10, 11	All	12		ns
Data hold time	t_{EFDX}		9, 10, 11	All	0		ns
Address valid to end of write	t_{AVWH}		9, 10, 11	All	12		ns
Write disable time	t_{WHWL}	See figures 4 and 5 as applicable $\overline{G} = V_{DD2}$	9, 10, 11	All	3		ns

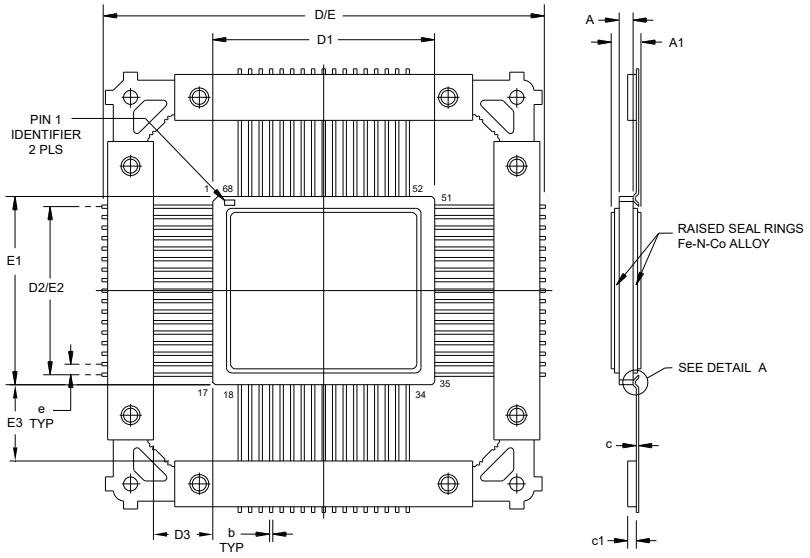
1/ Devices Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post \ irradiation electrical measurements for any RHA level, $T_A = +25°C$.
2/ Limits are guaranteed by characterization with $V_{DD1} = 2.0$ V, if not tested. Reference note 4/ of section 1.4 herein.
3/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table IA.
4/ Supplied as a design limit but not guaranteed or tested.
5/ Not more than one output may be shorted at a time, for a maximum duration of one second.
6/ Three-state is defined as a 200 mV change from steady-state output voltage.
7/ The ET (enable true) notation refers to the latter falling edge of $\overline{E}$. SEU immunity does not affect the read parameters.
8/ The EF (enable false) notation refers to the latter rising edge of $\overline{E}$. SEU immunity does not affect the read parameters.
9/ Guaranteed by design.
10/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation.

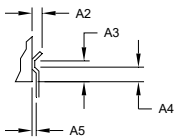
TABLE IB. SEP test limits. 1/ 2/ 4/

Device type	Test	Bias $V_{DD1} = 1.9$ V and $V_{DD2} = 3.6$ V for SEL test 3/ No SEL occurs at effective LET
All	No SEL	LET ≤ 100 MeV/(mg/cm^2)
All	No SEU	On set LET ≤ 9 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for worst case operating temperature $T_A = +125°C \pm 10°C$ for SEL test and $T_A = +25°C \pm 10°C$ for SEU.
4/ For SEP details information contact the device manufacturer.

Case outline X





DETAIL A

FIGURE 1. Case outline.

Case outline X – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		2.464		0.097
A1		5.588		0.220
A2		0.508		.020
A3		0.762		.030
A4		0.4572		.018
A5	0.051	0.3556	.002	.014
b	0.356	0.432	0.014	0.017
c	0.127	0.203	0.005	0.008
c1	0.762	1.016	0.030	0.040
e	1.27 BSC		.050 BSC	
D/E		72.898		2.870
D1	32.054	32.715	1.262	1.288
D3		13.79 (ref.)		.543 (ref.)
E1	26.467	27.127	1.042	1.068
E3		16.59 (ref.)		.653 (ref.)
D2/E2		20.32 (typ.)		.800 (typ.)

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The lids are electrically connected to V_{SS}.
4. Lead finish is in accordance with MIL-PRF-38535.
5. Tie bar dimensions are for reference only.

FIGURE 1. Case outline – Continued.

Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	DQ0(0)
2	DQ1(0)
3	DQ2(0)
4	DQ3(0)
5	DQ4(0)
6	DQ5(0)
7	DQ6(0)
8	DQ7(0)
9	V_{SS}
10	DQ0(1)
11	DQ1(1)
12	DQ2(1)
13	DQ3(1)
14	DQ4(1)
15	DQ5(1)
16	DQ6(1)
17	DQ7(1)
18	V_{DD2}
19	A11
20	A12
21	A13
22	A14
23	A15
24	A16
25	$\overline{E0}$
26	$\overline{G}$
27	$\overline{E1}$
28	A17
29	$\overline{W1}$
30	$\overline{W2}$
31	$\overline{W3}$
32	A18
33	V_{DD1}
34	V_{SS}

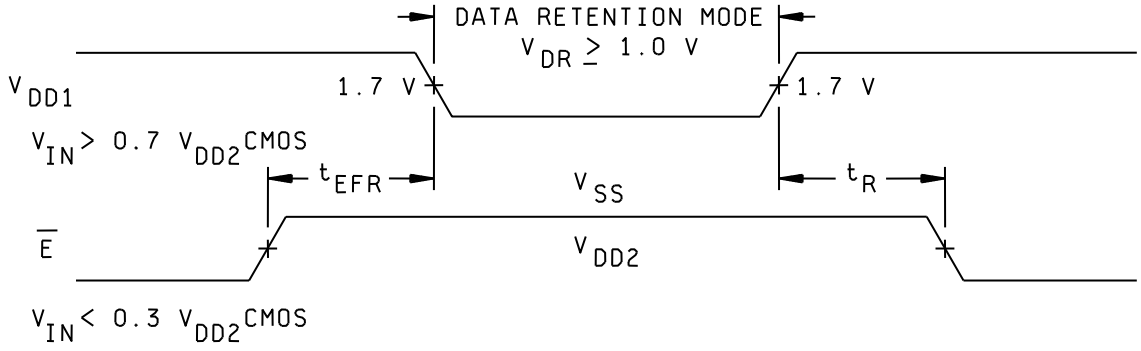
Device types	All
Case outlines	X
Terminal number	Terminal symbol
35	DQ7(3)
36	DQ6(3)
37	DQ5(3)
38	DQ4(3)
39	DQ3(3)
40	DQ2(3)
41	DQ1(3)
42	DQ0(3)
43	V_{SS}
44	DQ7(2)
45	DQ6(2)
46	DQ5(2)
47	DQ4(2)
48	DQ3(2)
49	DQ2(2)
50	DQ1(2)
51	DQ0(2)
52	V_{DD2}
53	A10
54	A9
55	A8
56	A7
57	A6
58	$\overline{W0}$
59	$\overline{E3}$
60	V_{SS}
61	$\overline{E2}$
62	A5
63	A4
64	A3
65	A2
66	A1
67	A0
68	V_{DD1}

FIGURE 2. Terminal connections.

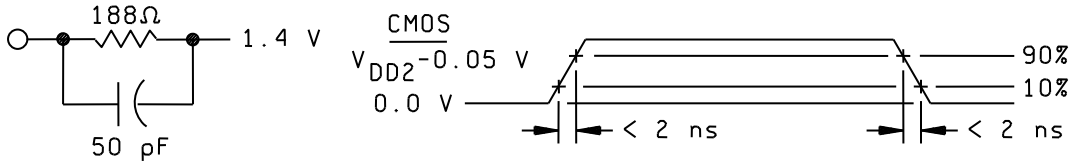
$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X	X	H	Three-state	Standby
X	L	L	Data in	Write
H	H	L	Three-state	Read (device active, outputs disabled)
L	H	L	Data out	Read

Note: L = low, H = high, X = don't care, Z = high impedance

FIGURE 3. Truth table.



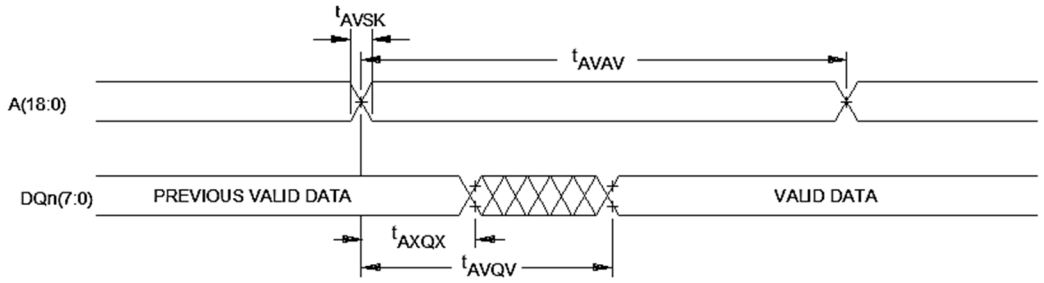
LOW V_{DD} DATA RETENTION WAVEFORM



AC TEST LOADS AND INPUT WAVEFORMS

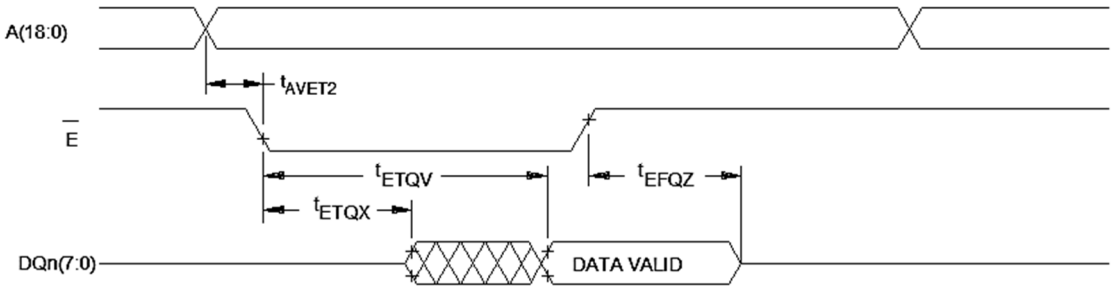
Note: 50 pF including scope probe and test socket.

FIGURE 4. Output load circuit



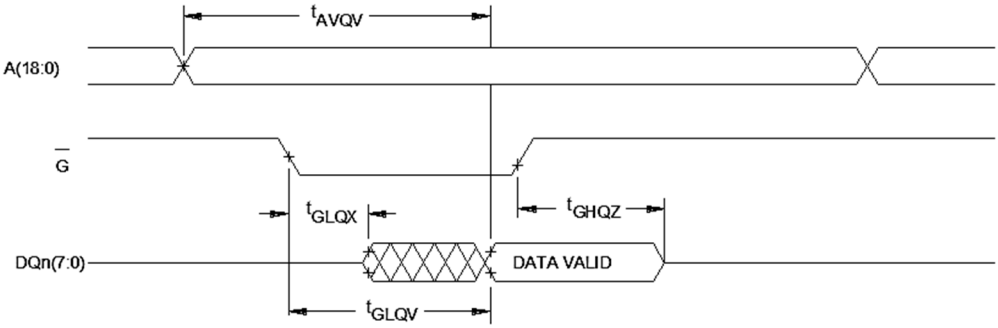
SRAM READ CYCLE 1:ADDRESS ACCESS

Note: $\overline{E}$ and $\overline{G} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)



SRAM READ CYCLE 2:CHIP ENABLE-CONTROLLED ACCESS

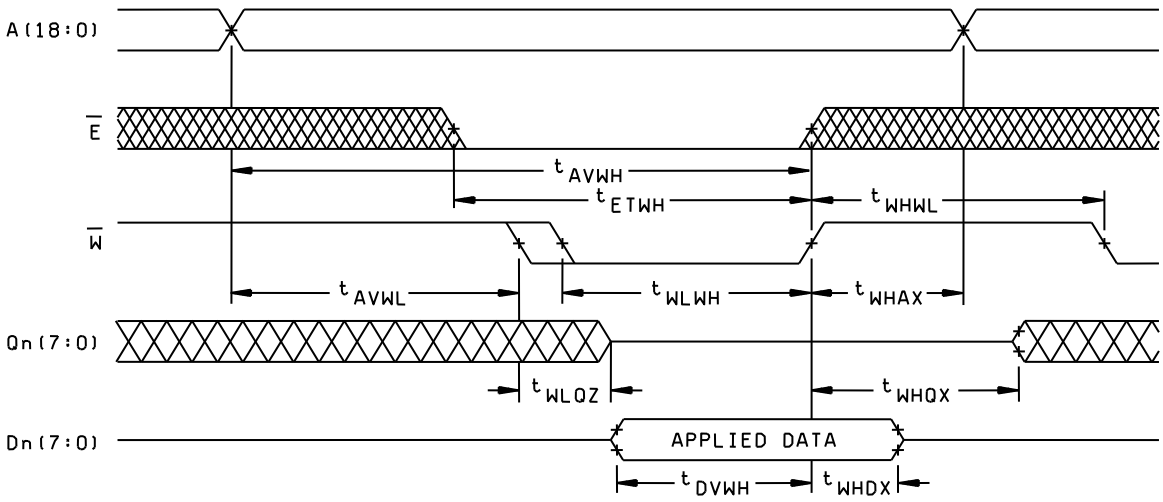
Note: $\overline{G} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)



SRAM READ CYCLE 3:OUTPUT ENABLE-CONTROLLED ACCESS

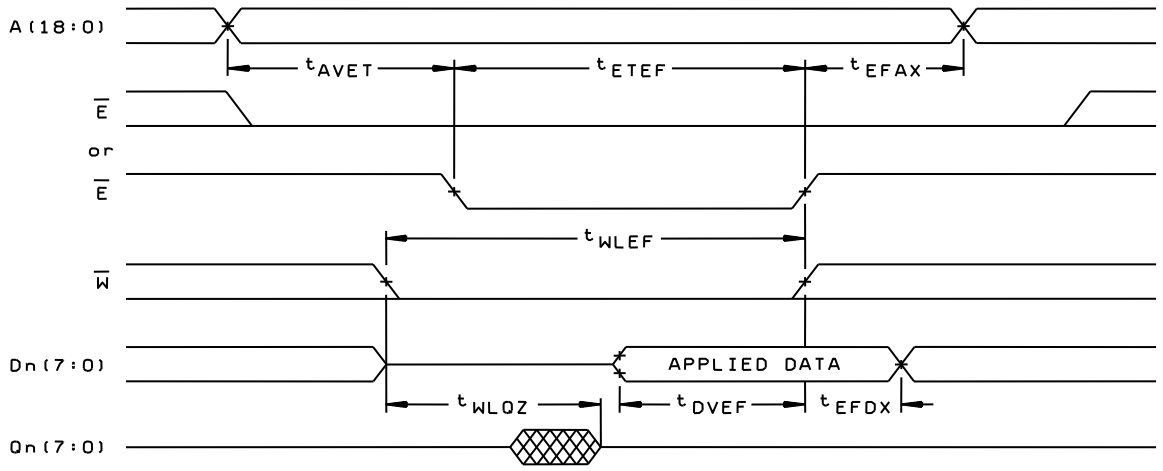
Note: $\overline{E} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)

FIGURE 5. Timing waveforms.



SRAM WRITE CYCLE 1: WRITE ENABLE-CONTROLLED ACCESS

Note: $\overline{G} \le V_{IL}$ (max). If $\overline{G} \ge V_{IH}$ (min) then Qn(8:0) will be in three-state for the entire cycle.



SRAM WRITE CYCLE 2: CHIP ENABLE-CONTROLLED ACCESS

Note: $\overline{G} \le V_{IL}$ (max). If $\overline{G} \ge V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
Either $\overline{E}$ scenario can occur.

FIGURE 5. Timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five (5) devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five (5) devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition B, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. Dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with zero (0) defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four (4) devices with zero (0) failures.

h. For SEP limits see table IB herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	- - -	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	- - -	1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limit	Unit
Supply current standby at 0 MHz I_{DD2}	± 10% of specified value in Table IA or 35 µA whichever is greater 2/	mA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ If device is tested at or below 35 µA, no deltas are required.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
Appendix A forms a part of SMD 5962-04227

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-09-23

Approved sources of supply for SMD 5962-04227 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0422701QXA	3/	UT8CR512K32-17VCA
5962F0422701QXC	3/	UT8CR512K32-17VCC
5962F0422701VXA	3/	UT8CR512K32-17VCA
5962F0422701VXC	3/	UT8CR512K32-17VCC
5962F0422702QXA	3/	UT8CR512K32-17VWA
5962F0422702QXC	3/	UT8CR512K32-17VWC
5962F0422702VXA	3/	UT8CR512K32-17VWA
5962F0422702VXC	3/	UT8CR512K32-17VWC
5962R0422701QXA	65342	UT8CR512K32-17VCA
5962R0422701QXC	65342	UT8CR512K32-17VCC
5962R0422701VXA	65342	UT8CR512K32-17VCA
5962R0422701VXC	65342	UT8CR512K32-17VCC
5962R0422702QXA	65342	UT8CR512K32-17VWA
5962R0422702QXC	65342	UT8CR512K32-17VWC
5962R0422702VXA	65342	UT8CR512K32-17VWA
5962R0422702VXC	65342	UT8CR512K32-17VWC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-7370