REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change “cycle-to-cycle” jitter designation to “period” jitter designation in table I and figure 5 waveforms. Correct pinout in figure 2 case outline. Update drawing boilerplate to latest requirements. - CFS	04-03-11	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	08-11-03	Thomas M. Hess

REV	B	B	B	B	B															
SHEET	75	76	77	78	79															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Charles F. Saffle

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
04-01-06

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, FIXED-POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

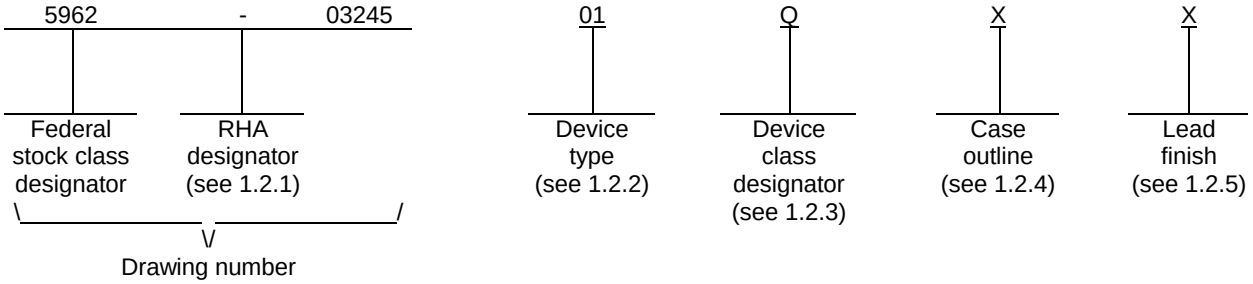
SIZE	CAGE CODE	
A	**67268**	**5962-03245**

SHEET 1 OF 79

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	SMJ320C6415	Fixed-point digital signal processor	600 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
Q or V	Certification and qualification to MIL-PRF-38535.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 2	570	Ceramic pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage core range (CV_{DD})	-0.3 V dc to +1.8 V dc	2/
Supply voltage I/O range (DV_{DD})	-0.3 V dc to +4.0 V dc	2/
Input voltage range (V_{IN}):		
(except PCI)	-0.3 V dc to +4.0 V dc	
(PCI) (V_{IP})	-0.5 V to DV_{DD} + 0.5 V	
Output voltage range (V_{OUT}):		
(except PCI)	-0.3 V dc to +4.0 V dc	
(PCI) (V_{OP})	-0.5 V to DV_{DD} + 0.5 V	
Operating case temperature range (T_C)	-55°C to +115°C	
Storage temperature range (T_{stg})	-65°C to +150°C	

1.4 Recommended operating conditions.

Supply voltage core range (CV_{DD})	+1.36 V dc to +1.44 V dc	3/
Supply voltage I/O range (DV_{DD})	+3.14 V dc to +3.46 V dc	
Supply voltage ground (V_{SS})	+0.0 V dc	
Minimum high level input voltage (except PCI) (V_{IH})	+2.0 V dc	
Maximum low level input voltage (except PCI) (V_{IL})	+0.8 V dc	
Input voltage range (PCI) (V_{IP})	-0.5 V to DV_{DD} +0.5 V	
High level input voltage range (PCI) (V_{IHP})	$0.5DV_{DD}$ to DV_{DD} +0.5 V	
Low level input voltage range (PCI) (V_{ILP})	-0.5 V to $0.3DV_{DD}$	
Maximum voltage during overshoot/undershoot (V_{OS})	-1.0 V dc to +4.3 V dc	4/
Operating case temperature range (T_C)	-55°C to +115°C	

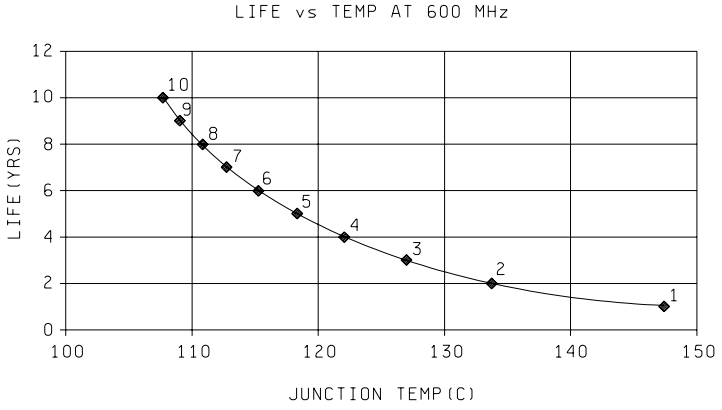


FIGURE 1. Impact of elevated temperature on device life.

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. See figure 1 above for impact of elevated temperature on device life.

2/ All voltage values are with respect to V_{SS}.

3/ Future variants of the C641x DSPs may operate at voltages ranging from 1.2 V to 1.4 V to provide a range of system power/performance options. The manufacturer highly recommends that users design-in a supply that can handle multiple voltages within this range (i.e., 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.4 V with ±3% tolerances) by implementing simple board changes such as reference resistor values or input pin configuration modifications.

4/ The maximum ratings should not be exceeded for more than 30% of the cycle period.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of documents are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1149.1-1990 - Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08855-1331)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Block diagram. The block diagram shall be as specified on figure 4.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figures 5a – 5kk.

3.2.5 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. These devices shall be compliant to IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage (except PCI)	V_{OH}	DV_{DD} = MIN, I_{OH} = MAX	1, 2, 3	All	2.4		V
High level output voltage (PCI)	V_{OHP}	DV_{DD} = 3.3 V, I_{OHP} = -0.5 mA	1, 2, 3	All	$0.9DV_{DD}$ 3/		V
Low level output voltage (except PCI)	V_{OL}	DV_{DD} = MIN, I_{OL} = MAX	1, 2, 3	All		0.4	V
Low level output voltage (PCI)	V_{OLP}	DV_{DD} = 3.3 V, I_{OLP} = 1.5 mA	1, 2, 3	All		$0.1DV_{DD}$ 3/	V
Input current (except PCI)	I_I	$V_I = V_{SS}$ to DV_{DD}, no opposing internal resistor	1, 2, 3	All		±10	µA
		$V_I = V_{SS}$ to DV_{DD}, opposing internal pullup resistor 4/			50	150	
		$V_I = V_{SS}$ to DV_{DD}, opposing internal pulldown resistor 4/			-150	-50	
Input leakage current (PCI)	I_{IP} 5/	$0 < V_{IP} < DV_{DD}$ = 3.3 V	1, 2, 3	All		±10	µA
High level output current	I_{OH}	EMIF, CLKOUT4, CLKOUT6, EMUx	1, 2, 3	All		–16	mA
		Timer, UTOPIA, TDO, GPIO (excluding GP[15:9, 2, 1]), McBSP				-8	
		PCI/HPI				-0.5 3/	
Low level output current	I_{OL}	EMIF, CLKOUT4, CLKOUT6, EMUx	1, 2, 3	All		16	mA
		Timer, UTOPIA, TDO, GPIO (excluding GP[15:9, 2, 1]), McBSP				8	
		PCI/HPI				1.5 3/	
Off-state output current	I_{OZ}	$V_O = DV_{DD}$ or 0 V	1, 2, 3	All		±10	µA
Core supply current	I_{CDD} 6/	CV_{DD} = 1.4 V, CPU clock = 600 MHz	1, 2, 3	All	750 TYP 7/		mA
I/O supply current	I_{DDD} 6/	DV_{DD} = 3.3 V, CPU clock = 600 MHz	1, 2, 3	All	125 TYP 7/		mA
Input capacitance	C_{IN}	See 4.4.1b	4	All		12	pF
Output capacitance	C_{OUT}	See 4.4.1b	4	All		12	pF
Functional tests		See 4.4.1c	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKIN Timing Requirements 9/ 10/							
Cycle time, CLKIN	$t_{c(CLKIN)}$	PLL Mode x12 See ref. 1, figure 5b.	9, 10, 11	All	20	33.3	ns
		PLL Mode x6 See ref. 1, figure 5b.			13.3	33.3	
		x1 (Bypass) See ref. 1, figure 5b.			13.3 7/	33.3	
Pulse duration, CLKIN high	$t_{w(CLKINH)}$	PLL Mode x12 See ref. 2, figure 5b.	9, 10, 11	All	0.4C 7/		ns
		PLL Mode x6 See ref. 2, figure 5b.			0.4C 7/		
		x1 (Bypass) See ref. 2, figure 5b.			0.45C 7/		
Pulse duration, CLKIN low	$t_{w(CLKINL)}$	PLL Mode x12 See ref. 3, figure 5b.	9, 10, 11	All	0.4C 7/		ns
		PLL Mode x6 See ref. 3, figure 5b.			0.4C 7/		
		x1 (Bypass) See ref. 3, figure 5b.			0.45C 7/		
Transition time, CLKIN	$t_{t(CLKIN)}$	PLL Mode x12 See ref. 4, figure 5b.	9, 10, 11	All		5 7/	ns
		PLL Mode x6 See ref. 4, figure 5b.				5 7/	
		x1 (Bypass) See ref. 4, figure 5b.				1 7/	
CLKOUT4 Switching Characteristics 11/ 12/ 13/							
Period jitter, CLKOUT4	$t_{J(CKO4)}$	CLKMODE = x1, x6, x12 See ref. 1, figure 5c.	9, 10, 11	All	0 7/	±175 7/	ps
Pulse duration, CLKOUT4 high	$t_{w(CKO4H)}$	CLKMODE = x1, x6, x12 See ref. 2, figure 5c.	9, 10, 11	All	2P – 0.7 7/	2P + 0.7 7/	ns
Pulse duration, CLKOUT4 low	$t_{w(CKO4L)}$	CLKMODE = x1, x6, x12 See ref. 3, figure 5c.	9, 10, 11	All	2P – 0.7 7/	2P + 0.7 7/	ns
Transition time, CLKOUT4	$t_{t(CKO4)}$	CLKMODE = x1, x6, x12 See ref. 4, figure 5c.	9, 10, 11	All		1 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKOUT6 Switching Characteristics 11/ 12/ 13/							
Period jitter, CLKOUT6	$t_{J(CKO6)}$	CLKMODE = x1, x6, x12 See ref. 1, figure 5d.	9, 10, 11	All	0 7/	±175 7/	ps
Pulse duration, CLKOUT6 high	$t_{w(CKO6H)}$	CLKMODE = x1, x6, x12 See ref. 2, figure 5d.	9, 10, 11	All	3P – 0.7 7/	3P + 0.7 7/	ns
Pulse duration, CLKOUT6 low	$t_{w(CKO6L)}$	CLKMODE = x1, x6, x12 See ref. 3, figure 5d.	9, 10, 11	All	3P – 0.7 7/	3P + 0.7 7/	ns
Transition time, CLKOUT6	$t_{t(CKO6)}$	CLKMODE = x1, x6, x12 See ref. 4, figure 5d.	9, 10, 11	All		1 7/	ns
ECLKIN for EMIFA and EMIFB Timing Requirements 9/ 13/ 14/							
Cycle time, ECLKIN	$t_{c(EKI)}$	See ref. 1, figure 5e.	9, 10, 11	All	6 7/ 15/	16P 7/	ns
Pulse duration, ECLKIN high	$t_{w(EKIH)}$	See ref. 2, figure 5e.	9, 10, 11	All	2.7 7/		ns
Pulse duration, ECLKIN low	$t_{w(EKIL)}$	See ref. 3, figure 5e.	9, 10, 11	All	2.7 7/		ns
Transition time, ECLKIN	$t_{t(EKI)}$	See ref. 4, figure 5e.	9, 10, 11	All		2 7/	ns
ECLKOUT1 for EMIFA and EMIFB Modules Switching characteristics 11/ 14/ 16/ 17/							
Period jitter, ECLKOUT1	$t_{J(EKO1)}$	See ref. 1, figure 5f.	9, 10, 11	All	0 7/	±175 7/ 18/	ps
Pulse duration, ECLKOUT1 high	$t_{w(EKO1H)}$	See ref. 2, figure 5f.	9, 10, 11	All	EH – 0.7 7/	EH + 0.7 7/	ns
Pulse duration, ECLKOUT1 low	$t_{w(EKO1L)}$	See ref. 3, figure 5f.	9, 10, 11	All	EL – 0.7 7/	EL + 0.7 7/	ns
Transition time, ECLKOUT1	$t_{t(EKO1)}$	See ref. 4, figure 5f.	9, 10, 11	All		1 7/	ns
Delay time, ECLKIN high to ECLKOUT1 high	$t_{d(EKIH-EKO1H)}$	See ref. 5, figure 5f.	9, 10, 11	All	1 7/	8 7/	ns
Delay time, ECLKIN low to ECLKOUT1 low	$t_{d(EKIL-EKO1L)}$	See ref. 6, figure 5f.	9, 10, 11	All	1 7/	8 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ECLKOUT2 for EMIFA and EMIFB Modules Switching characteristics 11/ 14/ 19/							
Period jitter, ECLKOUT2	$t_{J(EKO2)}$	See ref. 1, figure 5g.	9, 10, 11	All	0 7/	±175 7/ 18/	ps
Pulse duration, ECLKOUT2 high	$t_{w(EKO2H)}$	See ref. 2, figure 5g.	9, 10, 11	All	0.5NE – 0.7 7/	0.5NE + 0.7 7/	ns
Pulse duration, ECLKOUT2 low	$t_{w(EKO2L)}$	See ref. 3, figure 5g.	9, 10, 11	All	0.5NE – 0.7 7/	0.5NE + 0.7 7/	ns
Transition time, ECLKOUT2	$t_{t(EKO2)}$	See ref. 4, figure 5g.	9, 10, 11	All		1 7/	ns
Delay time, ECLKIN high to ECLKOUT2 high	$t_{d(EKIH-EKO2H)}$	See ref. 5, figure 5g.	9, 10, 11	All	1 7/	8 7/	ns
Delay time, ECLKIN low to ECLKOUT2 low	$t_{d(EKIL-EKO2L)}$	See ref. 6, figure 5g.	9, 10, 11	All	1 7/	8 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous Memory Cycles for EMIFA Module Timing Requirements 20/ 21/ 22/							
Setup time, EDx valid before $\overline{ARE}$ high	$t_{su(EDV-AREH)}$	See ref. 3, figure 5h.	9, 10, 11	All	6.5		ns
Hold time, EDx valid after $\overline{ARE}$ high	$t_{h(AREH-EDV)}$	See ref. 4, figure 5h.	9, 10, 11	All	1		ns
Setup time, ARDY valid before ECLKOUT1 high	$t_{su(ARDY-EKO1H)}$	See ref. 6, figure 5h.	9, 10, 11	All	3		ns
Hold time, ARDY valid after ECLKOUT1 high	$t_{h(EKO1H-ARDY)}$	See ref. 7, figure 5h.	9, 10, 11	All	1		ns
Asynchronous Memory Cycles for EMIFA Module Switching characteristics 21/ 22/ 23/ 24/							
Output setup time, select signals valid to $\overline{ARE}$ low	$t_{osu(SELV-AREL)}$	See ref. 1, figure 5h.	9, 10, 11	All	RS*E – 2.0		ns
Output hold time, $\overline{ARE}$ high to select signals invalid	$t_{oh(AREH-SELIV)}$	See ref. 2, figure 5h.	9, 10, 11	All	RH*E – 1.9		ns
Delay time, ECLKOUT1 high to $\overline{ARE}$ valid	$t_{d(EKO1H-AREV)}$	See ref. 5, figure 5h.	9, 10, 11	All	1	7	ns
Output setup time, select signals valid to $\overline{AWE}$ low	$t_{osu(SELV-AWEL)}$	See ref. 8, figure 5h.	9, 10, 11	All	WS*E – 1.7		ns
Output hold time, $\overline{AWE}$ high to select signals invalid	$t_{oh(AWEH-SELIV)}$	See ref. 9, figure 5h.	9, 10, 11	All	WH*E – 1.8		ns
Delay time, ECLKOUT1 high to $\overline{AWE}$ valid	$t_{d(EKO1H-AWEV)}$	See ref. 10, figure 5h.	9, 10, 11	All	1.3	7.1	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous Memory Cycles for EMIFB Module Timing Requirements 20/ 21/ 22/							
Setup time, EDx valid before $\overline{ARE}$ high	$t_{su(EDV-AREH)}$	See ref. 3, figure 5h.	9, 10, 11	All	6.2		ns
Hold time, EDx valid after $\overline{ARE}$ high	$t_{h(AREH-EDV)}$	See ref. 4, figure 5h.	9, 10, 11	All	1		ns
Setup time, ARDY valid before ECLKOUT1 high	$t_{su(ARDY-EKO1H)}$	See ref. 6, figure 5h.	9, 10, 11	All	3		ns
Hold time, ARDY valid after ECLKOUT1 high	$t_{h(EKO1H-ARDY)}$	See ref. 7, figure 5h.	9, 10, 11	All	1.2		ns
Asynchronous Memory Cycles for EMIFB Module Switching characteristics 21/ 22/ 23/ 24/							
Output setup time, select signals valid to $\overline{ARE}$ low	$t_{osu(SELV-AREL)}$	See ref. 1, figure 5h.	9, 10, 11	All	RS*E – 2.0		ns
Output hold time, $\overline{ARE}$ high to select signals invalid	$t_{oh(AREH-SELIV)}$	See ref. 2, figure 5h.	9, 10, 11	All	RH*E – 1.7		ns
Delay time, ECLKOUT1 high to $\overline{ARE}$ valid	$t_{d(EKO1H-AREV)}$	See ref. 5, figure 5h.	9, 10, 11	All	0.8	6.6	ns
Output setup time, select signals valid to $\overline{AWE}$ low	$t_{osu(SELV-AWEL)}$	See ref. 8, figure 5h.	9, 10, 11	All	WS*E – 1.9		ns
Output hold time, $\overline{AWE}$ high to select signals invalid	$t_{oh(AWEH-SELIV)}$	See ref. 9, figure 5h.	9, 10, 11	All	WH*E – 1.7		ns
Delay time, ECLKOUT1 high to $\overline{AWE}$ valid	$t_{d(EKO1H-AWEV)}$	See ref. 10, figure 5h.	9, 10, 11	All	0.9	6.7	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Programmable Synchronous Interface Cycles for EMIFA Module Timing Requirements 25/							
Setup time, read EDx valid before ECLKOUTx high	$t_{su(EDV-EKOxH)}$	See ref. 6, figure 5j.	9, 10, 11	All	2		ns
Hold time, read EDx valid after ECLKOUTx high	$t_{h(EKOxH-EDV)}$	See ref. 7, figure 5j.	9, 10, 11	All	1.5		ns
Programmable Synchronous Interface Cycles for EMIFA Module Switching Characteristics 25/ 26/							
Delay time, ECLKOUTx high to $\overline{CE}$x valid	$t_{d(EKOxH-CEV)}$	See ref. 1, figure 5j.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUTx high to $\overline{BE}$x valid	$t_{d(EKOxH-BEV)}$	See ref. 2, figure 5j.	9, 10, 11	All		5.1	ns
Delay time, ECLKOUTx high to $\overline{BE}$x invalid	$t_{d(EKOxH-BEIV)}$	See ref. 3, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to EAx valid	$t_{d(EKOxH-EAV)}$	See ref. 4, figure 5j.	9, 10, 11	All		4.9	ns
Delay time, ECLKOUTx high to EAx invalid	$t_{d(EKOxH-EAIV)}$	See ref. 5, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to $\overline{SADS}$/$\overline{SRE}$ valid	$t_{d(EKOxH-ADSV)}$	See ref. 8, figure 5j.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUTx high to $\overline{SOE}$ valid	$t_{d(EKOxH-OEV)}$	See ref. 9, figure 5j.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUTx high to $\overline{ED}$x valid	$t_{d(EKOxH-EDV)}$	See ref. 10, figure 5j.	9, 10, 11	All		4.9	ns
Delay time, ECLKOUTx high to $\overline{ED}$x invalid	$t_{d(EKOxH-EDIV)}$	See ref. 11, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to $\overline{SWE}$ valid	$t_{d(EKOxH-WEV)}$	See ref. 12, figure 5j.	9, 10, 11	All	1.3	4.9	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Programmable Synchronous Interface Cycles for EMIFB Module Timing Requirements 25/							
Setup time, read EDx valid before ECLKOUTx high	$t_{su(EDV-EKOxH)}$	See ref. 6, figure 5j.	9, 10, 11	All	3.1		ns
Hold time, read EDx valid after ECLKOUTx high	$t_{h(EKOxH-EDV)}$	See ref. 7, figure 5j.	9, 10, 11	All	1.5		ns
Programmable Synchronous Interface Cycles for EMIFB Module Switching Characteristics 25/ 26/							
Delay time, ECLKOUTx high to $\overline{CE}$x valid	$t_{d(EKOxH-CEV)}$	See ref. 1, figure 5j.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUTx high to $\overline{BE}$x valid	$t_{d(EKOxH-BEV)}$	See ref. 2, figure 5j.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUTx high to $\overline{BE}$x invalid	$t_{d(EKOxH-BEIV)}$	See ref. 3, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to EAx valid	$t_{d(EKOxH-EAV)}$	See ref. 4, figure 5j.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUTx high to EAx invalid	$t_{d(EKOxH-EAIV)}$	See ref. 5, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to $\overline{SADS}$/$\overline{SRE}$ valid	$t_{d(EKOxH-ADSV)}$	See ref. 8, figure 5j.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUTx high to $\overline{SOE}$ valid	$t_{d(EKOxH-OEV)}$	See ref. 9, figure 5j.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUTx high to $\overline{ED}$x valid	$t_{d(EKOxH-EDV)}$	See ref. 10, figure 5j.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUTx high to $\overline{ED}$x invalid	$t_{d(EKOxH-EDIV)}$	See ref. 11, figure 5j.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUTx high to $\overline{SWE}$ valid	$t_{d(EKOxH-WEV)}$	See ref. 12, figure 5j.	9, 10, 11	All	1.3	6.4	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Synchronous DRAM Cycles for EMIFA Module Timing Requirements 27/							
Setup time, read EDx valid before ECLKOUT1 high	$t_{su(EDV-EKO1H)}$	See ref. 6, figure 5k.	9, 10, 11	All	0.6		ns
Hold time, read EDx valid after ECLKOUT1 high	$t_{h(EKO1H-EDV)}$	See ref. 7, figure 5k.	9, 10, 11	All	1.8		ns
Synchronous DRAM Cycles for EMIFA Module Switching Characteristics 27/							
Delay time, ECLKOUT1 high to $\overline{CE}$x valid	$t_{d(EKO1H-CEV)}$	See ref. 1, figure 5k.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUT1 high to $\overline{BE}$x valid	$t_{d(EKO1H-BEV)}$	See ref. 2, figure 5k.	9, 10, 11	All		4.9	ns
Delay time, ECLKOUT1 high to $\overline{BE}$x invalid	$t_{d(EKO1H-BEIV)}$	See ref. 3, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to EAx valid	$t_{d(EKO1H-EAV)}$	See ref. 4, figure 5k.	9, 10, 11	All		4.9	ns
Delay time, ECLKOUT1 high to EAx invalid	$t_{d(EKO1H-EAIV)}$	See ref. 5, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to $\overline{SDCAS}$ valid	$t_{d(EKO1H-CASV)}$	See ref. 8, figure 5k.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUT1 high to $\overline{ED}$x valid	$t_{d(EKO1H-EDV)}$	See ref. 9, figure 5k.	9, 10, 11	All		4.9	ns
Delay time, ECLKOUT1 high to $\overline{ED}$x invalid	$t_{d(EKO1H-EDIV)}$	See ref. 10, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to $\overline{SDWE}$ valid	$t_{d(EKO1H-WEV)}$	See ref. 11, figure 5k.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUT1 high to $\overline{SDRAS}$ valid	$t_{d(EKO1H-RAS)}$	See ref. 12, figure 5k.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUT1 high to ASDCKE valid (EMIFA only)	$t_{d(EKO1H-ACKEV)}$	See ref. 13, figure 5k.	9, 10, 11	All	1.3	4.9	ns
Delay time, ECLKOUT1 high to $\overline{PDT}$ valid	$t_{d(EKO1H-PDTV)}$	See ref. 14, figure 5k.	9, 10, 11	All	1.3	4.9	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Synchronous DRAM Cycles for EMIFB Module Timing Requirements 27/							
Setup time, read EDx valid before ECLKOUT1 high	$t_{su(EDV-EKO1H)}$	See ref. 6, figure 5k.	9, 10, 11	All	2.1		ns
Hold time, read EDx valid after ECLKOUT1 high	$t_{h(EKO1H-EDV)}$	See ref. 7, figure 5k.	9, 10, 11	All	2.5		ns
Synchronous DRAM Cycles for EMIFB Module Switching Characteristics 27/							
Delay time, ECLKOUT1 high to $\overline{CE}$x valid	$t_{d(EKO1H-CEV)}$	See ref. 1, figure 5k.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUT1 high to $\overline{BE}$x valid	$t_{d(EKO1H-BEV)}$	See ref. 2, figure 5k.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUT1 high to $\overline{BE}$x invalid	$t_{d(EKO1H-BEIV)}$	See ref. 3, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to EAx valid	$t_{d(EKO1H-EAV)}$	See ref. 4, figure 5k.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUT1 high to EAx invalid	$t_{d(EKO1H-EAIV)}$	See ref. 5, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to $\overline{SDCAS}$ valid	$t_{d(EKO1H-CASV)}$	See ref. 8, figure 5k.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUT1 high to $\overline{ED}$x valid	$t_{d(EKO1H-EDV)}$	See ref. 9, figure 5k.	9, 10, 11	All		6.4	ns
Delay time, ECLKOUT1 high to $\overline{ED}$x invalid	$t_{d(EKO1H-EDIV)}$	See ref. 10, figure 5k.	9, 10, 11	All	1.3		ns
Delay time, ECLKOUT1 high to $\overline{SDWE}$ valid	$t_{d(EKO1H-WEV)}$	See ref. 11, figure 5k.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUT1 high to $\overline{SDRAS}$ valid	$t_{d(EKO1H-RAS)}$	See ref. 12, figure 5k.	9, 10, 11	All	1.3	6.4	ns
Delay time, ECLKOUT1 high to ASDCKE valid (EMIFA only)	$t_{d(EKO1H-ACKEV)}$	See ref. 13, figure 5k.	9, 10, 11	All	1.3 7/	6.4 7/	ns
Delay time, ECLKOUT1 high to $\overline{PDT}$ valid	$t_{d(EKO1H-PDTV)}$	See ref. 14, figure 5k.	9, 10, 11	All	1.3	6.4	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ Cycles for EMIFA and EMIFB Modules Timing Requirements 16/							
Hold time, $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low	$t_{oh(HOLDAL-HOLDL)}$	See ref. 3, figure 5m.	9, 10, 11	All	E 7/		ns
$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ Cycles for EMIFA and EMIFB Modules Switching Characteristics 16/ 28/ 29/							
Delay time, $\overline{\text{HOLD}}$ low to EMIF Bus high impedance	$t_{d(HOLDL-EMHZ)}$	See ref. 1, figure 5m.	9, 10, 11	All	2E 7/	30/ 7/	ns
Delay time, EMIF Bus high impedance to $\overline{\text{HOLDA}}$ low	$t_{d(EMHZ-HOLDAL)}$	See ref. 2, figure 5m.	9, 10, 11	All	0 7/	2E 7/	ns
Delay time, $\overline{\text{HOLD}}$ high to EMIF Bus low impedance	$t_{d(HOLDH-EMLZ)}$	See ref. 4, figure 5m.	9, 10, 11	All	2E 7/	7E 7/	ns
Delay time, EMIF Bus low impedance to $\overline{\text{HOLDA}}$ high	$t_{d(EMLZ-HOLDAH)}$	See ref. 5, figure 5m.	9, 10, 11	All	0 7/	2E 7/	ns
Delay time, $\overline{\text{HOLD}}$ low to ECLKOUTx high impedance	$t_{d(HOLDL-EKOHZ)}$	See ref. 6, figure 5m.	9, 10, 11	All	2E 7/	30/ 7/	ns
Delay time, $\overline{\text{HOLD}}$ high to ECLKOUTx low impedance	$t_{d(HOLDH-EKOLZ)}$	See ref. 7, figure 5m.	9, 10, 11	All	2E 7/	7E 7/	ns
BUSREQ Cycles for EMIFA and EMIFB Modules Switching Characteristics							
Delay time, AECLKOUT1 high to ABUSREQ valid	$t_{d(AEKO1H-ABUSRV)}$	See ref. 1, figure 5n.	9, 10, 11	All	1	5.5	ns
Delay time, BECLKOUT1 high to BBUSREQ valid	$t_{d(BEKO1H-BBUSRV)}$	See ref. 2, figure 5n.	9, 10, 11	All	0.9	5.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET Timing Requirements 13/							
Width of the $\overline{\text{RESET}}$ pulse (PLL stable) 31/	$t_{w(RST)}$	See ref. 1, figure 5p.	9, 10, 11	All	10P 7/		ns
Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) 32/					250 7/		µs
Setup time, boot configuration bits valid before $\overline{\text{RESET}}$ high	$t_{su(boot)}$ 33/	See ref. 16, figure 5p.	9, 10, 11	All	4P 7/		ns
Hold time, boot configuration bits valid after $\overline{\text{RESET}}$ high	$t_{h(boot)}$ 33/	See ref. 17, figure 5p.	9, 10, 11	All	4P 7/		ns
RESET Switching characteristics 13/ 16/ 34/							
Delay time, $\overline{\text{RESET}}$ low to ECLKIN synchronized internally	$t_{d(RSTL-ECKI)}$	See ref. 2, figure 5p.	9, 10, 11	All	2E 7/	3P + 20E 7/	ns
Delay time, $\overline{\text{RESET}}$ high to ECLKIN synchronized internally	$t_{d(RSTH-ECKI)}$	See ref. 3, figure 5p.	9, 10, 11	All	2E 7/	8P + 20E 7/	ns
Delay time, $\overline{\text{RESET}}$ low to ECLKOUT1 high impedance	$t_{d(RSTL-ECKO1HZ)}$	See ref. 4, figure 5p.	9, 10, 11	All	2E 7/		ns
Delay time, $\overline{\text{RESET}}$ high to ECLKOUT1 valid	$t_{d(RSTH-ECKO1V)}$	See ref. 5, figure 5p.	9, 10, 11	All		8P + 20E 7/	ns
Delay time, $\overline{\text{RESET}}$ low to EMIF Z high impedance	$t_{d(RSTL-EMIFZHZ)}$	See ref. 6, figure 5p.	9, 10, 11	All	2E 7/	3P + 4E 7/	ns
Delay time, $\overline{\text{RESET}}$ high to EMIF Z valid	$t_{d(RSTH-EMIFZV)}$	See ref. 7, figure 5p.	9, 10, 11	All	16E 7/	8P + 20E 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET Switching characteristics - Continued 13/ 16/ 34/							
Delay time, $\overline{\text{RESET}}$ low to EMIF high group invalid	$t_{d(RSTL-EMIFHIV)}$	See ref. 8, figure 5p.	9, 10, 11	All	2E 7/		ns
Delay time, $\overline{\text{RESET}}$ high to EMIF high group valid	$t_{d(RSTH-EMIFHV)}$	See ref. 9, figure 5p.	9, 10, 11	All		8P + 20E 7/	ns
Delay time, $\overline{\text{RESET}}$ low to EMIF low group invalid	$t_{d(RSTL-EMIFLIV)}$	See ref. 10, figure 5p.	9, 10, 11	All	2E 7/		ns
Delay time, $\overline{\text{RESET}}$ high to EMIF low group valid	$t_{d(RSTH-EMIFLV)}$	See ref. 11, figure 5p.	9, 10, 11	All		8P + 20E 7/	ns
Delay time, $\overline{\text{RESET}}$ low to low group invalid	$t_{d(RSTL-LOWIV)}$	See ref. 12, figure 5p.	9, 10, 11	All	0 7/		ns
Delay time, $\overline{\text{RESET}}$ high to low group valid	$t_{d(RSTH-LOWV)}$	See ref. 13, figure 5p.	9, 10, 11	All		11P 7/	ns
Delay time, $\overline{\text{RESET}}$ low to Z group high impedance	$t_{d(RSTL-ZHZ)}$	See ref. 14, figure 5p.	9, 10, 11	All	0 7/		ns
Delay time, $\overline{\text{RESET}}$ high to Z group valid	$t_{d(RSTH-ZV)}$	See ref. 15, figure 5p.	9, 10, 11	All	2P 7/	8P 7/	ns
External Interrupts Timing Requirements 13/							
Width of the NMI interrupt pulse low	$t_{w(ILOW)}$	See ref. 1, figure 5q.	9, 10, 11	All	4P 7/		ns
Width of the EXT_INT interrupt pulse low					8P 7/		
Width of the NMI interrupt pulse high	$t_{w(IHIGH)}$	See ref. 2, figure 5q.	9, 10, 11	All	4P 7/		ns
Width of the EXT_INT interrupt pulse high					8P 7/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Host-Port Interface (HPI) Cycles Timing Requirements 13/ 35/							
Setup time, select signals valid before HSTROBE low 36/	$t_{su(SELV-HSTBL)}$	See ref. 1, figure 5r.	9, 10, 11	All	5		ns
Hold time, select signals valid after HSTROBE low 36/	$t_{h(HSTBL-SELV)}$	See ref. 2, figure 5r.	9, 10, 11	All	2.4		ns
Pulse duration, HSTROBE low	$t_{w(HSTBL)}$	See ref. 3, figure 5r.	9, 10, 11	All	4P 7/ 37/		ns
Pulse duration, HSTROBE high between consecutive accesses	$t_{w(HSTBH)}$	See ref. 4, figure 5r.	9, 10, 11	All	4P 7/		ns
Setup time, select signals valid before HAS low 36/	$t_{su(SELV-HASL)}$	See ref. 10, figure 5r.	9, 10, 11	All	5		ns
Hold time, select signals valid after HAS low 36/	$t_{h(HASL-SELV)}$	See ref. 11, figure 5r.	9, 10, 11	All	2		ns
Setup time, host data valid before HSTROBE high 36/	$t_{su(HDV-HSTBH)}$	See ref. 12, figure 5r.	9, 10, 11	All	5		ns
Hold time, host data valid after HSTROBE high 36/	$t_{h(HSTBH-HDV)}$	See ref. 13, figure 5r.	9, 10, 11	All	2.8		ns
Hold time, HSTROBE low after HRDY low 38/	$t_{h(HRDYL-HSTBL)}$	See ref. 14, figure 5r.	9, 10, 11	All	2 7/		ns
Setup time, HAS low before HSTROBE low	$t_{su(HASL-HSTBL)}$	See ref. 18, figure 5r.	9, 10, 11	All	2		ns
Hold time, HAS low after HSTROBE low	$t_{h(HSTBL-HASL)}$	See ref. 19, figure 5r.	9, 10, 11	All	2.1		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Host-Port Interface (HPI) Cycles Switching Characteristics 13/ 35/							
Delay time, HSTROBE low to HRDY high 39/	$t_{d(HSTBL-HRDYH)}$	See ref. 6, figure 5r.	9, 10, 11	All	1.3	4P + 8	ns
Delay time, HSTROBE low to HD low impedance for an HPI read	$t_{d(HSTBL-HDLZ)}$	See ref. 7, figure 5r.	9, 10, 11	All	2 7/		ns
Delay time, HD valid to HRDY low	$t_{d(HDV-HRDYL)}$	See ref. 8, figure 5r.	9, 10, 11	All	-3		ns
Output hold time, HD valid after HSTROBE high	$t_{oh(HSTBH-HDV)}$	See ref. 9, figure 5r.	9, 10, 11	All	1.5		ns
Delay time, HSTROBE high to HD high impedance	$t_{oh(HSTBH-HDHZ)}$	See ref. 15, figure 5r.	9, 10, 11	All		12 7/	ns
Delay time, HSTROBE low to HD valid (HPI16 only)	$t_{oh(HSTBL-HDV)}$	See ref. 16, figure 5r.	9, 10, 11	All		4P + 8	ns
PCLK Timing Requirements 13/ 40/							
Cycle time, PCLK	$t_{c(PCLK)}$	See ref. 1, figure 5t.	9, 10, 11	All	30 (or 8P) 7/ 41/		ns
Pulse duration, PCLK high	$t_{w(PCLKH)}$	See ref. 2, figure 5t.	9, 10, 11	All	11 7/		ns
Pulse duration, PCLK low	$t_{w(PCLKL)}$	See ref. 3, figure 5t.	9, 10, 11	All	11 7/		ns
Δv/Δt slew rate, PCLK	$t_{sr(PCLK)}$	See ref. 4, figure 5t.	9, 10, 11	All	1 7/	4 7/	V/ns
PCI Reset ($\overline{PRST}$) Timing Requirements							
Pulse duration, $\overline{PRST}$	$t_{w(PRST)}$	See ref. 1, figure 5u.	9, 10, 11	All	1 7/		ms
Setup time, PCLK active before $\overline{PRST}$ high	$t_{w(PCLKA-PRSTH)}$	See ref. 2, figure 5u.	9, 10, 11	All	100 7/		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PCI Inputs Timing Requirements							
Setup time, input valid before PCLK high	$t_{su(IV-PCLKH)}$	See ref. 5, figure 5v.	9, 10, 11	All	7		ns
Hold time, input valid after PCLK high	$t_{h(IV-PCLKH)}$	See ref. 6, figure 5v.	9, 10, 11	All	0		ns
PCI Outputs Switching Characteristics							
Delay time, PCLK high to output valid	$t_{d(PCLKH-OV)}$	See ref. 1, figure 5v.	9, 10, 11	All		11	ns
Delay time, PCLK high to output invalid	$t_{d(PCLKH-OIV)}$	See ref. 2, figure 5v.	9, 10, 11	All	2		ns
Delay time, PCLK high to output low impedance	$t_{d(PCLKH-OLZ)}$	See ref. 3, figure 5v.	9, 10, 11	All	2 7/		ns
Delay time, PCLK high to output high impedance	$t_{d(PCLKH-OHZ)}$	See ref. 4, figure 5v.	9, 10, 11	All		28 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial EEPROM Interface Timing Requirements							
Setup time, XSP_DI valid before XSP_CLK high	$t_{su(DIV-CLKH)}$	See ref. 8, figure 5w.	9, 10, 11	All	50 7/		ns
Hold time, XSP_DI valid after XSP_CLK high	$t_{h(CLKH-DIV)}$	See ref. 9, figure 5w.	9, 10, 11	All	0 7/		ns
Serial EEPROM Interface Switching characteristics 13/							
Pulse duration, XSP_CS low	$t_{w(CSL)}$	See ref. 1, figure 5w.	9, 10, 11	All	4092P TYP		ns
Delay time, XSP_CLK low to XSP_CS low	$t_{d(CLKL-CSL)}$	See ref. 2, figure 5w.	9, 10, 11	All	0 TYP		ns
Delay time, XSP_CS high to XSP_CLK high	$t_{d(CSH-CLKH)}$	See ref. 3, figure 5w.	9, 10, 11	All	2046P TYP		ns
Pulse duration, XSP_CLK high	$t_{w(CLKH)}$	See ref. 4, figure 5w.	9, 10, 11	All	2046P TYP		ns
Pulse duration, XSP_CLK low	$t_{w(CLKL)}$	See ref. 5, figure 5w.	9, 10, 11	All	2046P TYP		ns
Output setup time, XSP_DO valid after XSP_CLK high	$t_{osu(DOV-CLKH)}$	See ref. 6, figure 5w.	9, 10, 11	All	2046P TYP		ns
Output hold time, XSP_DO valid after XSP_CLK high	$t_{oh(CLKH-DOV)}$	See ref. 7, figure 5w.	9, 10, 11	All	2046P TYP		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP Timing Requirements 13/ 42/							
Cycle time, CLKR/X	$t_{c(CKRX)}$	CLKR/X ext See ref. 2, figure 5x.	9, 10, 11	All	6.67 7/ 43/		ns
Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$	CLKR/X ext See ref. 3, figure 5x.	9, 10, 11	All	$0.5t_{c(CKRX)}$ -1 7/ 44/		ns
Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$	CLKR int See ref. 5, figure 5x.	9, 10, 11	All	9		ns
		CLKR ext See ref. 5, figure 5x.			1.3		
Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$	CLKR int See ref. 6, figure 5x.	9, 10, 11	All	6		ns
		CLKR ext See ref. 6, figure 5x.			3		
Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$	CLKR int See ref. 7, figure 5x.	9, 10, 11	All	8		ns
		CLKR ext See ref. 7, figure 5x.			0.9		
Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$	CLKR int See ref. 8, figure 5x.	9, 10, 11	All	3		ns
		CLKR ext See ref. 8, figure 5x.			3.1		
Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$	CLKR int See ref. 10, figure 5x.	9, 10, 11	All	9		ns
		CLKR ext See ref. 10, figure 5x.			1.3		
Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$	CLKR int See ref. 11, figure 5x.	9, 10, 11	All	6		ns
		CLKR ext See ref. 11, figure 5x.			3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP Switching Characteristics 42/ 45/							
Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRXH)}$	See ref. 1, figure 5x.	9, 10, 11	All	1.4	10	ns
Cycle time, CLKR/X	$t_{c(CKRX)}$	CLKR/X int See ref. 2, figure 5x.	9, 10, 11	All	6.67 7/ 43/		ns
Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$	CLKR/X int See ref. 3, figure 5x.	9, 10, 11	All	C - 1 7/ 46/	C + 1 7/ 46/	ns
Delay time, CLKR high to Internal FSR valid	$t_{d(CKRH-FRV)}$	CLKR int See ref. 4, figure 5x.	9, 10, 11	All	-2.1	3	ns
Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$	CLKX int See ref. 9, figure 5x.	9, 10, 11	All	-1.7	3	ns
		CLKX ext See ref. 9, figure 5x.			1.7	9	
Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$	CLKX int See ref. 12, figure 5x.	9, 10, 11	All	-3.9 7/	4 7/	ns
		CLKX ext See ref. 12, figure 5x.			-2.1 7/	9 7/	
Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$	CLKX int See ref. 13, figure 5x.	9, 10, 11	All	-3.9 + D1 47/	4 + D2 47/	ns
		CLKX ext See ref. 13, figure 5x.			-2.1 + D1 47/	9 + D2 47/	
Delay time, FSX high to DX valid 48/	$t_{d(FXH-DXV)}$	FSX int See ref. 14, figure 5x.	9, 10, 11	All	-2.3	5.6	ns
		FSX ext See ref. 14, figure 5x.			1.9	9	
FSR When GSYNC = 1 Timing Requirements							
Setup time, FSR high before CLKS high	$t_{su(FRH-CKSH)}$	See ref. 1, figure 5y.	9, 10, 11	All	4 7/		ns
Hold time, FSR high after CLKS high	$t_{h(CKSH-FRH)}$	See ref. 2, figure 5y.	9, 10, 11	All	4 7/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 Timing Requirements 13/ 49/							
Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	Master See ref. 4, figure 5z.	9, 10, 11	All	12		ns
		Slave See ref. 4, figure 5z.			2 – 12P		
Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$	Master See ref. 5, figure 5z.	9, 10, 11	All	4		ns
		Slave See ref. 5, figure 5z.			5 + 24P		
McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 Switching Characteristics 13/ 49/							
Hold time, FSX low after CLKX low 50/	$t_{h(CKXL-FXL)}$	Master 51/ See ref. 1, figure 5z.	9, 10, 11	All	T - 2	T + 3	ns
Delay time, FSX low to CLKX high 52/	$t_{d(FXL-CKXH)}$	Master 51/ See ref. 2, figure 5z.	9, 10, 11	All	L – 2 7/	L + 3 7/	ns
Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$	Master 51/ See ref. 3, figure 5z.	9, 10, 11	All	-2	4	ns
		Slave See ref. 3, figure 5z.			12P + 2.8	20P + 17	
Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$	Master 51/ See ref. 6, figure 5z.	9, 10, 11	All	L – 2 7/	L + 3 7/	ns
Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$	Slave See ref. 7, figure 5z.	9, 10, 11	All	4P + 3 7/	12P + 17 7/	ns
Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$	Slave See ref. 8, figure 5z.	9, 10, 11	All	8P + 1.8	16P + 17	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 Timing Requirements 13/ 49/							
Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	Master See ref. 4, figure 5aa.	9, 10, 11	All	12 7/		ns
		Slave See ref. 4, figure 5aa.			2 – 12P 7/		
Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$	Master See ref. 5, figure 5aa.	9, 10, 11	All	4 7/		ns
		Slave See ref. 5, figure 5aa.			5 + 24P 7/		
McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 Switching Characteristics 13/ 49/							
Hold time, FSX low after CLKX low 50/	$t_{h(CKXL-FXL)}$	Master 51/ See ref. 1, figure 5aa.	9, 10, 11	All	L – 2 7/	L + 3 7/	ns
Delay time, FSX low to CLKX high 52/	$t_{d(FXL-CKXH)}$	Master 51/ See ref. 2, figure 5aa.	9, 10, 11	All	T – 2 7/	T + 3 7/	ns
Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$	Master 51/ See ref. 3, figure 5aa.	9, 10, 11	All	-2 7/	4 7/	ns
		Slave See ref. 3, figure 5aa.			12P + 4 7/	20P + 17 7/	
Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$	Master 51/ See ref. 6, figure 5aa.	9, 10, 11	All	-2 7/	4 7/	ns
		Slave See ref. 6, figure 5aa.			12P + 3 7/	20P + 17 7/	
Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$	Master 51/ See ref. 7, figure 5aa.	9, 10, 11	All	H - 2 7/	H + 4 7/	ns
		Slave See ref. 7, figure 5aa.			8P + 2 7/	16P + 17 7/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 Timing Requirements 13/ 49/							
Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	Master See ref. 4, figure 5bb.	9, 10, 11	All	12 7/		ns
		Slave See ref. 4, figure 5bb.			2 – 12P 7/		
Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$	Master See ref. 5, figure 5bb.	9, 10, 11	All	4 7/		ns
		Slave See ref. 5, figure 5bb.			5 + 24P 7/		
McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 Switching Characteristics 13/ 49/							
Hold time, FSX low after CLKX high 50/	$t_{h(CKXH-FXL)}$	Master 51/ See ref. 1, figure 5bb.	9, 10, 11	All	T – 2 7/	T + 3 7/	ns
Delay time, FSX low to CLKX low 52/	$t_{d(FXL-CKXL)}$	Master 51/ See ref. 2, figure 5bb.	9, 10, 11	All	H – 2 7/	H + 3 7/	ns
Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$	Master 51/ See ref. 3, figure 5bb.	9, 10, 11	All	-2 7/	4 7/	ns
		Slave See ref. 3, figure 5bb.			12P + 4 7/	20P + 17 7/	
Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$	Master 51/ See ref. 6, figure 5bb.	9, 10, 11	All	H - 2 7/	H + 3 7/	ns
Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$	Slave See ref. 7, figure 5bb.	9, 10, 11	All	4P + 3 7/	12P + 17 7/	ns
Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$	Slave See ref. 8, figure 5bb.	9, 10, 11	All	8P + 2 7/	16P + 17 7/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 Timing Requirements 13/ 49/							
Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	Master See ref. 4, figure 5cc.	9, 10, 11	All	12 7/		ns
		Slave See ref. 4, figure 5cc.			2 – 12P 7/		
Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$	Master See ref. 5, figure 5cc.	9, 10, 11	All	4 7/		ns
		Slave See ref. 5, figure 5cc.			5 + 24P 7/		
McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 Switching Characteristics 13/ 49/							
Hold time, FSX low after CLKX high 50/	$t_{h(CKXH-FXL)}$	Master 51/ See ref. 1, figure 5cc.	9, 10, 11	All	H – 2 7/	H + 3 7/	ns
Delay time, FSX low to CLKX low 52/	$t_{d(FXL-CKXL)}$	Master 51/ See ref. 2, figure 5cc.	9, 10, 11	All	T – 2 7/	T + 1 7/	ns
Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$	Master 51/ See ref. 3, figure 5cc.	9, 10, 11	All	-2 7/	4 7/	ns
		Slave See ref. 3, figure 5cc.			12P + 4 7/	20P + 17 7/	
Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$	Master 51/ See ref. 6, figure 5cc.	9, 10, 11	All	-2 7/	4 7/	ns
		Slave See ref. 6, figure 5cc.			12P + 3 7/	20P + 17 7/	
Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$	Master 51/ See ref. 7, figure 5cc.	9, 10, 11	All	L - 2 7/	L + 4 7/	ns
		Slave See ref. 7, figure 5cc.			8P + 2 7/	16P + 17 7/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
UXCLK Timing requirements 9/							
Cycle time, UXCLK	$t_{c(UXCK)}$	See ref. 1, figure 5dd.	9, 10, 11	All	20 7/		ns
Pulse duration, UXCLK high	$t_{w(UXCKH)}$	See ref. 2, figure 5dd.	9, 10, 11	All	$0.4t_{c(UXCK)}$ 7/	$0.6t_{c(UXCK)}$ 7/	ns
Pulse duration, UXCLK low	$t_{w(UXCKL)}$	See ref. 3, figure 5dd.	9, 10, 11	All	$0.4t_{c(UXCK)}$ 7/	$0.6t_{c(UXCK)}$ 7/	ns
Transition time, UXCLK	$t_{t(UXCK)}$	See ref. 4, figure 5dd.	9, 10, 11	All		2 7/	ns
URCLK Timing requirements 9/							
Cycle time, URCLK	$t_{c(URCK)}$	See ref. 1, figure 5ee.	9, 10, 11	All	20 7/		ns
Pulse duration, URCLK high	$t_{w(URCKH)}$	See ref. 2, figure 5ee.	9, 10, 11	All	$0.4t_{c(URCK)}$ 7/	$0.6t_{c(URCK)}$ 7/	ns
Pulse duration, URCLK low	$t_{w(URCKL)}$	See ref. 3, figure 5ee.	9, 10, 11	All	$0.4t_{c(URCK)}$ 7/	$0.6t_{c(URCK)}$ 7/	ns
Transition time, URCLK	$t_{t(URCK)}$	See ref. 4, figure 5ee.	9, 10, 11	All		2 7/	ns
UTOPIA Slave Transmit Timing requirements							
Setup time, UXADDR valid before UXCLK high	$t_{su(UXAV-UXCH)}$	See ref. 2, figure 5ff.	9, 10, 11	All	4		ns
Hold time, UXADDR valid after UXCLK high	$t_{h(UXCH-UXAV)}$	See ref. 3, figure 5ff.	9, 10, 11	All	1		ns
Setup time, $\overline{\text{UXENB}}$ low before UXCLK high	$t_{su(UXENBL-UXCH)}$	See ref. 8, figure 5ff.	9, 10, 11	All	4		ns
Hold time, $\overline{\text{UXENB}}$ low after UXCLK high	$t_{h(UXCH-UXENBL)}$	See ref. 9, figure 5ff.	9, 10, 11	All	1		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
UTOPIA Slave Transmit Switching Characteristics							
Delay time, UXCLK high to UXDATA valid	$t_{d(UXCH-UXDV)}$	See ref. 1, figure 5ff.	9, 10, 11	All	3	12	ns
Delay time, UXCLK high to UXCLAV driven active value	$t_{d(UXCH-UXCLAV)}$	See ref. 4, figure 5ff.	9, 10, 11	All	3	12	ns
Delay time, UXCLK high to UXCLAV driven inactive low	$t_{d(UXCH-UXCLAVL)}$	See ref. 5, figure 5ff.	9, 10, 11	All	3 7/	12 7/	ns
Delay time, UXCLK high to UXCLAV going Hi-Z	$t_{d(UXCH-UXCLAVHZ)}$	See ref. 6, figure 5ff.	9, 10, 11	All	9 7/	18.5 7/	ns
Pulse duration (low), UXCLAV low to UXCLAV Hi-Z	$t_{w(UXCLAVL-UXCLAVHZ)}$	See ref. 7, figure 5ff.	9, 10, 11	All	3 7/		ns
Delay time, UXCLK high to UXSOC valid	$t_{d(UXCH-UXSV)}$	See ref. 10, figure 5ff.	9, 10, 11	All	3	12	ns
UTOPIA Slave Receive Timing requirements							
Setup time, URDATA valid before URCLK high	$t_{su(URDV-URCH)}$	See ref. 1, figure 5gg.	9, 10, 11	All	4		ns
Hold time, URDATA valid after URCLK high	$t_{h(URCH-URDV)}$	See ref. 2, figure 5gg.	9, 10, 11	All	1		ns
Setup time, URADDR valid before URCLK high	$t_{su(URAV-URCH)}$	See ref. 3, figure 5gg.	9, 10, 11	All	4		ns
Hold time, URADDR valid after URCLK high	$t_{h(URCH-URAV)}$	See ref. 4, figure 5gg.	9, 10, 11	All	1		ns
Setup time, $\overline{\text{URENB}}$ low before URCLK high	$t_{su(URENBL-URCH)}$	See ref. 9, figure 5gg.	9, 10, 11	All	4		ns
Hold time, $\overline{\text{URENB}}$ low after URCLK high	$t_{h(URCH-URENBL)}$	See ref. 10, figure 5gg.	9, 10, 11	All	1		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
UTOPIA Slave Receive Timing requirements - Continued							
Setup time, URSOC high before URCLK high	$t_{su(URSH-URCH)}$	See ref. 11, figure 5gg.	9, 10, 11	All	4		ns
Hold time, URSOC high after URCLK high	$t_{h(URCH-URSH)}$	See ref. 12, figure 5gg.	9, 10, 11	All	1		ns
UTOPIA Slave Receive Switching Characteristics							
Delay time, URCLK high to URCLAV driven active value	$t_{d(URCH-URCLAV)}$	See ref. 5, figure 5gg.	9, 10, 11	All	3	12	ns
Delay time, URCLK high to URCLAV driven inactive low	$t_{d(URCH-URCLAVL)}$	See ref. 6, figure 5gg.	9, 10, 11	All	3 7/	12 7/	ns
Delay time, URCLK high to URCLAV going Hi-Z	$t_{d(URCH-URCLAVHZ)}$	See ref. 7, figure 5gg.	9, 10, 11	All	9 7/	18.5 7/	ns
Pulse duration (low), URCLAV low to URCLAV Hi-Z	$t_{w(URCLAVL-URCLAVHZ)}$	See ref. 8, figure 5gg.	9, 10, 11	All	3 7/		ns
Timer Inputs Timing Requirements 13/							
Pulse duration, TINP high	$t_{w(TINPH)}$	See ref. 1, figure 5hh.	9, 10, 11	All	8P 7/		ns
Pulse duration, TINP low	$t_{w(TINPL)}$	See ref. 2, figure 5hh.	9, 10, 11	All	8P 7/		ns
Timer Outputs Switching Characteristics 13/							
Pulse duration, TOUT high	$t_{w(TOUTH)}$	See ref. 3, figure 5hh.	9, 10, 11	All	8P - 3 7/		ns
Pulse duration, TOUT low	$t_{w(TOUTL)}$	See ref. 4, figure 5hh.	9, 10, 11	All	8P - 3 7/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 8/ -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
GPIO Inputs Timing Requirements 13/ 53/							
Pulse duration, GPIx high	$t_{w(GPIH)}$	See ref. 1, figure 5jj.	9, 10, 11	All	8P 7/		ns
Pulse duration, GPIx low	$t_{w(GPIL)}$	See ref. 2, figure 5jj.	9, 10, 11	All	8P 7/		ns
GPIO Outputs Switching Characteristics 13/							
Pulse duration, GPOx high	$t_{w(GPOH)}$	See ref. 3, figure 5jj.	9, 10, 11	All	32P 7/		ns
Pulse duration, GPOx low	$t_{w(GPOL)}$	See ref. 4, figure 5jj.	9, 10, 11	All	32P 7/		ns
JTAG Test Port Timing Requirements							
Cycle time, TCK	$t_{c(TCK)}$	See ref. 1, figure 5kk.	9, 10, 11	All	35 7/		ns
Setup time, TDI/TMS/TRST valid before TCK high	$t_{su(TDIV-TCKH)}$	See ref. 3, figure 5kk.	9, 10, 11	All	10 7/		ns
Hold time, TDI/TMS/TRST valid after TCK high	$t_{h(TCKH-TDIV)}$	See ref. 4, figure 5kk.	9, 10, 11	All	9 7/		ns
JTAG Test Port Switching Characteristics							
Delay time, TCK low to TDO valid	$t_{d(TCKL-TDOV)}$	See ref. 2, figure 5kk.	9, 10, 11	All	-3 7/	18 7/	ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics – Continued.

1/ Electrical characteristics over recommended range of supply voltages and operating case temperature, unless otherwise noted.

2/ For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

3/ These rated numbers are from the PCI specification version 2.3.

4/ Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

5/ PCI input leakage currents include Hi-Z output leakage for all bidirectional buffers with 3-state outputs.

6/ Measured with average activity (50% high/50% low power). The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6414/15/16 Power Consumption Summary* application report (literature number SPRA811).

7/ This parameter is not production tested. This parameter is established by design, or is only characterized at initial release and after changes which may affect performance.

8/ See figure 5a herein for input and output voltage reference levels for ac timing measurements and test circuit.

9/ The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

10/ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 50 MHz, use C = 20 ns.

11 The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

12/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

13/ P = 1/CPU clock frequency in nanoseconds (ns). For example, when running parts at 600 MHz, use P = 1.67 ns.

14/ These C64x™ devices have two EMIFs (64-bit EMIFA and 16-bit EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted.

15/ Minimum ECLKIN times are based on internal logic speed; the maximum useable speed of the EMIF may be lower due to AC timing requirements.

16/ E = the EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) period in ns for EMIFA or EMIFB.

17/ EH is the high period of E (EMIF input clock period) in ns and EL is the low period of E (EMIF input clock period) in ns for EMIFA or EMIFB.

18/ This period jitter specification was measured with CPU/4 or CPU/6 as the source of the EMIF input clock.

19/ E = the EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) period in ns for EMIFA or EMIFB.
N = the EMIF input clock divider; N = 1, 2, or 4.

20/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is *only* recognized two cycles before the end of the programmed strobe time and while ARDY is low, the strobe time is extended cycle-by-cycle. When ARDY is recognized low, the end of the strobe time is two cycles after ARDY is recognized high. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.

21/ RS = Read setup, RST = Read strobe, RH = read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

TABLE I. Electrical performance characteristics – Continued.

22/ These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the asynchronous memory access signals are shown as generic (AOE, ARE, and AWE) instead of AAOE, AARE, and AAWE (for EMIFA) and BAOE, BARE, and BAWE (for EMIFB)].

23/ E = ECLKOUT1 period in ns for EMIFA or EMIFB.

24/ Select signals for EMIFA include: $\overline{\text{ACEx}}$, $\overline{\text{ABE[7:0]}}$, AEA[22:3], $\overline{\text{AAOE}}$; and for EMIFA writes, include AED[63:0].
Select signals for EMIFB include: $\overline{\text{BCEx}}$, $\overline{\text{BBE[1:0]}}$, BEA[20:1], $\overline{\text{BAOE}}$; and for EMIFB writes, include BED[15:0].

25/ These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the programmable synchronous interface access signals are shown as generic (SADS/SRE, SOE, and SWE) instead of ASADS/ASRE, ASOE, and ASWE (for EMIFA) and BSADS/BSRE, BSOE, and BSWE (for EMIFB)].

26/ The following parameters are programmable via the EMIF CE Space Secondary Control register (CExSEC):
- Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
- Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
- $\overline{\text{CEx}}$ assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{CEx}}$ goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, $\overline{\text{CEx}}$ is active when $\overline{\text{SOE}}$ is active (CEEXT = 1).
- Function of $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ (RENEN): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ acts as $\overline{\text{SADS}}$ with deselect cycles (RENEN = 0). For FIFO interface, $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ acts as $\overline{\text{SRE}}$ with NO deselect cycles (RENEN = 1).
- Synchronization clock (SNCCLK): Synchronized to ECLKOUT1 or ECLKOUT2.

27/ These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].

28/ For EMIFA, EMIF Bus consists of: $\overline{\text{ACE[3:0]}}$, $\overline{\text{ABE[7:0]}}$, AED[63:0], AEA[22:3], $\overline{\text{AARE}}$/$\overline{\text{ASDCAS}}$/$\overline{\text{ASADS}}$/$\overline{\text{ASRE}}$, AAOE/ASDRAS/ASOE, and $\overline{\text{AAWE}}$/$\overline{\text{ASDWE}}$/$\overline{\text{ASWE}}$, ASDCKE, ASOE3, and $\overline{\text{APDT}}$.
For EMIFB, EMIF Bus consists of: $\overline{\text{BCE[3:0]}}$, $\overline{\text{BBE[1:0]}}$, BED[15:0], BEA[20:1], $\overline{\text{BARE}}$/$\overline{\text{BSDCAS}}$/$\overline{\text{BSADS}}$/$\overline{\text{BSRE}}$, BAOE/BSDRAS/BSOE, and $\overline{\text{BAWE}}$/$\overline{\text{BSDWE}}$/$\overline{\text{BSWE}}$, BSOE3, and BPDT.

29/ The EkxHZ bits in the EMIF Global control register (GBLCTL) determine the state of the ECLKOUTx signals during HOLDA. If EkxHZ = 0, ECLKOUTx continues clocking during Hold mode. If EkxHZ = 1, ECLKOUTx goes to high impedance during Hold mode, as shown in figure 5m.

30/ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.

31/ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x6, x12 when CLKIN and PLL are stable.

32/ This parameter applies to CLKMODE x6, x12 only (it does not apply to CLKMODE x1). The $\overline{\text{RESET}}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following device power-up or after PLL configuration has been changed. During that time, RESET must be asserted to ensure proper device operation.

33/ EMIFB address pins BEA[20:13, 11, 7] are the boot configuration pins during device reset.

TABLE I. Electrical performance characteristics – Continued.

34/ EMIF Z group consists of: AEA[22:3], BEA[20:1], AED[63:0], BED[15:0], $\overline{CE}$[3:0], $\overline{ABE}$[7:0], $\overline{BBE}$[1:0], $\overline{ARE}$/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE, SOE3, ASDCKE, and $\overline{PDT}$.

EMIF high group consists of: $\overline{AHOLDA}$ and $\overline{BHOLDA}$ (when the corresponding $\overline{HOLD}$ input is high).

EMIF low group consists of: ABUSREQ and BBUSREQ; $\overline{AHOLDA}$ and $\overline{BHOLDA}$ (when the corresponding $\overline{HOLD}$ input is low).

Low group consists of: XSP_CS, CLKX2/XSP_CLK, and DX2/XSP_DO; all of which apply only when PCI EEPROM (BEA13) is enabled (with PCI_EN = 1 and MCBSP2_EN = 0). Otherwise, the CLKX2/XSP_CLK and DX2/XSP_DO pins are in the Z group.

Z group consists of: HD[31:0]/AD[31:0], CLKX0, CLKX1/URADDR4, CLKX2/XSP_CLK, FSX0, FSX1/UXADDR3, FSX2, DX0, DX1/UXADDR4, DX2/XSP_DO, CLKR0, CLKR1/URADDR2, CLKR2, FSR0, FSR1/UXADDR2, FSR2, TOUT0, TOUT1, TOUT2, GP[8:0], GP10/PCBE3, HR/W/PCBE2, HDS2/PCBE1, PCBE0, GP13/PINTA, GP11/PREQ, HDS1/PSERR, HCS/PPERR, HCNTL1/PDEVSEL, HAS/PPAR, HCNTL0/PSTOP, HHWIL/PTRDY (16-bit HPI mode only), HRDY/PIRDY, HINT/PFRAME, UXDATA[7:0], UXSOC, UXCLAV, and URCLAV.

35/ $\overline{HSTROBE}$ refers to the following logical operation on $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$: [NOT($\overline{HDS1}$ XOR $\overline{HDS2}$)] OR $\overline{HCS}$.

36/ Select signals include: HCNTL[1:0] and HR/$\overline{W}$. For HPI16 mode only, select signals also include HHWIL.

37/ Select the parameter value of 4P or 12.5 ns, whichever is greater.

38/ $\overline{HSTROBE}$ should not be inactivated until $\overline{HRDY}$ is active (low); otherwise, HPI writes will not complete properly.

39/ This parameter is used during HPID reads and writes. For reads, at the beginning of a word transfer (HPI32) or the first half-word transfer (HPI16) on the falling edge of HSTROBE, the HPI sends the request to the EDMA internal address generation hardware, and HRDY remains high until the EDMA internal address generation hardware loads the requested data into HPID. For writes, HRDY goes high if the internal write buffer is full.

40/ For 3.3-V operation, the reference points for the rise and fall transitions are measured at V_{ILP} MAX and V_{IHP} MIN.

41/ Select the parameter value of 30 ns or 8P, whichever is greater.

42/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

43/ Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and ac timing requirements.

44/ This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

45/ Minimum delay times also represent minimum output hold times.

46/ C = H or L
S = sample rate generator input clock = 4P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see footnote 42/).

TABLE I. Electrical performance characteristics – Continued.

47/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 4P, D2 = 8P

48/ ONLY applies when in data delay 0 (XDATDLY = 00b) mode.

49/ For all SPI Slave modes, CLKG is programmed as 1/4 of the CPU clock by setting CLKSM = CLKGDV = 1.

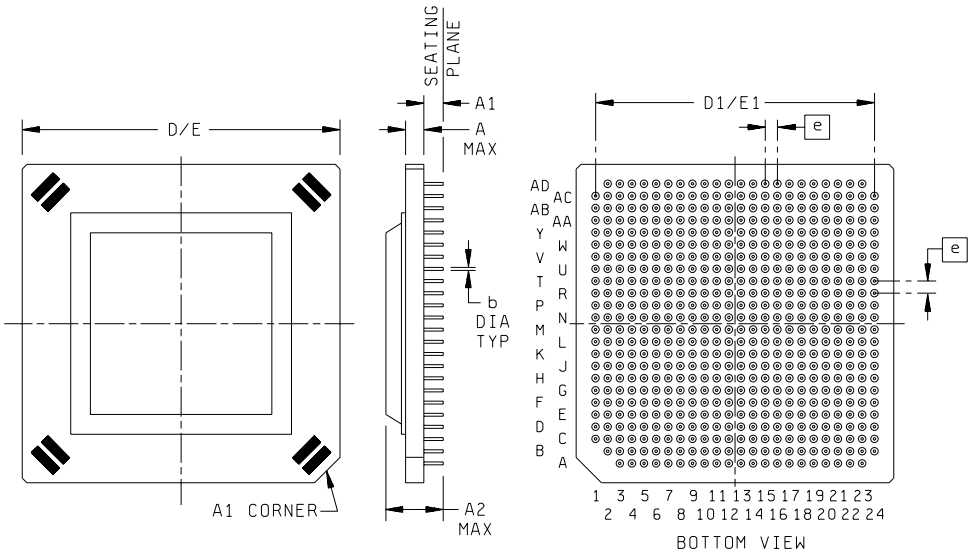
50/ FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active-low slave-enable output. As a Slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP

51/ S = sample rate generator input clock = 4P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

52/ FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

53/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 12P to allow the DSP enough time to access the GPIO register through the CFGBUS.

Case X



Case outline	X			
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.075	---	1.90
A1	0.070	0.090	1.78	2.28
A2	---	0.236	---	6.00
b	0.010	0.014	0.254	0.356
D/E	1.290	1.330	32.77	33.78
D1/E1	1.150 TYP		29.21 TYP	
e	0.050 NOM		1.27 NOM	

NOTES:
1. All linear dimensions are in inches. Millimeter equivalents are given for general information only.
2. This package is hermetically sealed with a metal lid.

Ceramic Pin Grid Array Thermal Resistance Characteristics

$R\theta_{JA}$ Junction-to-free air (Low K JEDEC PCB): ..... 20.96°C/W
$R\theta_{JA}$ Junction-to-free air (High K JEDEC PCB):..... 16.5°C/W
$R\theta_{JC}$ Junction-to-case (High K JEDEC PCB w/heat sink on lid):..... 10.9°C/W
$R\theta_{JC}$ Junction-to-case (High K JEDEC PCB w/heat sink on body):..... 7.69°C/W
$R\theta_{JB}$ Junction-to-board (High K JEDEC PCB):..... 9.0°C/W
$R\theta_{JB}$ Junction-to-board (High K JEDEC PCB w/Thermal Compound on top of the die):..... 2.93°C/W

FIGURE 2. Case outline.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A3	V_{SS}	B21	DV_{DD}-3.3V
A4	CV_{DD}-1.2V/1.4V	B22	DV_{DD}-3.3V
A5	V_{SS}	B23	V_{SS}
A6	CV_{DD}-1.2V/1.4V	B24	CV_{DD}-1.2V/1.4V
A7	V_{SS}	C1	CV_{DD}-1.2V/1.4V
A8	CV_{DD}-1.2V/1.4V	C2	CV_{DD}-1.2V/1.4V
A9	V_{SS}	C3	V_{SS}
A10	CV_{DD}-1.2V/1.4V	C4	RSV
A11	V_{SS}	C5	BED12
A12	CV_{DD}-1.2V/1.4V	C6	BED9
A13	V_{SS}	C7	$\overline{BARE}$/$\overline{BSDCAS}$/$\overline{BSADS}$/$\overline{BSRE}$
A14	CV_{DD}-1.2V/1.4V	C8	BECLKOUT2
A15	V_{SS}	C9	$\overline{BCE2}$
A16	CV_{DD}-1.2V/1.4V	C10	DV_{DD}-3.3V
A17	V_{SS}	C11	DV_{DD}-3.3V
A18	CV_{DD}-1.2V/1.4V	C12	CV_{DD}-1.2V/1.4V
A19	V_{SS}	C13	CV_{DD}-1.2V/1.4V
A20	CV_{DD}-1.2V/1.4V	C14	DV_{DD}-3.3V
A21	V_{SS}	C15	DV_{DD}-3.3V
A22	CV_{DD}-1.2V/1.4V	C16	BEA5
A23	V_{SS}	C17	BEA10
B2	V_{SS}	C18	BEA15
B3	DV_{DD}-3.3V	C19	$\overline{BHOLD}$
B4	DV_{DD}-3.3V	C20	AED12
B5	CV_{DD}-1.2V/1.4V	C21	AED0
B6	DV_{DD}-3.3V	C22	V_{SS}
B7	CV_{DD}-1.2V/1.4V	C23	DV_{DD}-3.3V
B8	V_{SS}	C24	V_{SS}
B9	DV_{DD}-3.3V	D1	V_{SS}
B10	V_{SS}	D2	DV_{DD}-3.3V
B11	DV_{DD}-3.3V	D3	FSR0
B12	V_{SS}	D4	V_{SS}
B13	DV_{DD}-3.3V	D5	TINP2
B14	V_{SS}	D6	TINP1
B15	DV_{DD}-3.3V	D7	BED13
B16	V_{SS}	D8	BED2
B17	DV_{DD}-3.3V	D9	BED3
B18	V_{SS}	D10	$\overline{BAOE}$/$\overline{BSDRAS}$/$\overline{BSOE}$
B19	DV_{DD}-3.3V	D11	$\overline{BCE3}$
B20	CV_{DD}-1.2V/1.4V	D12	$\overline{BBE1}$

FIGURE 3. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
D13	BEA2	F5	CLKR0
D14	BBUSREQ	F6	V_{SS}
D15	BEA4	F7	TOUT2
D16	BEA13	F8	BED15
D17	BEA19	F9	BED6
D18	AED11	F10	BED0
D19	AED8	F11	$\overline{BAWE}/\overline{BSDWE}/\overline{BSWE}$
D20	AED3	F12	$\overline{BHOLDA}$
D21	V_{SS}	F13	BEA1
D22	AED31	F14	BEA11
D23	DV_{DD}-3.3V	F15	BEA14
D24	CV_{DD}-1.2V/1.4V	F16	AED15
E1	CV_{DD}-1.2V/1.4V	F17	AED9
E2	V_{SS}	F18	AED2
E3	CLKMODE0	F19	V_{SS}
E4	DX0	F20	AED29
E5	V_{SS}	F21	AED26
E6	NMI	F22	AED16
E7	TINP0	F23	DV_{DD}-3.3V
E8	BED8	F24	CV_{DD}-1.2V/1.4V
E9	BED7	G1	CV_{DD}-1.2V/1.4V
E10	BECLKIN	G2	V_{SS}
E11	$\overline{BPDT}$	G3	DV_{DD}-3.3V
E12	$\overline{BBE0}$	G4	GP13/$\overline{PINTA}$
E13	BEA3	G5	GP14/PCLK
E14	BEA7	G6	DR0
E15	BEA20	G7	V_{SS}
E16	BEA17	G8	TOUT1
E17	AED14	G9	BED10
E18	AED7	G10	BED5
E19	AED1	G11	BARDY
E20	V_{SS}	G12	$\overline{BCE0}$
E21	AED27	G13	BEA9
E22	AED22	G14	BEA8
E23	CV_{DD}-1.2V/1.4V	G15	BEA16
E24	V_{SS}	G16	AED10
F1	V_{SS}	G17	AED4
F2	DV_{DD}-3.3V	G18	V_{SS}
F3	DV_{DD}-3.3V	G19	AED30
F4	CLKS0	G20	AED25

FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
G21	AED21	J13	$\overline{BSOE3}$
G22	$\overline{AAWE}/\overline{ASDWE}/\overline{ASWE}$	J14	BEA18
G23	CV_{DD}-1.2V/1.4V	J15	AED6
G24	V_{SS}	J16	V_{SS}
H1	V_{SS}	J17	AED23
H2	DV_{DD}-3.3V	J18	AED20
H3	RSV	J19	AECLKIN
H4	CLKIN	J20	$\overline{AAOE}/\overline{ASDRAS}/\overline{ASOE}$
H5	RSV	J21	$\overline{ACE1}$
H6	GP11/$\overline{PREQ}$	J22	AEA3
H7	FSX0	J23	DV_{DD}-3.3V
H8	V_{SS}	J24	V_{SS}
H9	TOUT0	K1	V_{SS}
H10	BED11	K2	DV_{DD}-3.3V
H11	BED1	K3	DV_{DD}-3.3V
H12	$\overline{BCE1}$	K4	HD28/AD28
H13	BEA6	K5	HD27/AD27
H14	BEA12	K6	GP9/PIDSEL
H15	AED13	K7	HD30/AD30
H16	AED5	K8	CLKMODE1
H17	V_{SS}	K9	CLKX0
H18	AED28	K10	CV_{DD}-1.2V/1.4V
H19	AED19	K11	V_{SS}
H20	AED18	K12	CV_{DD}-1.2V/1.4V
H21	AECLKOUT1	K13	V_{SS}
H22	$\overline{ABE1}$	K14	CV_{DD}-1.2V/1.4V
H23	V_{SS}	K15	V_{SS}
H24	CV_{DD}-1.2V/1.4V	K16	AED24
J1	CV_{DD}-1.2V/1.4V	K17	AED17
J2	V_{SS}	K18	AECLKOUT2
J3	DV_{DD}-3.3V	K19	$\overline{ACE0}$
J4	HD31/AD31	K20	$\overline{ACE3}$
J5	HD29/AD29	K21	ASDCKE
J6	HD24/AD24	K22	DV_{DD}-3.3V
J7	GP12/$\overline{PGNT}$	K23	V_{SS}
J8	GP15/$\overline{PRST}$	K24	CV_{DD}-1.2V/1.4V
J9	V_{SS}	L1	CV_{DD}-1.2V/1.4V
J10	BED14	L2	V_{SS}
J11	BED4	L3	CV_{DD}-1.2V/1.4V
J12	BECLKOUT1	L4	HD19/AD19

FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
L5	HD23/AD23	M21	AEA7
L6	HD26/AD26	M22	CV_{DD}-1.2V/1.4V
L7	GP10/$\overline{PCBE3}$	M23	V_{SS}
L8	HD25/AD25	M24	CV_{DD}-1.2V/1.4V
L9	PLLV	N1	CV_{DD}-1.2V/1.4V
L10	V_{SS}	N2	V_{SS}
L11	CV_{DD}-1.2V/1.4V	N3	RSV
L12	V_{SS}	N4	$\overline{HRDY}$/$\overline{PIRDY}$
L13	CV_{DD}-1.2V/1.4V	N5	HHWIL/$\overline{PTRDY}$
L14	V_{SS}	N6	HR/$\overline{W}$/$\overline{PCBE2}$
L15	CV_{DD}-1.2V/1.4V	N7	$\overline{HAS}$/$\overline{PPAR}$
L16	$\overline{AARE}$/$\overline{ASDCAS}$/$\overline{ASADS}$/$\overline{ASRE}$	N8	HCNTL1/$\overline{PDEVSEL}$
L17	$\overline{ACE2}$	N9	$\overline{HCS}$/$\overline{PPERR}$
L18	AARDY	N10	V_{SS}
L19	$\overline{ABE0}$	N11	CV_{DD}-1.2V/1.4V
L20	$\overline{APDT}$	N12	V_{SS}
L21	AEA5	N13	CV_{DD}-1.2V/1.4V
L22	DV_{DD}-3.3V	N14	V_{SS}
L23	DV_{DD}-3.3V	N15	CV_{DD}-1.2V/1.4V
L24	V_{SS}	N16	$\overline{ASOE3}$
M1	V_{SS}	N17	AEA11
M2	DV_{DD}-3.3V	N18	AEA14
M3	CV_{DD}-1.2V/1.4V	N19	AEA8
M4	HD18/AD18	N20	AEA10
M5	HD22/AD22	N21	AEA9
M6	HD21/AD21	N22	CV_{DD}-1.2V/1.4V
M7	HD16/AD16	N23	DV_{DD}-3.3V
M8	HD20/AD20	N24	V_{SS}
M9	HD17/AD17	P1	V_{SS}
M10	CV_{DD}-1.2V/1.4V	P2	DV_{DD}-3.3V
M11	V_{SS}	P3	RSV
M12	CV_{DD}-1.2V/1.4V	P4	$\overline{HINT}$/$\overline{PFRAME}$
M13	V_{SS}	P5	HCNTL0/$\overline{PSTOP}$
M14	CV_{DD}-1.2V/1.4V	P6	$\overline{HDS2}$/$\overline{PCBE1}$
M15	V_{SS}	P7	HD12/AD12
M16	AEA4	P8	HD15/AD15
M17	$\overline{ABE3}$	P9	HD8/AD8
M18	$\overline{ABE2}$	P10	CV_{DD}-1.2V/1.4V
M19	$\overline{AHOLDA}$	P11	V_{SS}
M20	AEA6	P12	CV_{DD}-1.2V/1.4V

FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
P13	V_{SS}	T5	HD10/AD10
P14	CV_{DD}-1.2V/1.4V	T6	HD7/AD7
P15	V_{SS}	T7	HD3/AD3
P16	AEA21	T8	PCI_EN
P17	AEA15	T9	V_{SS}
P18	AEA13	T10	CLKOUT6/GP2
P19	$\overline{ABE7}$	T11	UXDATA6
P20	AEA12	T12	CLKX1/URADDR4
P21	ABUSREQ	T13	EMU1
P22	DV_{DD}-3.3V	T14	EMU9
P23	V_{SS}	T15	AED56
P24	CV_{DD}-1.2V/1.4V	T16	V_{SS}
R1	CV_{DD}-1.2V/1.4V	T17	AED37
R2	V_{SS}	T18	AED42
R3	CV_{DD}-1.2V/1.4V	T19	AED47
R4	HD13/AD13	T20	AEA20
R5	$\overline{HDS1}$/$\overline{PSERR}$	T21	AEA16
R6	HD14/AD14	T22	$\overline{ABE5}$
R7	HD11/AD11	T23	V_{SS}
R8	HD6/AD6	T24	CV_{DD}-1.2V/1.4V
R9	DX2/XSP_DO	U1	CV_{DD}-1.2V/1.4V
R10	V_{SS}	U2	V_{SS}
R11	CV_{DD}-1.2V/1.4V	U3	DV_{DD}-3.3V
R12	V_{SS}	U4	HD5/AD5
R13	CV_{DD}-1.2V/1.4V	U5	HD4/AD4
R14	V_{SS}	U6	HD2/AD2
R15	CV_{DD}-1.2V/1.4V	U7	FSX2
R16	AED38	U8	V_{SS}
R17	AED45	U9	GP4/EXT_INT4
R18	AEA19	U10	UXDATA2
R19	AEA17	U11	URADDR1
R20	AEA22	U12	URCLK
R21	$\overline{ABE4}$	U13	$\overline{UXENB}$
R22	DV_{DD}-3.3V	U14	EMU8
R23	DV_{DD}-3.3V	U15	AED49
R24	V_{SS}	U16	AED55
T1	V_{SS}	U17	V_{SS}
T2	DV_{DD}-3.3V	U18	AED36
T3	DV_{DD}-3.3V	U19	AED41
T4	HD9/AD9	U20	AED46

FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
U21	$\overline{AHOLD}$	W13	URSOC
U22	$\overline{ABE6}$	W14	EMU3
U23	DV_{DD}-3.3V	W15	EMU5
U24	V_{SS}	W16	TDO
V1	V_{SS}	W17	AED51
V2	DV_{DD}-3.3V	W18	AED62
V3	DV_{DD}-3.3V	W19	V_{SS}
V4	HD1/AD1	W20	AED33
V5	HD0/AD0	W21	AED40
V6	FSR2	W22	RSV
V7	V_{SS}	W23	DV_{DD}-3.3V
V8	GP6/EXT_INT6	W24	V_{SS}
V9	UXDATA0	Y1	V_{SS}
V10	UXDATA3	Y2	DV_{DD}-3.3V
V11	DR1/UXADDR1	Y3	$\overline{PCBE0}$
V12	URDATA6	Y4	DR2/XSP_DI
V13	EMU0	Y5	V_{SS}
V14	TMS	Y6	GP7/EXT_INT7
V15	EMU11	Y7	CLKOUT4/GP1
V16	AED52	Y8	CLKS1/URADDR3
V17	AED60	Y9	UXADDR0
V18	V_{SS}	Y10	DX1/UXADDR4
V19	AED34	Y11	URDATA3
V20	AED39	Y12	UXSOC
V21	AED43	Y13	URDATA1
V22	AEA18	Y14	$\overline{TRST}$
V23	V_{SS}	Y15	TCK
V24	CV_{DD}-1.2V/1.4V	Y16	EMU10
W1	CV_{DD}-1.2V/1.4V	Y17	AED50
W2	V_{SS}	Y18	AED57
W3	DV_{DD}-3.3V	Y19	AED61
W4	CLKR2	Y20	V_{SS}
W5	CLKX2/XSP_CLK	Y21	AED35
W6	V_{SS}	Y22	AED44
W7	CLKS2/GP8	Y23	CV_{DD}-1.2V/1.4V
W8	GP0	Y24	CV_{DD}-1.2V/1.4V
W9	UXDATA5	AA1	CV_{DD}-1.2V/1.4V
W10	UXDATA7	AA2	V_{SS}
W11	URDATA4	AA3	XSP_CS
W12	URDATA5	AA4	V_{SS}

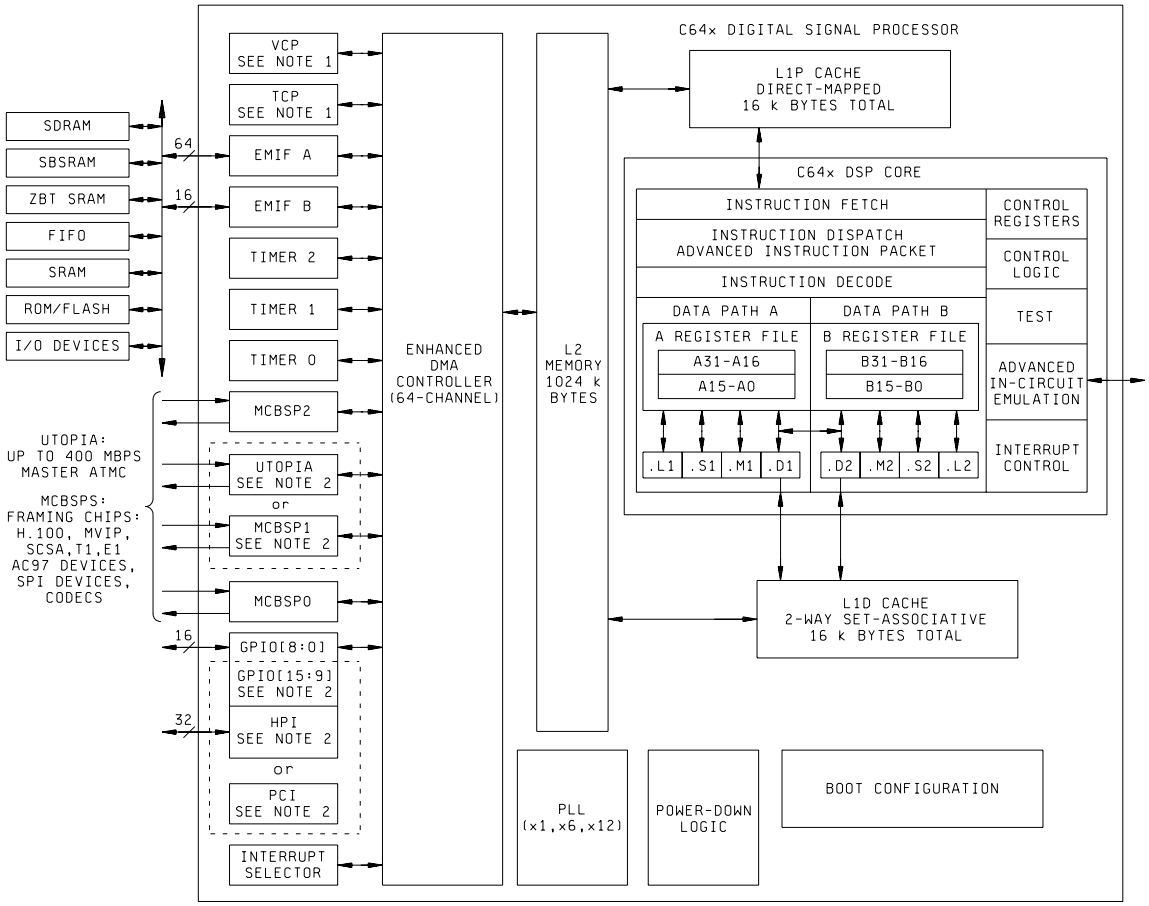
FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
AA5	GP5/EXT_INT5	AB21	AED63
AA6	GP3	AB22	V_{SS}
AA7	UXDATA1	AB23	DV_{DD}-3.3V
AA8	FSR1/UXADDR2	AB24	CV_{DD}-1.2V/1.4V
AA9	URADDR0	AC1	V_{SS}
AA10	URDATA7	AC2	V_{SS}
AA11	FSX1/UXADDR3	AC3	DV_{DD}-3.3V
AA12	URDATA0	AC4	DV_{DD}-3.3V
AA13	UXCLAV	AC5	CV_{DD}-1.2V/1.4V
AA14	URCLAV	AC6	DV_{DD}-3.3V
AA15	EMU2	AC7	V_{SS}
AA16	EMU6	AC8	DV_{DD}-3.3V
AA17	TDI	AC9	V_{SS}
AA18	AED53	AC10	DV_{DD}-3.3V
AA19	AED58	AC11	V_{SS}
AA20	AED59	AC12	DV_{DD}-3.3V
AA21	V_{SS}	AC13	V_{SS}
AA22	AED32	AC14	DV_{DD}-3.3V
AA23	DV_{DD}-3.3V	AC15	V_{SS}
AA24	V_{SS}	AC16	DV_{DD}-3.3V
AB1	V_{SS}	AC17	V_{SS}
AB2	DV_{DD}-3.3V	AC18	CV_{DD}-1.2V/1.4V
AB3	V_{SS}	AC19	DV_{DD}-3.3V
AB4	MCBSP2_EN	AC20	CV_{DD}-1.2V/1.4V
AB5	$\overline{\text{RESET}}$	AC21	DV_{DD}-3.3V
AB6	UXDATA4	AC22	DV_{DD}-3.3V
AB7	CLKR1/URADDR2	AC23	V_{SS}
AB8	UXCLK	AC24	V_{SS}
AB9	URDATA2	AD2	V_{SS}
AB10	DV_{DD}-3.3V	AD3	CV_{DD}-1.2V/1.4V
AB11	DV_{DD}-3.3V	AD4	V_{SS}
AB12	CV_{DD}-1.2V/1.4V	AD5	CV_{DD}-1.2V/1.4V
AB13	CV_{DD}-1.2V/1.4V	AD6	V_{SS}
AB14	DV_{DD}-3.3V	AD7	CV_{DD}-1.2V/1.4V
AB15	DV_{DD}-3.3V	AD8	V_{SS}
AB16	$\overline{\text{URENB}}$	AD9	CV_{DD}-1.2V/1.4V
AB17	EMU4	AD10	V_{SS}
AB18	EMU7	AD11	CV_{DD}-1.2V/1.4V
AB19	AED48	AD12	V_{SS}
AB20	AED54	AD13	CV_{DD}-1.2V/1.4V

FIGURE 3. Terminal connections – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
AD14	V_{SS}	AD19	CV_{DD}-1.2V/1.4V
AD15	CV_{DD}-1.2V/1.4V	AD20	V_{SS}
AD16	V_{SS}	AD21	CV_{DD}-1.2V/1.4V
AD17	CV_{DD}-1.2V/1.4V	AD22	V_{SS}
AD18	V_{SS}	AD23	CV_{DD}-1.2V/1.4V

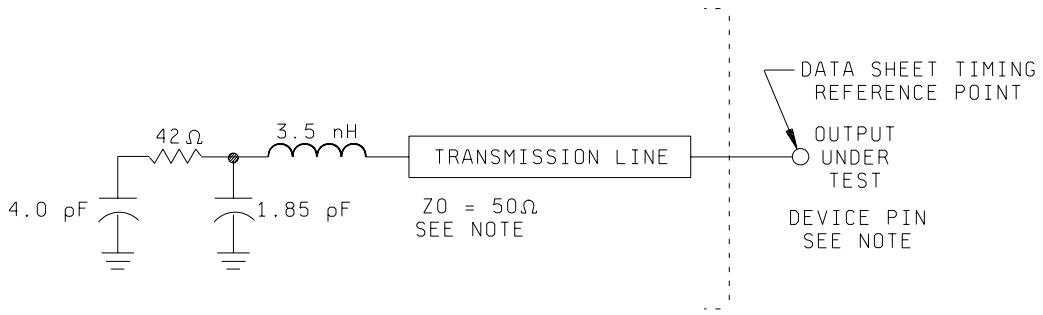
FIGURE 3. Terminal connections – Continued.



NOTES:

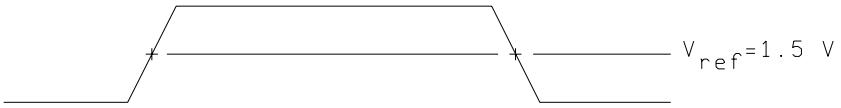
1. VCP and TCP decoder coprocessors are not applicable to the C6415 device.
2. For the C6415 device, the UTOPIA peripheral is muxed with McBSP1, and the PCI peripheral is muxed with the HPI peripheral and the GPIO[15:9] port.

FIGURE 4. Block diagram.

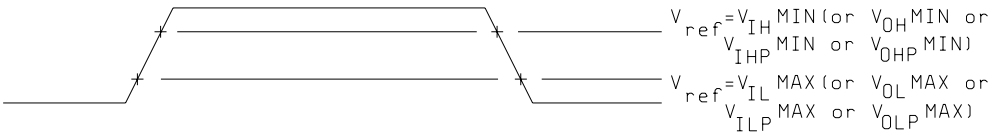


TEST LOAD CIRCUIT FOR AC TIMING MEASUREMENTS

NOTE: The data sheet (table I) provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the table I timings. Input requirements are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.



INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS



RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

FIGURE 5a. Test circuit and switching waveforms.

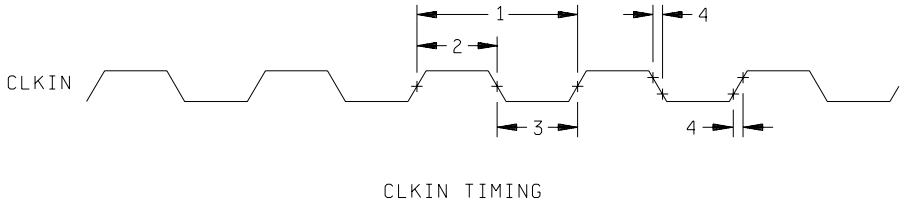


FIGURE 5b. Test circuit and switching waveforms.

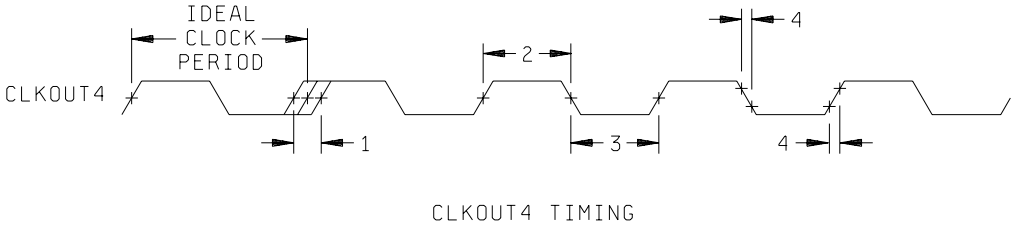


FIGURE 5c. Test circuit and switching waveforms.

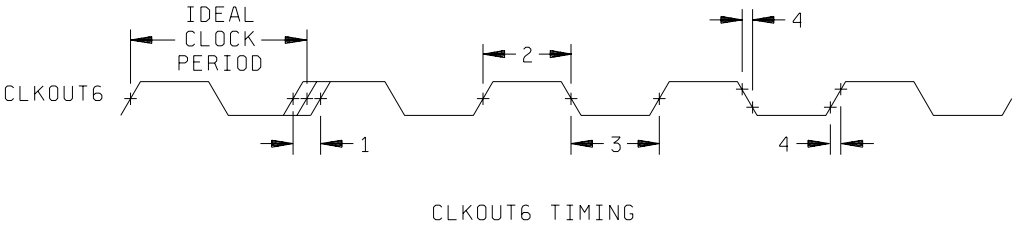


FIGURE 5d. Test circuit and switching waveforms.

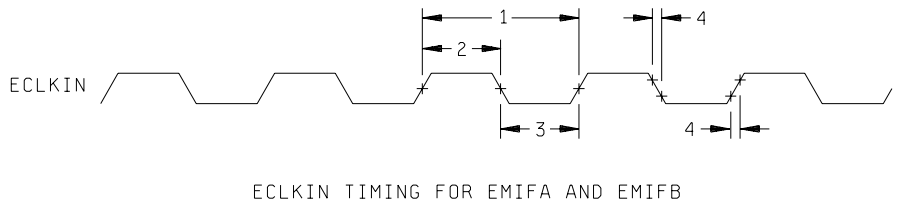


FIGURE 5e. Test circuit and switching waveforms.

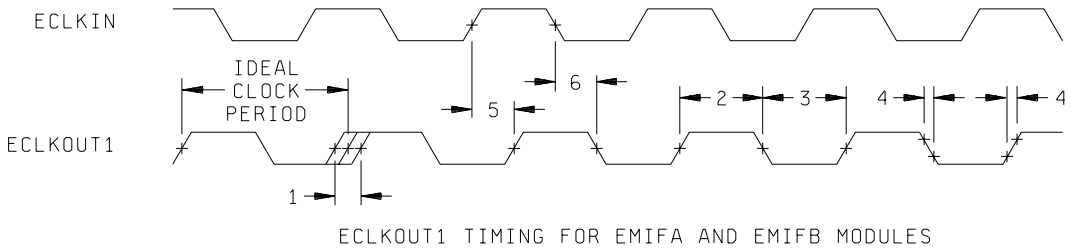


FIGURE 5f. Test circuit and switching waveforms.

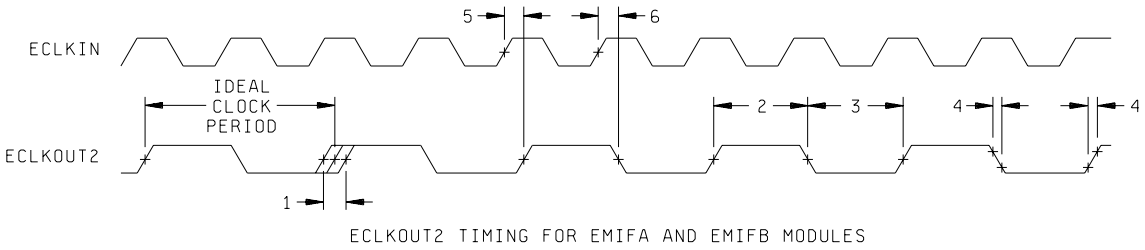
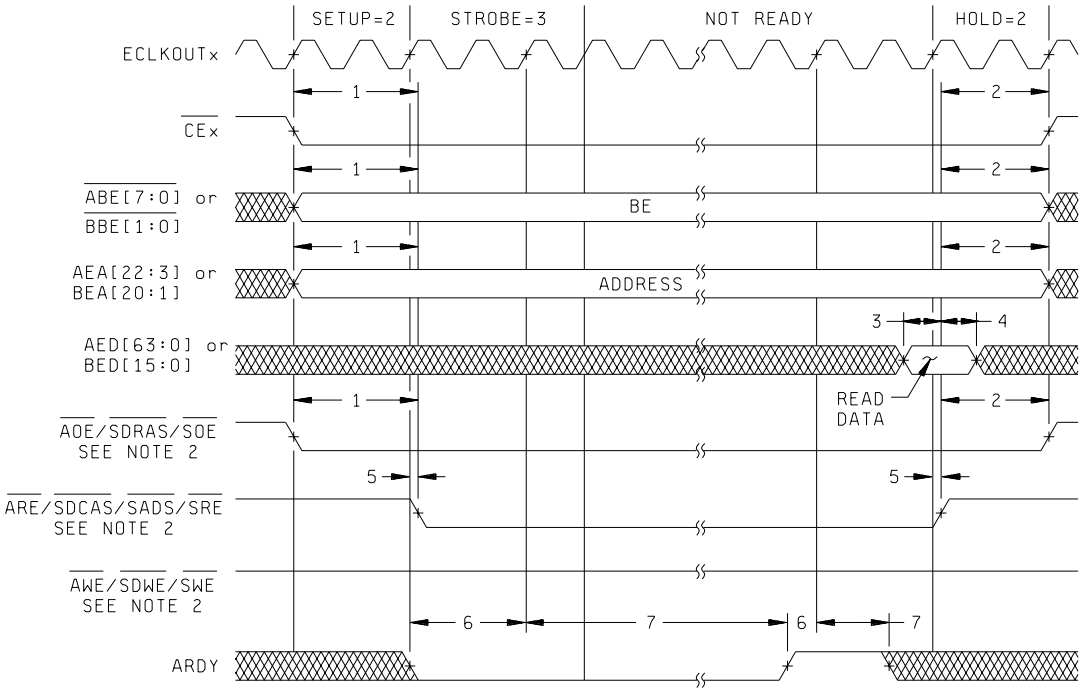


FIGURE 5g. Test circuit and switching waveforms.

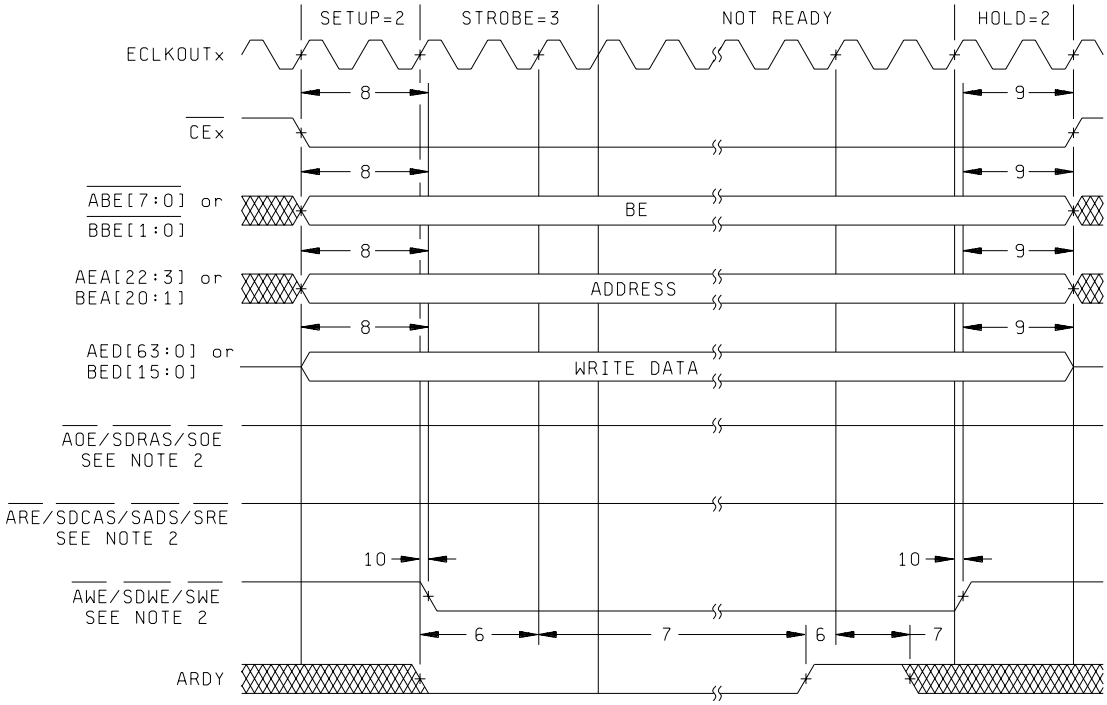


ASYNCHRONOUS MEMORY READ TIMING FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the asynchronous memory access signals are shown as generic (AOE, ARE, and AWE) instead of AAOE, AARE, and AAWE (for EMIFA) and BAOE, BARE, and BAWE (for EMIFB)].
2. AOE/SDRAS/SOE, ARE/SDCAS/SADS/SRE, and AWE/SDWE/SWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

FIGURE 5h. Test circuit and switching waveforms.

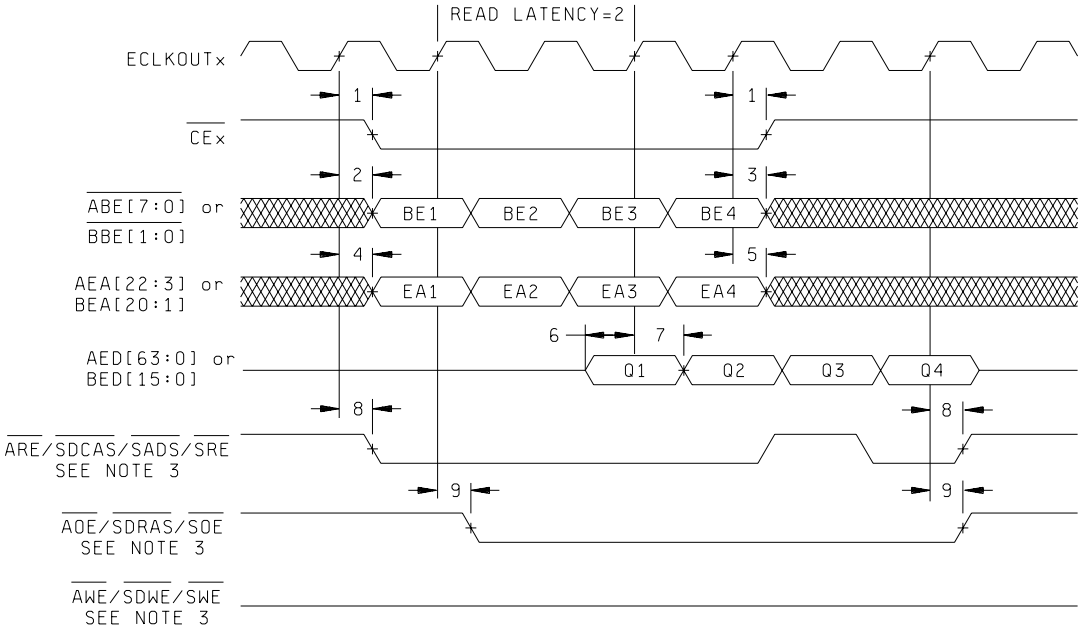


ASYNCHRONOUS MEMORY WRITE TIMING FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the asynchronous memory access signals are shown as generic (AOE, ARE, and AWE) instead of AAOE, AARE, and AAWE (for EMIFA) and BAOE, BARE, and BAWE (for EMIFB)].
2. AOE/SDRAS/SOE, ARE/SDCAS/SADS/SRE, and AWE/SDWE/SWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

FIGURE 5h. Test circuit and switching waveforms - Continued.

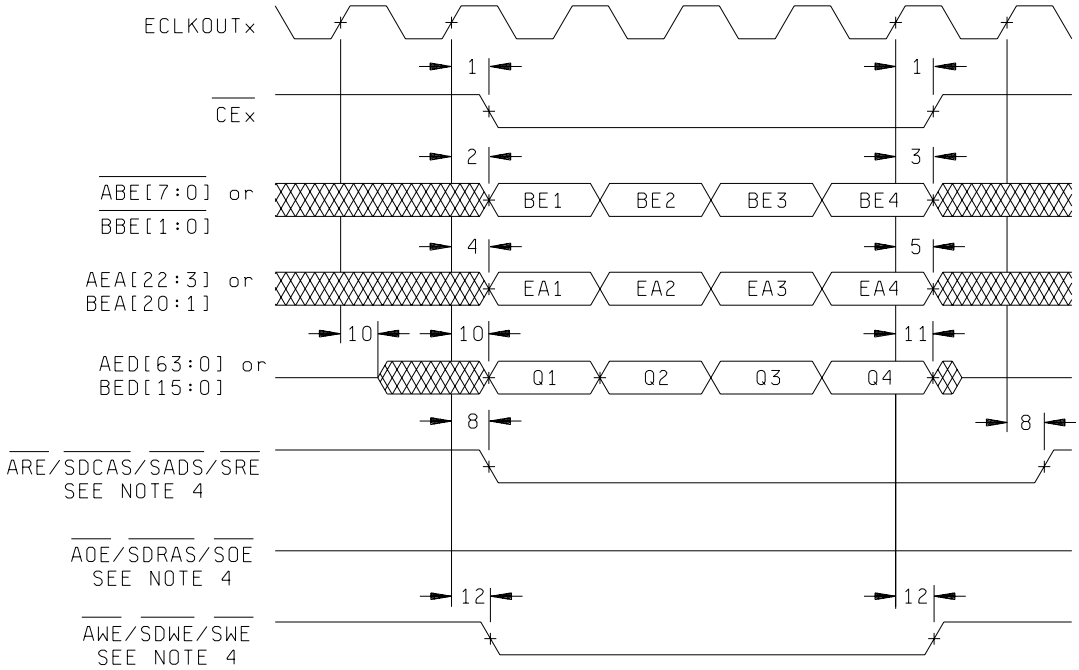


PROGRAMMABLE SYNCHRONOUS INTERFACE READ TIMING FOR EMIFA AND EMIFB
(WITH READ LATENCY=2)
SEE NOTES 1,2 AND 3

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the programmable synchronous interface access signals are shown as generic (SADS/SRE, SOE, and SWE) instead of ASADS/ASRE, ASOE, and ASWE (for EMIFA) and BSADS/BSRE, BSOE, and BSWE (for EMIFB)].
2. The read latency and the length of CEx assertion are programmable via the SYNCRL and CEEXT fields, respectively, in the EMIFx CE Space Secondary Control register (CExSEC). In this figure, SYNCRL = 2 and CEEXT = 0.
3. The following parameters are programmable via the EMIF CE Space Secondary Control register (CExSEC):
   - Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
   - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
   - CEx assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, CEx goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, CEx is active when SOE is active (CEEXT = 1).
   - Function of SADS/SRE (RENEN): For standard SBSRAM or ZBT SRAM interface, SADS/SRE acts as SADS with deselect cycles (RENEN = 0). For FIFO interface, SADS/SRE acts as SRE with NO deselect cycles (RENEN = 1).
   - Synchronization clock (SNCCLK): Synchronized to ECLKOUT1 or ECLKOUT2.

FIGURE 5j. Test circuit and switching waveforms.

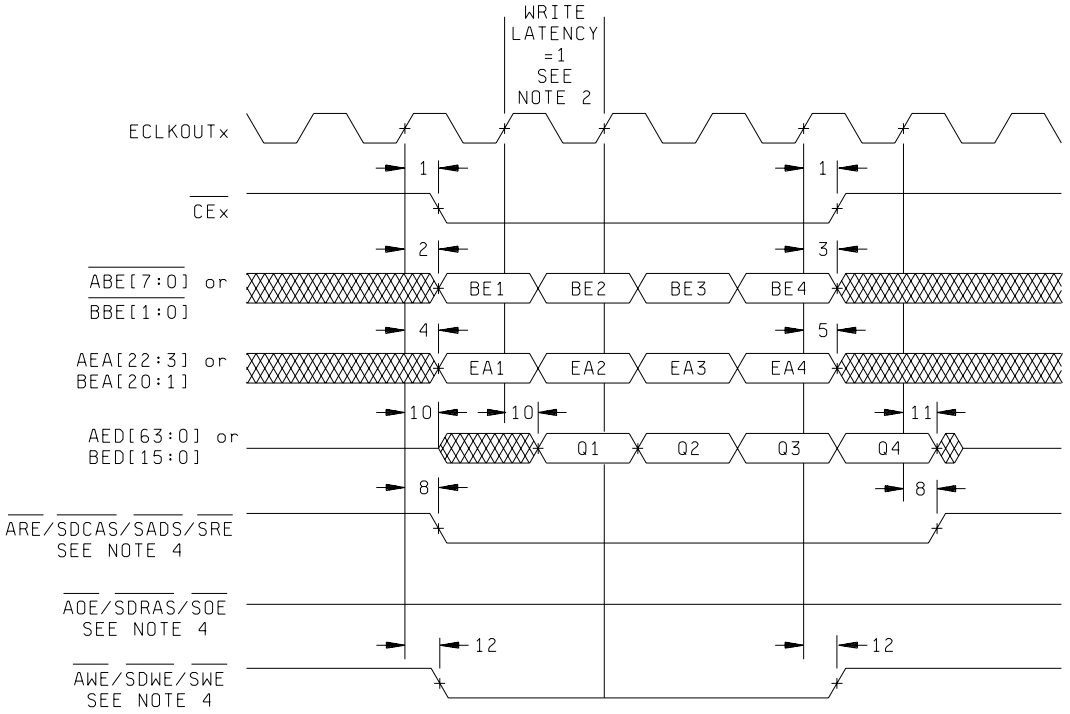


PROGRAMMABLE SYNCHRONOUS INTERFACE WRITE TIMING FOR EMIFA AND EMIFB
(WITH WRITE LATENCY=0)
SEE NOTES 1,2 AND 3

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the programmable synchronous interface access signals are shown as generic (SADS/SRE, SOE, and SWE) instead of ASADS/ASRE, ASOE, and ASWE (for EMIFA) and BSADS/BSRE, BSOE, and BSWE (for EMIFB)].
2. The write latency and the length of CEx assertion are programmable via the SYNCWL and CEEXT fields, respectively, in the EMIFx CE Space Secondary Control register (CExSEC). In this figure, SYNCWL = 0 and CEEXT = 0.
3. The following parameters are programmable via the EMIF CE Space Secondary Control register (CExSEC):
   - Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
   - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
   - CEx assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, CEx goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, CEx is active when SOE is active (CEEXT = 1).
   - Function of SADS/SRE (RENEN): For standard SBSRAM or ZBT SRAM interface, SADS/SRE acts as SADS with deselect cycles (RENEN = 0). For FIFO interface, SADS/SRE acts as SRE with NO deselect cycles (RENEN = 1).
   - Synchronization clock (SNCCLK): Synchronized to ECLKOUT1 or ECLKOUT2.
4. ARE/SDCAS/SADS/SRE, AOE/SDRAS/SOE, and AWE/SDWE/SWE operate as SADS/SRE, SOE, and SWE, respectively, during programmable synchronous interface accesses.

FIGURE 5j. Test circuit and switching waveforms - Continued.

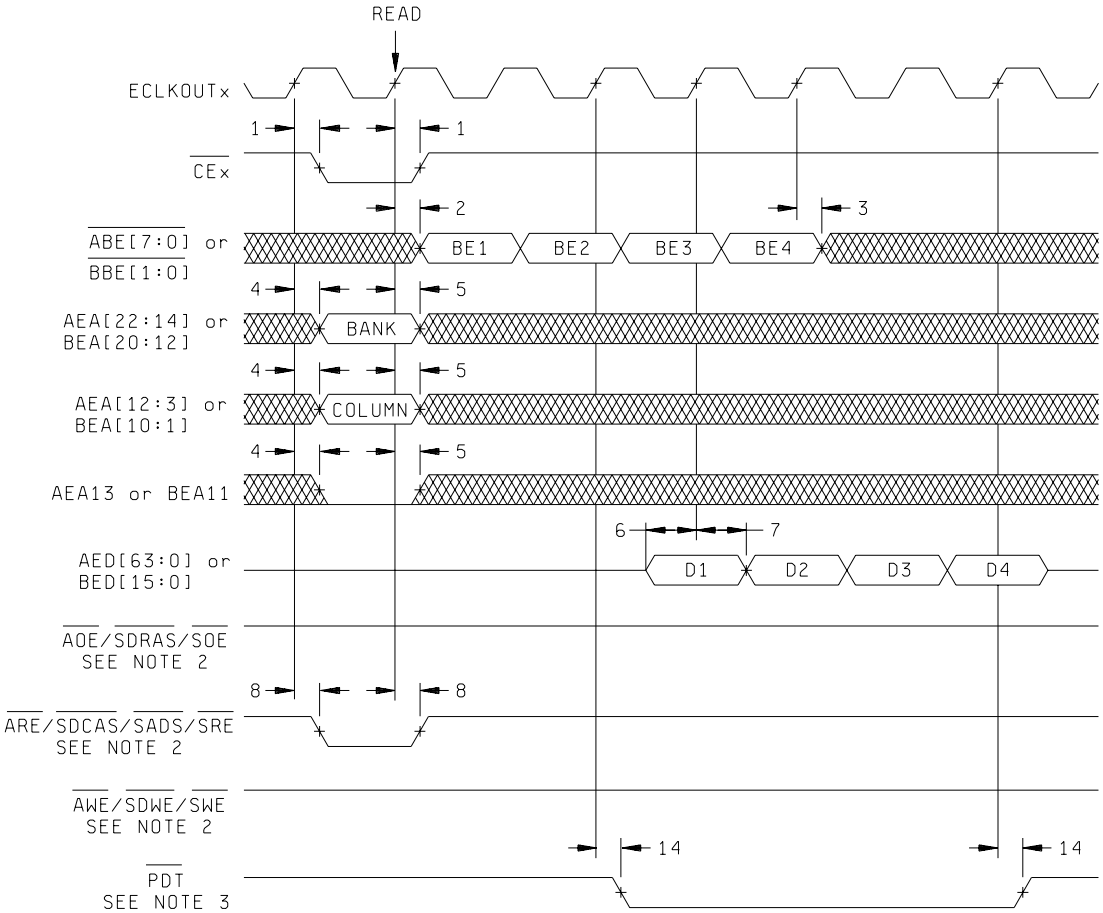


PROGRAMMABLE SYNCHRONOUS INTERFACE WRITE TIMING FOR EMIFA AND EMIFB
(WITH WRITE LATENCY=1)
SEE NOTES 1,2 AND 3

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the programmable synchronous interface access signals are shown as generic (SADS/SRE, SOE, and SWE) instead of ASADS/ASRE, ASOE, and ASWE (for EMIFA) and BSADS/BSRE, BSOE, and BSWE (for EMIFB)].
2. The write latency and the length of CEx assertion are programmable via the SYNCWL and CEEXT fields, respectively, in the EMIFx CE Space Secondary Control register (CExSEC). In this figure, SYNCWL = 1 and CEEXT = 0.
3. The following parameters are programmable via the EMIF CE Space Secondary Control register (CExSEC):
   - Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
   - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
   - CEx assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, CEx goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, CEx is active when SOE is active (CEEXT = 1).
   - Function of SADS/SRE (RENEN): For standard SBSRAM or ZBT SRAM interface, SADS/SRE acts as SADS with deselect cycles (RENEN = 0). For FIFO interface, SADS/SRE acts as SRE with NO deselect cycles (RENEN = 1).
   - Synchronization clock (SNCCLK): Synchronized to ECLKOUT1 or ECLKOUT2.
4. ARE/SDCAS/SADS/SRE, AOE/SDRAS/SOE, and AWE/SDWE/SWE operate as SADS/SRE, SOE, and SWE, respectively, during programmable synchronous interface accesses.

FIGURE 5j. Test circuit and switching waveforms - Continued.

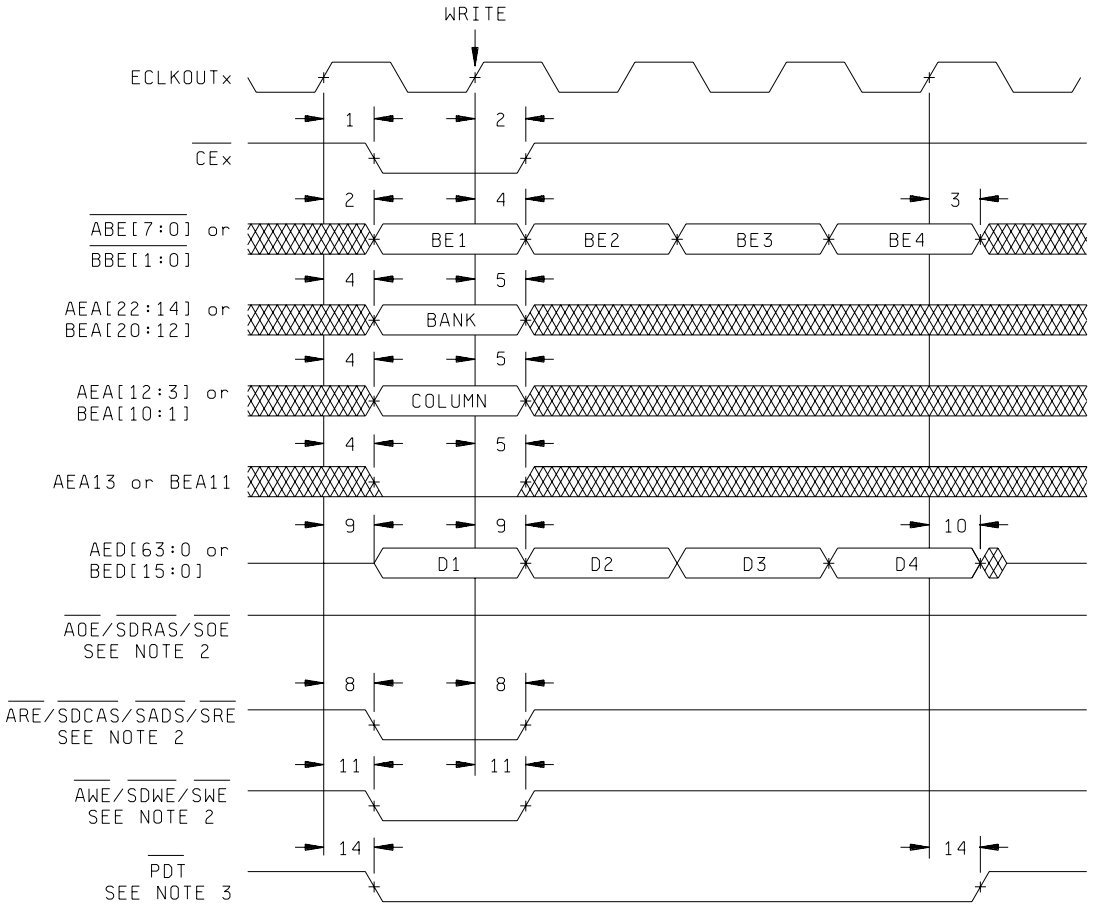


SDRAM READ COMMAND (CAS LATENCY 3) FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.
3. PDT signal is only asserted when the EDMA is in PDT mode (set the PDTS bit to 1 in the EDMA options parameter RAM). For PDT read, data is not latched into EMIF. The PDTRL field in the PDT control register (PDTCTL) configures the latency of the PDT signal with respect to the data phase of a read transaction. The latency of the PDT signal for a read can be programmed to 0, 1, 2, or 3 by setting PDTRL to 00, 01, 10, or 11, respectively. PDTRL equals 00 (zero latency) in this figure.

FIGURE 5k. Test circuit and switching waveforms.

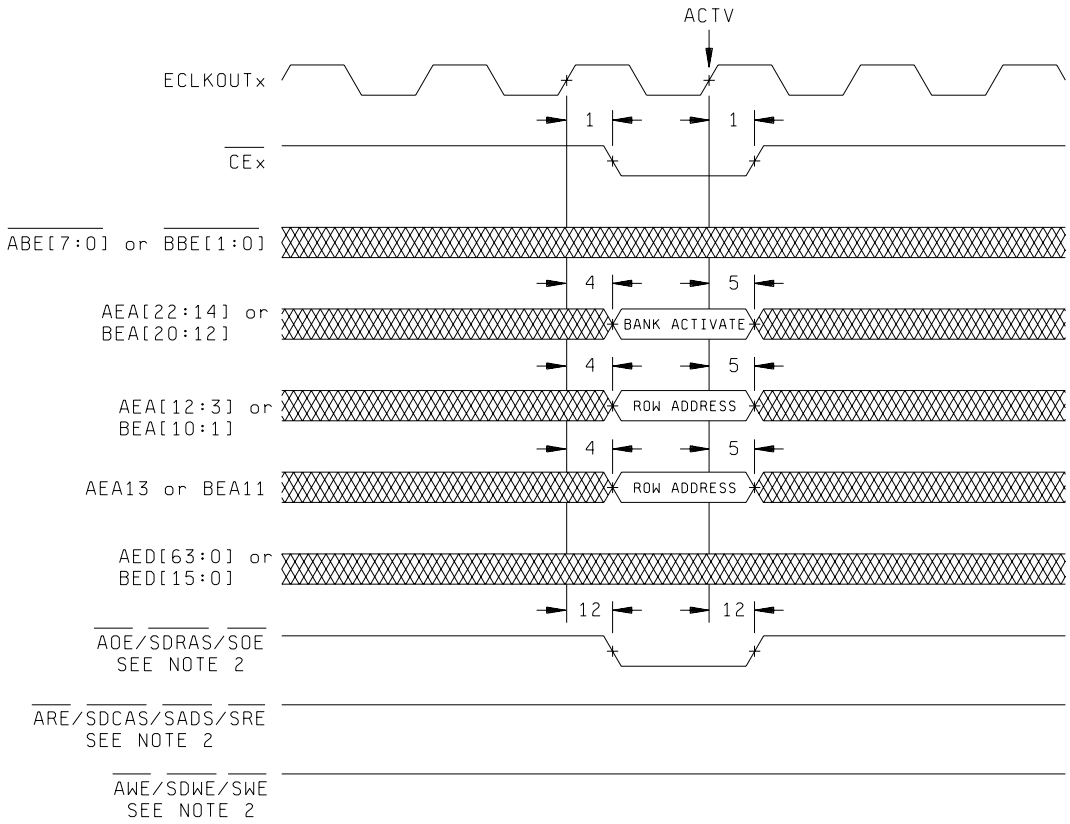


SDRAM WRITE COMMAND FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.
3. PDT signal is only asserted when the EDMA is in PDT mode (set the PDTS bit to 1 in the EDMA options parameter RAM). For PDT write, data is not driven (in High-Z). The PDTWL field in the PDT control register (PDTCTL) configures the latency of the PDT signal with respect to the data phase of a write transaction. The latency of the PDT signal for a write transaction can be programmed to 0, 1, 2, or 3 by setting PDTWL to 00, 01, 10, or 11, respectively. PDTWL equals 00 (zero latency) in this figure.

FIGURE 5k. Test circuit and switching waveforms - Continued.

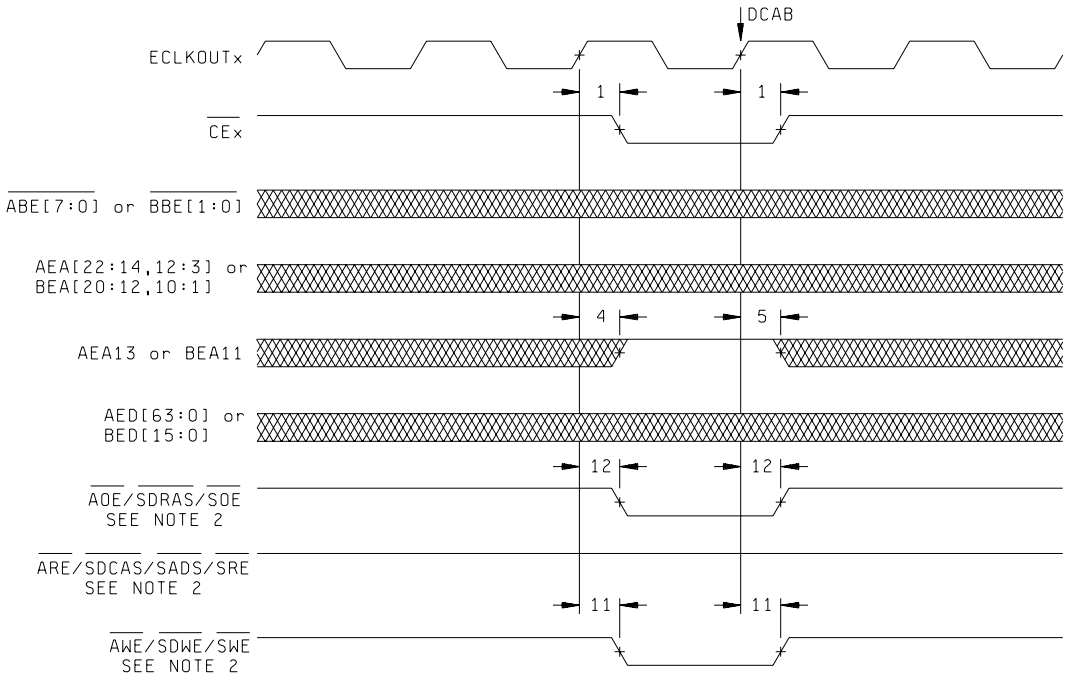


SDRAM ACTV COMMAND FOR EMIFA AND EMFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

FIGURE 5k. Test circuit and switching waveforms - Continued.

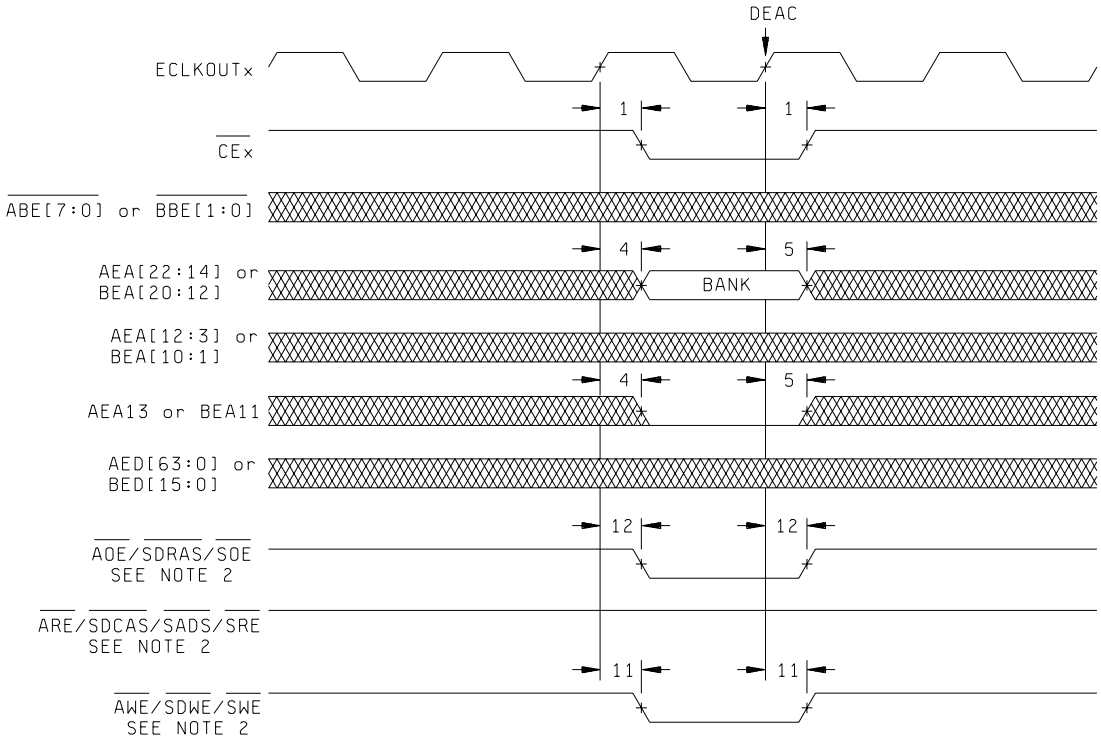


SDRAM DCAB COMMAND EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

FIGURE 5k. Test circuit and switching waveforms - Continued.

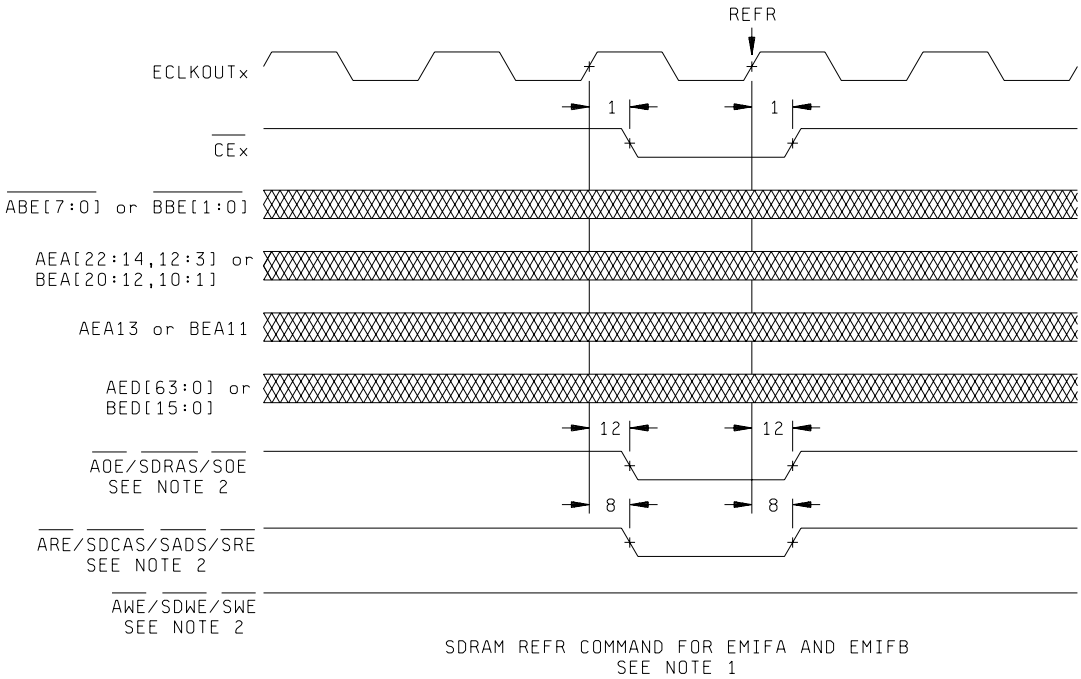


SDRAM DEAC COMMAND FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

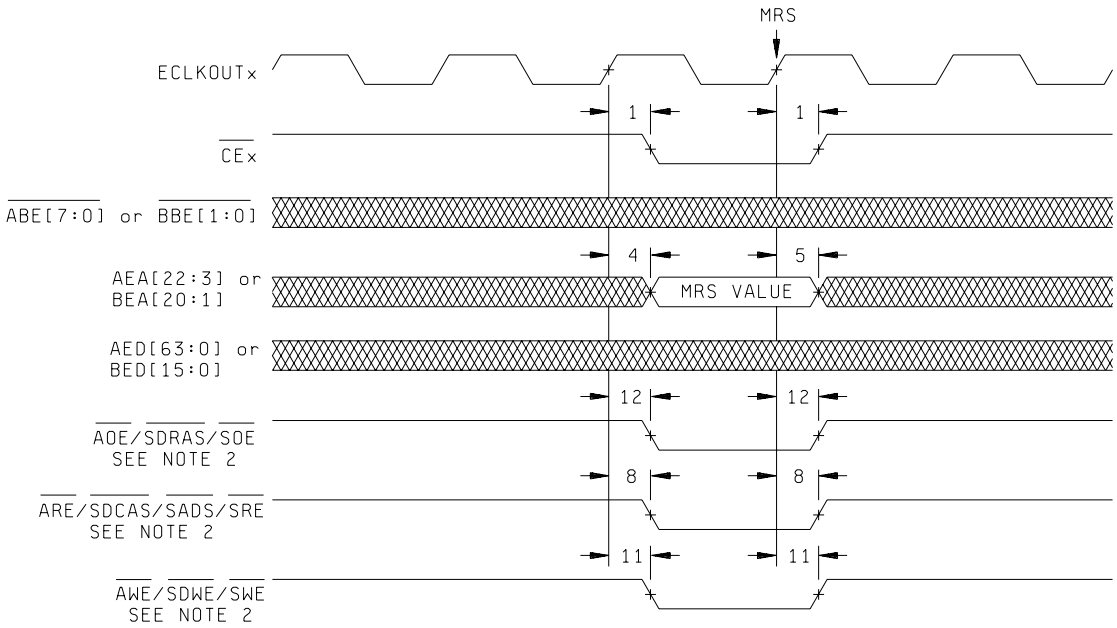
FIGURE 5k. Test circuit and switching waveforms - Continued.



NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

FIGURE 5k. Test circuit and switching waveforms - Continued.

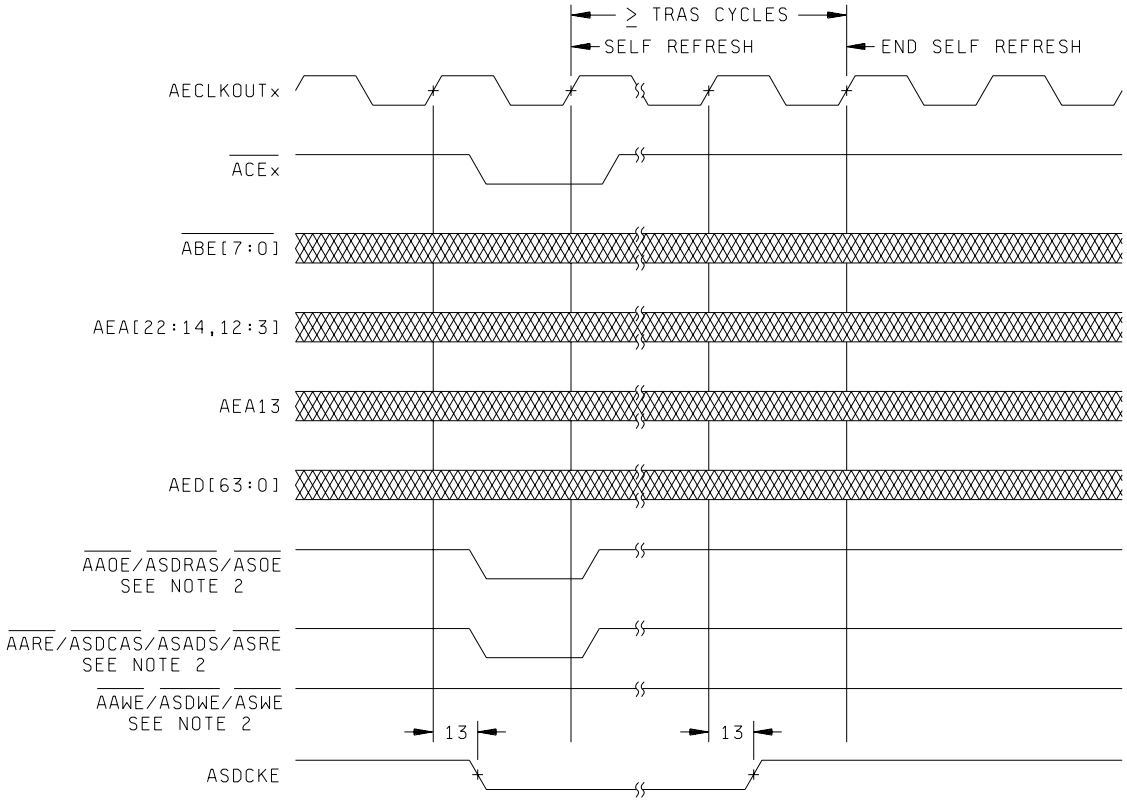


SDRAM MRS COMMAND FOR EMIFA AND EMIFB
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

FIGURE 5k. Test circuit and switching waveforms - Continued.

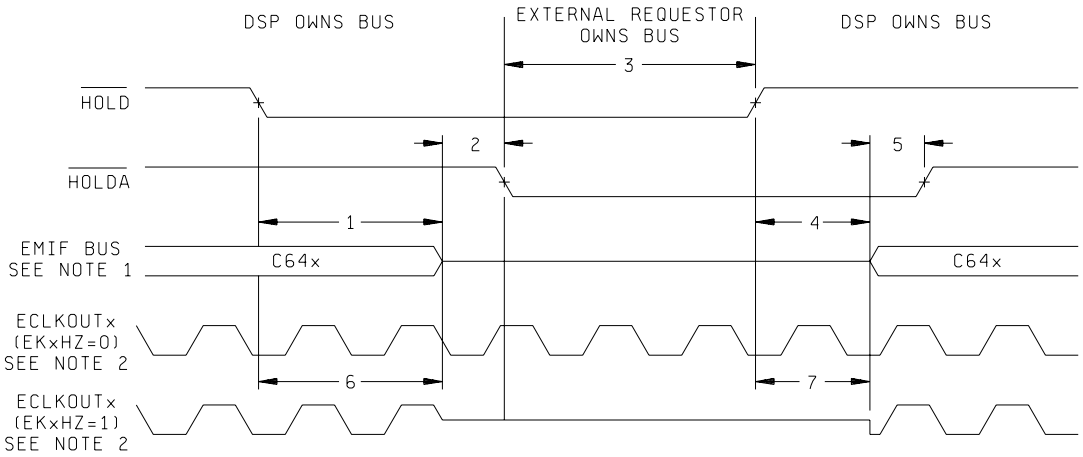


SDRAM SELF-REFRESH TIMING FOR EMIFA ONLY
SEE NOTE 1

NOTES:

1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic (SDCAS, SDWE, and SDRAS) instead of ASDCAS, ASDWE, and ASDRAS (for EMIFA) and BSDCAS, BSDWE, and BSDRAS (for EMIFB)].
2. ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

FIGURE 5k. Test circuit and switching waveforms - Continued.

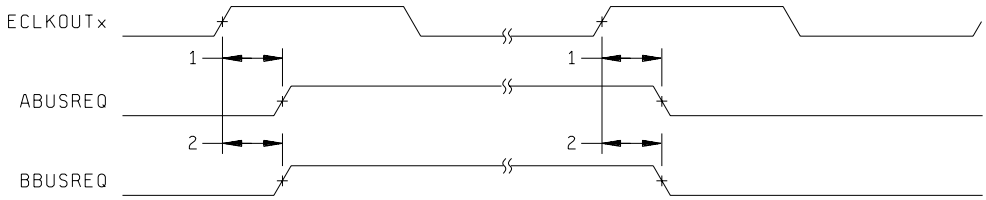


HOLD/HOLDA TIMING FOR EMIFA AND EMIFB

NOTES:

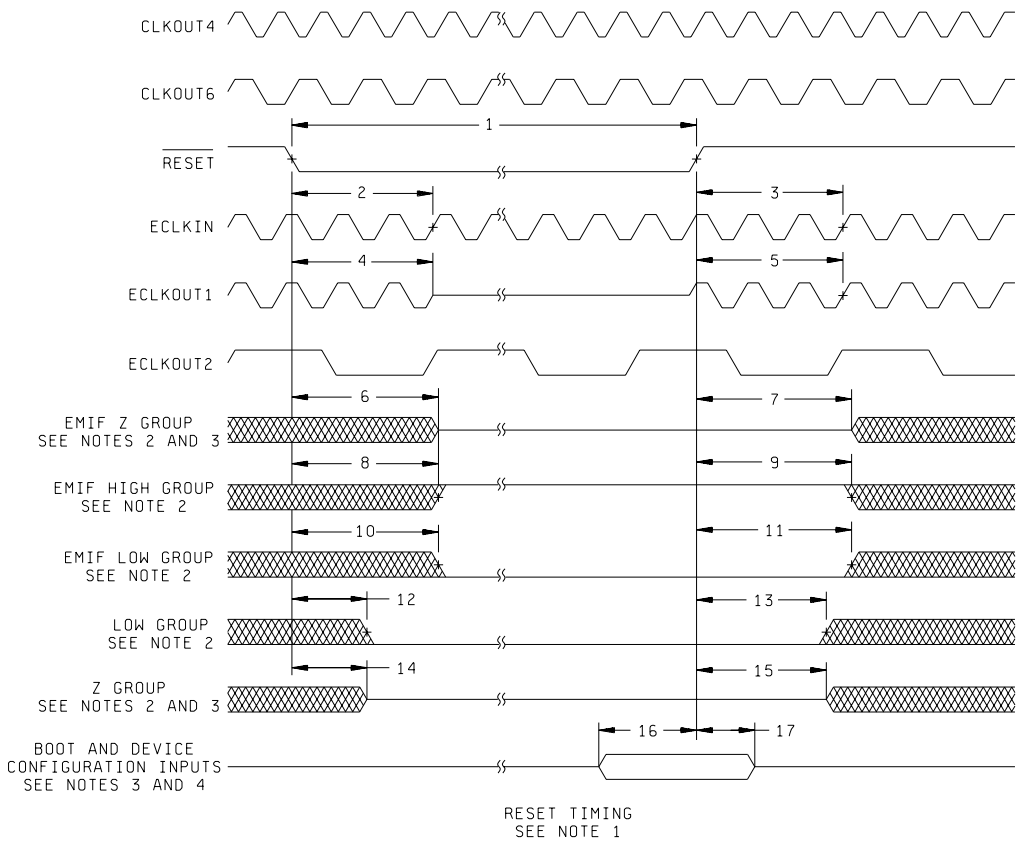
1. For EMIFA, EMIF Bus consists of: ACE[3:0], ABE[7:0], AED[63:0], AEA[22:3], AARE/ASDCAS/ASADS/ASRE, AAOE/ASDRAS/ASOE, and AAWE/ASDWE/ASWE, ASDCKE, ASOE3, and APDT.
   For EMIFB, EMIF Bus consists of: BCE[3:0], BBE[1:0], BED[15:0], BEA[20:1], BARE/BSDCAS/BSADS/BSRE, BAOE/BSDRAS/BSOE, and BAWE/BSDWE/BSWE, BSOE3, and BPDT.
2. The EkxHZ bits in the EMIF Global Control register (GBLCTL) determine the state of the ECLKOUTx signals during HOLDA. If EkxHZ = 0, ECLKOUTx continues clocking during Hold mode. If EkxHZ = 1, ECLKOUTx goes to high impedance during Hold mode, as shown in this figure.

FIGURE 5m. Test circuit and switching waveforms.



BUSREQ TIMING FOR EMIFA AND EMIFB

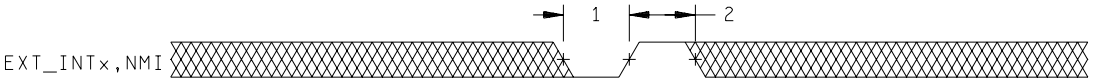
FIGURE 5n. Test circuit and switching waveforms.



NOTES:

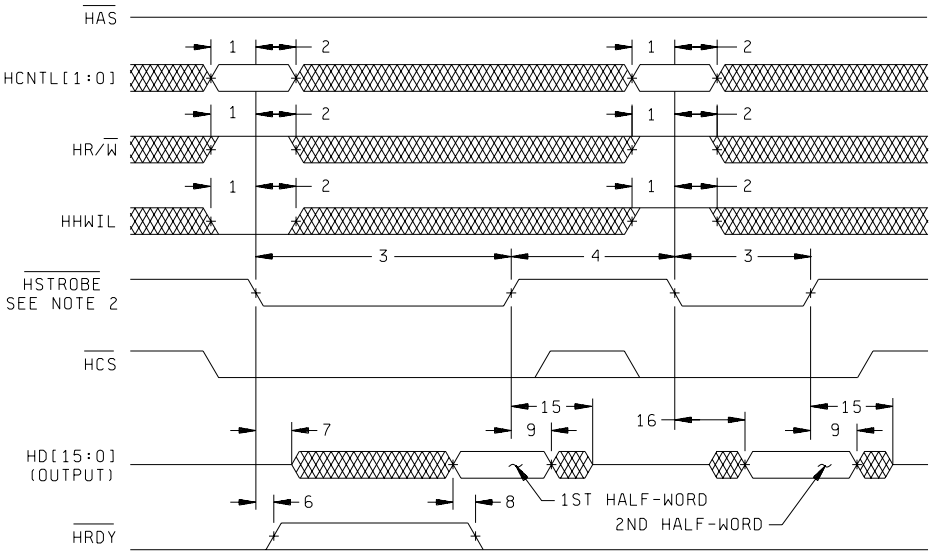
1. These C64x™ devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, the prefix “A” or “B” may be omitted [e.g., ECLKIN, ECLKOUT1, and ECLKOUT2].
2. EMIF Z group consists of: AEA[22:3], BEA[20:1], AED[63:0], BED[15:0], CE[3:0], ABE[7:0], BBE[1:0], ARE/SDCAS/SADS/SRE, AWE/SDWE/SWE, and AOE/SDRAS/SOE, SOE3, ASDCKE, and PDT.
   EMIF high group consists of: AHOLDA and BHOLDA (when the corresponding HOLD input is high).
   EMIF low group consists of: ABUSREQ and BBUSREQ; AHOLDA and BHOLDA (when the corresponding HOLD input is low).
   Low group consists of: XSP_CS, CLKX2/XSP_CLK, and DX2/XSP_DO; all of which apply only when PCI EEPROM (BEA13) is enabled (with PCI_EN = 1 and MCBSP2_EN = 0). Otherwise, the CLKX2/XSP_CLK and DX2/XSP_DO pins are in the Z group.
   Z group consists of: HD[31:0]/AD[31:0], CLKX0, CLKX1/URADDR4, CLKX2/XSP_CLK, FSX0, FSX1/UXADDR3, FSX2, DX0, DX1/UXADDR4, DX2/XSP_DO, CLKR0, CLKR1/URADDR2, CLKR2, FSR0, FSR1/UXADDR2, FSR2, TOUT0, TOUT1, TOUT2, GP[8:0], GP10/PCBE3, HR/W/PCBE2, HDS2/PCBE1, PCBE0, GP13/PINTA, GP11/PREQ, HDS1/PSERR, HCS/PPERR, HCNTL1/PDEVSEL, HAS/PPAR, HCNTL0/PSTOP, HHWIL/PTRDY (16-bit HPI mode only), HRDY/PIRDY, HINT/PFRAME, UXDATA[7:0], UXSOC, UXCLAV, and URCLAV.
3. If BEA[20:13, 11, 7] and HD5/AD5 pins are actively driven, care must be taken to ensure no timing contention between parameters 6, 7, 14, 15, 16, and 17.
4. Boot and Device Configurations Inputs (during reset) include: EMIFB address pins BEA[20:13, 11, 7] and HD5/AD5. The PCI_EN pin *must* be driven valid at all times and the user *must not* switch values throughout device operation. The MCBSP2_EN pin *must* be driven valid at all times and the user *can* switch values throughout device operation.

FIGURE 5p. Test circuit and switching waveforms.

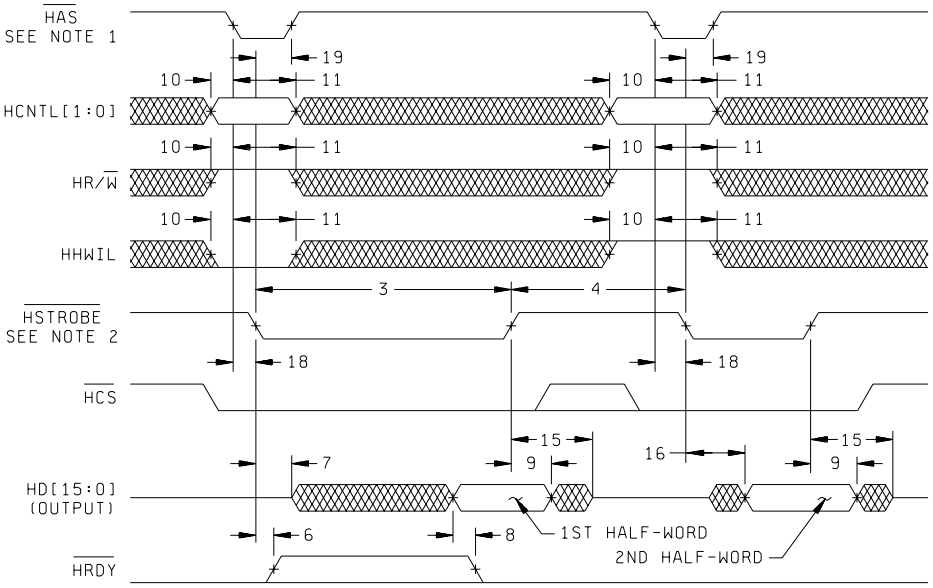


EXTERNAL/NMI INTERRUPT TIMING

FIGURE 5q. Test circuit and switching waveforms.



HPI16 READ TIMING (HAS NOT USED,TIED HIGH)

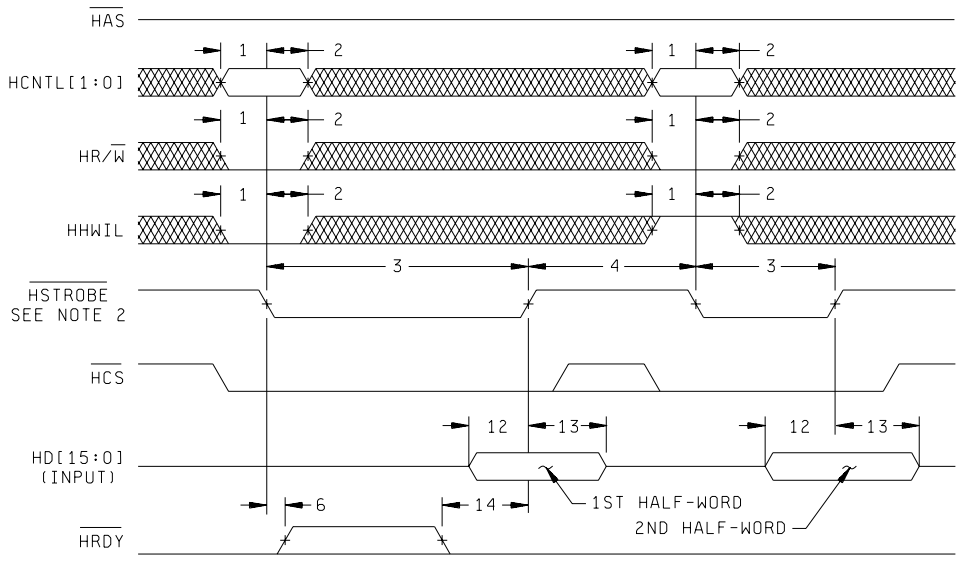


HPI16 READ TIMING (HAS USED)

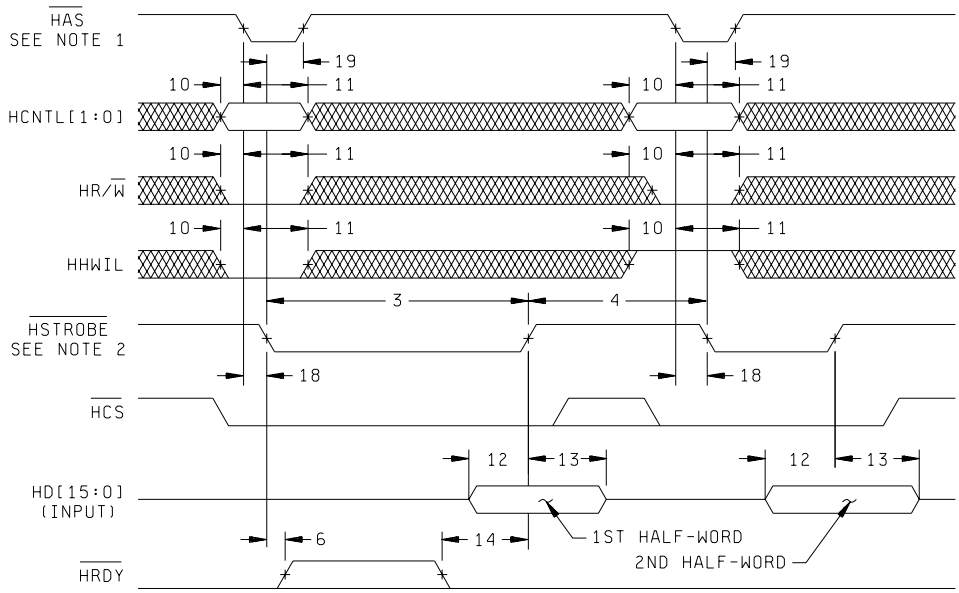
NOTES:

1. For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
2. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

FIGURE 5r. Test circuit and switching waveforms.



HPI16 WRITE TIMING (HAS NOT USED,TIED HIGH)

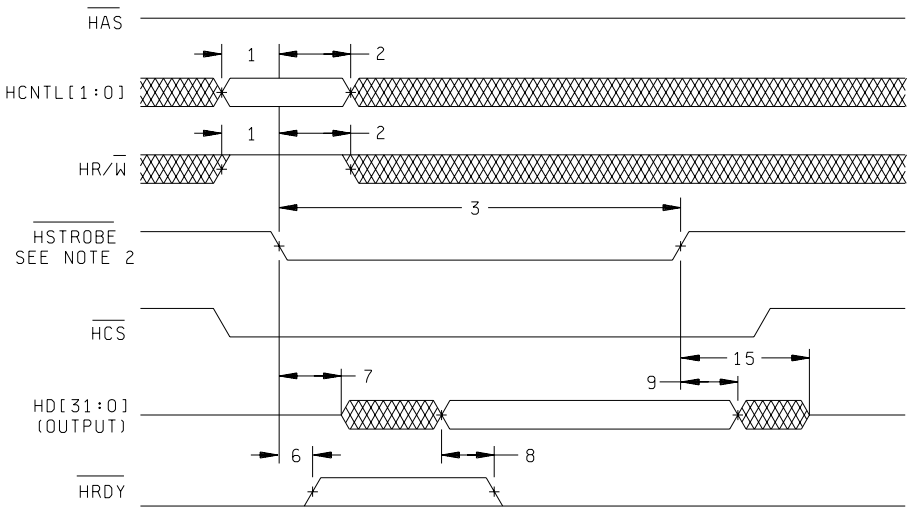


HPI16 WRITE TIMING (HAS USED)

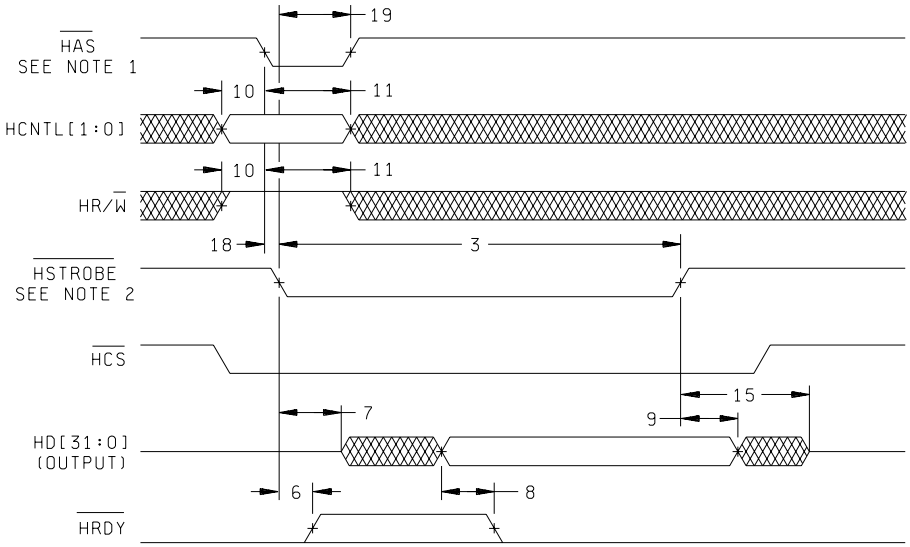
NOTES:

1. For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
2. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

FIGURE 5r. Test circuit and switching waveforms - Continued.



HP132 READ TIMING (HAS NOT USED,TIED HIGH)

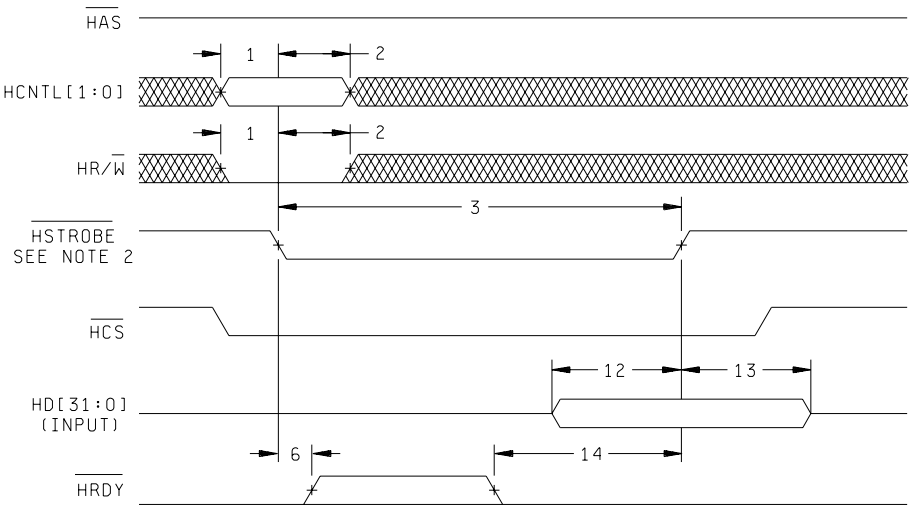


HP132 READ TIMING (HAS USED)

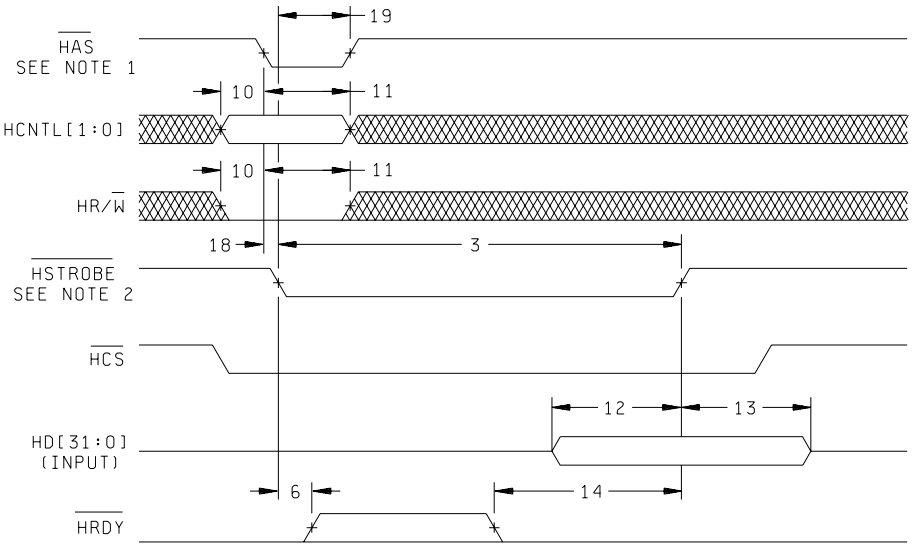
NOTES:

1. For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
2. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

FIGURE 5r. Test circuit and switching waveforms - Continued.



HP132 WRITE TIMING (HAS NOT USED,TIED HIGH)



HP132 WRITE TIMING (HAS USED)

NOTES:

1. For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
2. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

FIGURE 5r. Test circuit and switching waveforms - Continued.

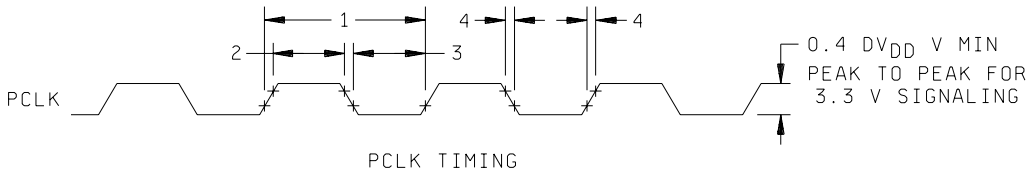


FIGURE 5t. Test circuit and switching waveforms.

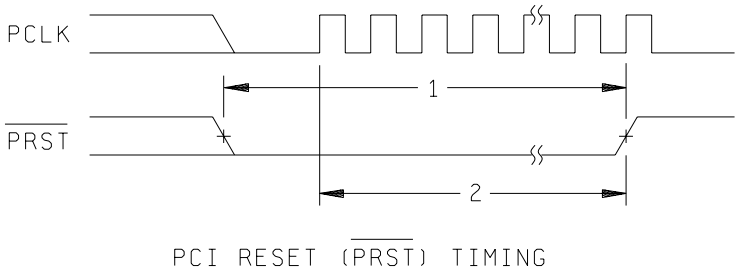


FIGURE 5u. Test circuit and switching waveforms.

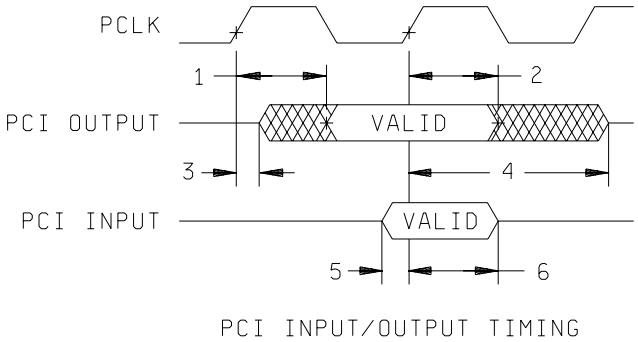


FIGURE 5v. Test circuit and switching waveforms.

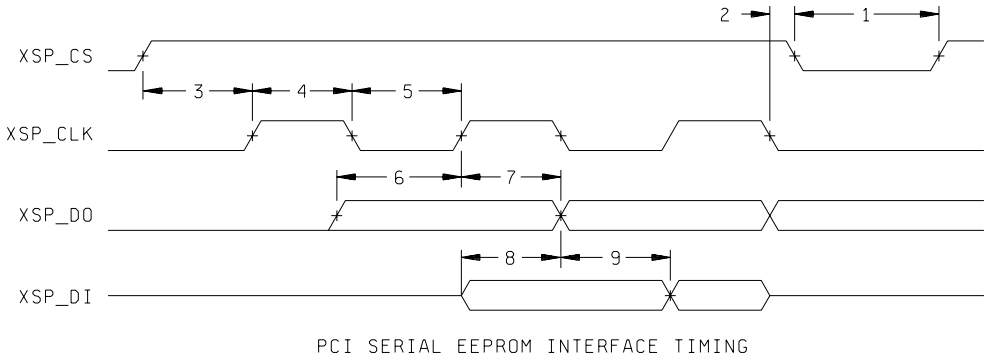


FIGURE 5w. Test circuit and switching waveforms.

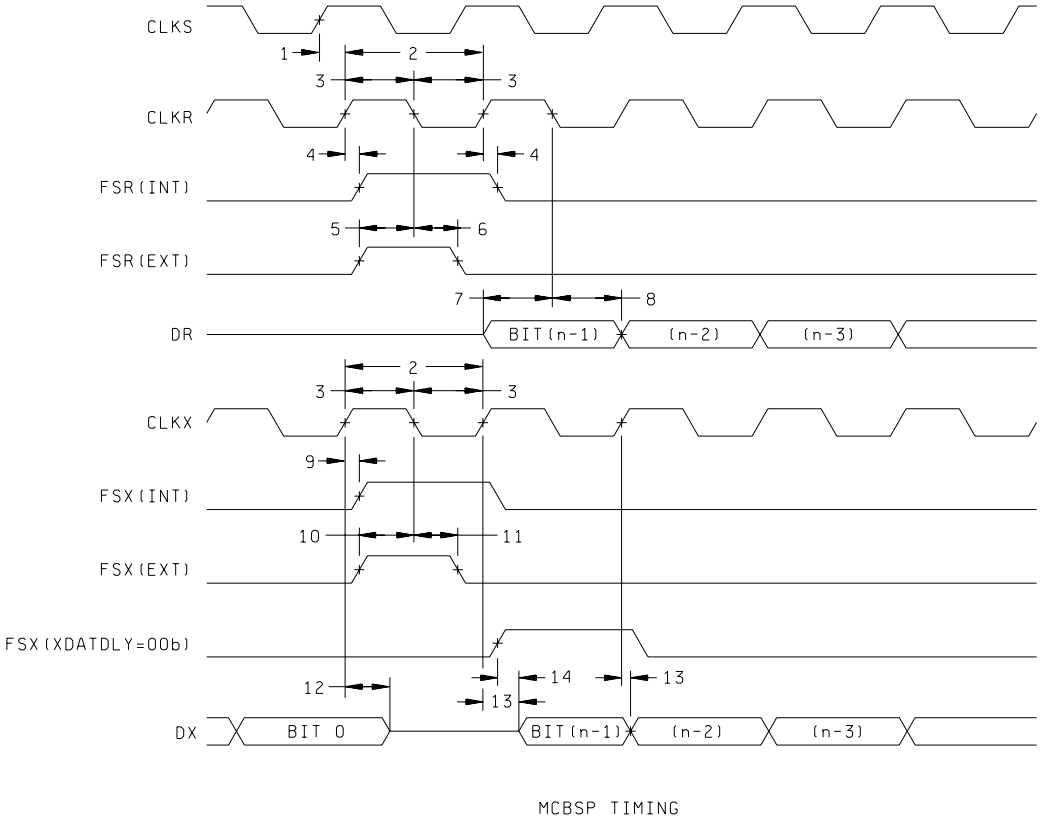


FIGURE 5x. Test circuit and switching waveforms.

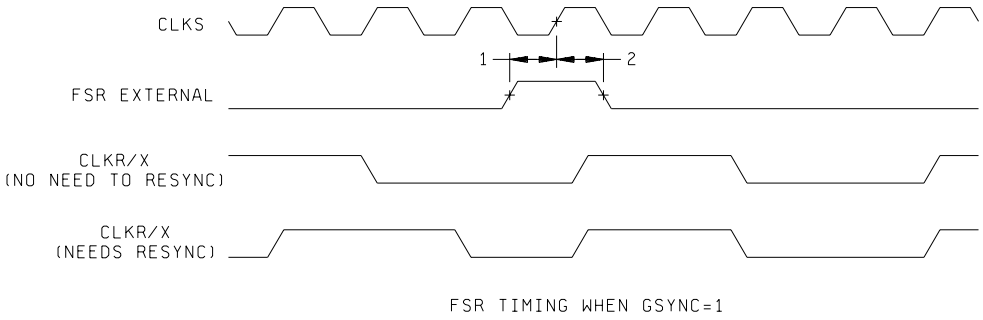


FIGURE 5y. Test circuit and switching waveforms.

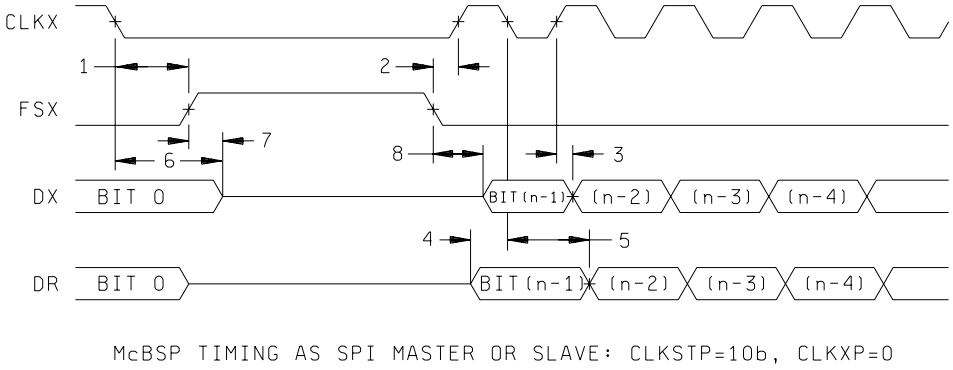


FIGURE 5z. Test circuit and switching waveforms.

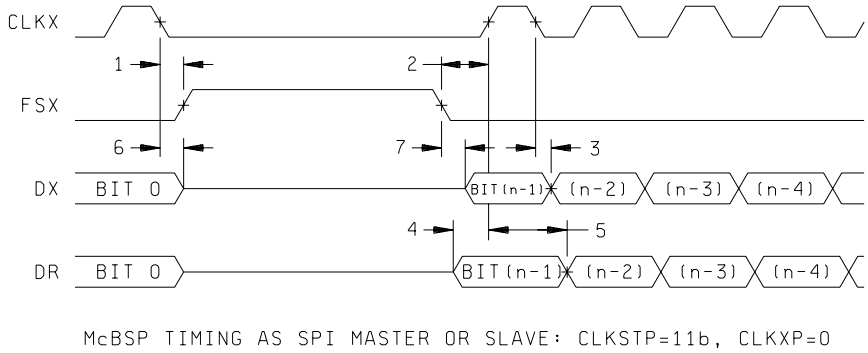


FIGURE 5aa. Test circuit and switching waveforms.

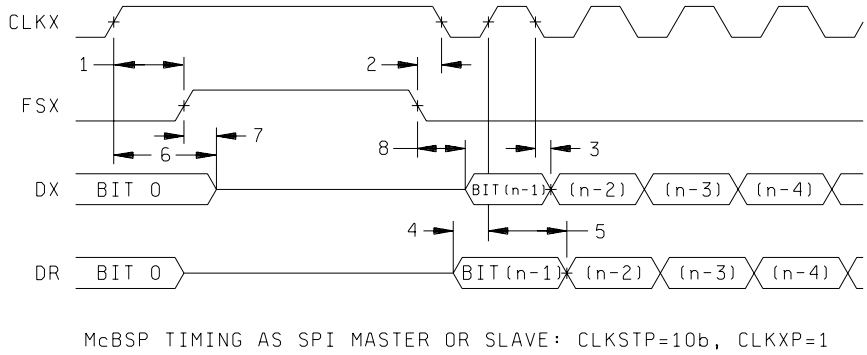


FIGURE 5bb. Test circuit and switching waveforms.

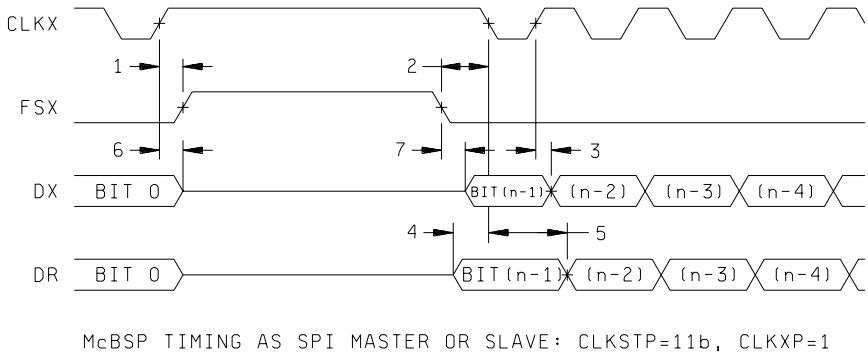


FIGURE 5cc. Test circuit and switching waveforms.

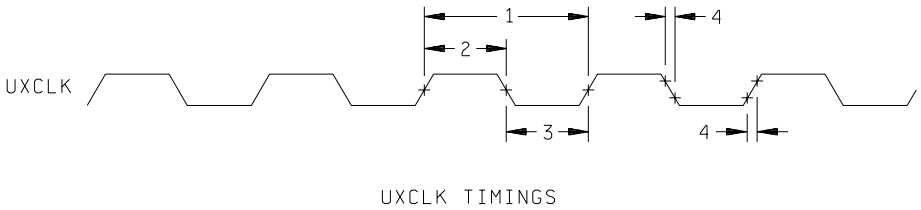


FIGURE 5dd. Test circuit and switching waveforms.

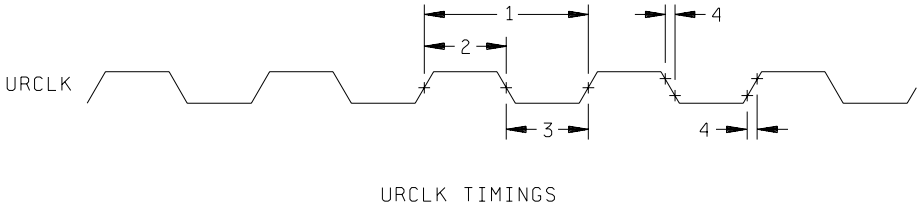
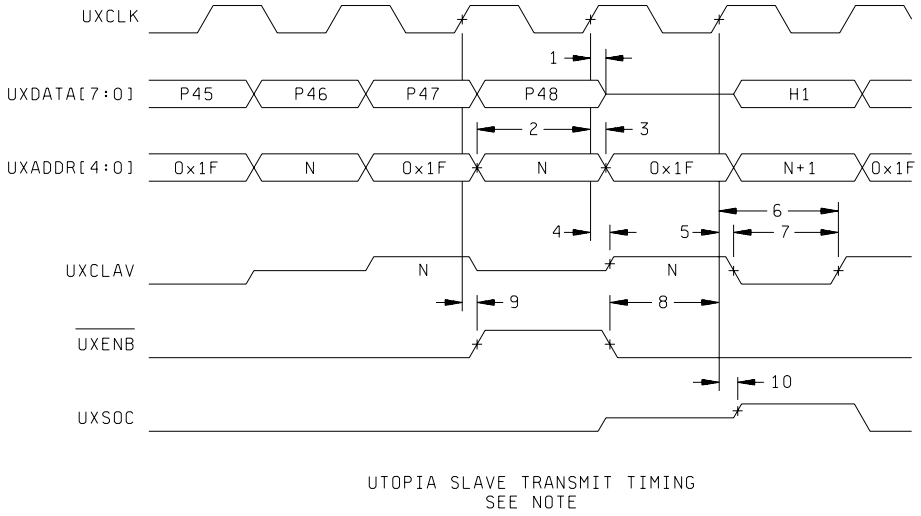
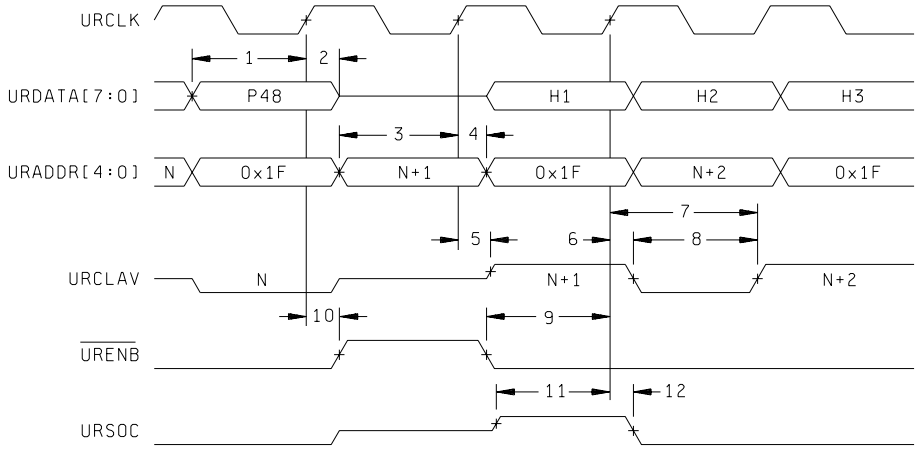


FIGURE 5ee. Test circuit and switching waveforms.



NOTE: The UTOPIA Slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the UXCLAV and UXSOC signals).

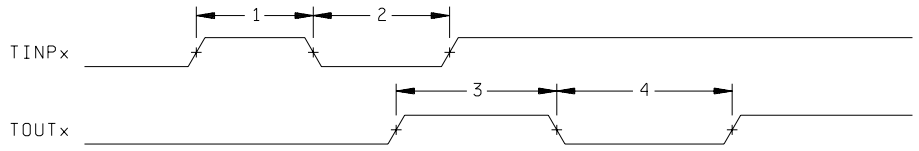
FIGURE 5ff. Test circuit and switching waveforms.



UTOPIA SLAVE RECEIVE TIMING

NOTE: The UTOPIA Slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the URCLAV and URSOC signals).

FIGURE 5gg. Test circuit and switching waveforms.



TIMER TIMING

FIGURE 5hh. Test circuit and switching waveforms.

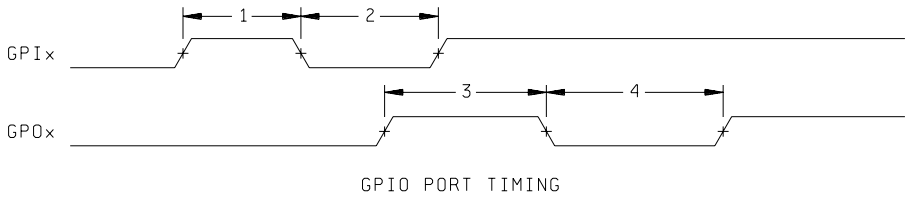


FIGURE 5jj. Test circuit and switching waveforms.

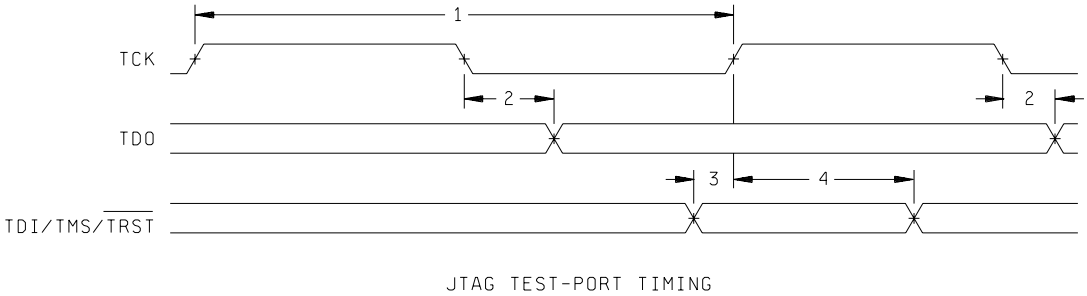


FIGURE 5kk. Test circuit and switching waveforms.

Instruction Name	Instruction Code
IDCODE	00100101
EXTEST	00000000
BYPASS	11111111
SAMPLE	00000001

FIGURE 6. Boundary scan instruction codes.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of 5 devices with zero rejects shall be required.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-11-03

Approved sources of supply for SMD 5962-03245 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0324501QXA	01295	SMJ320C6415DGADW60

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.