REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add footnote 4/ in 1.5. Add footnote 2/ and make changes to I_{DCHG} test in table I. - rrp	03-06-17	R. MONNIN
B	Add new footnote under 1.3 and 1.4. Add footnote 3/ to Table I. Make changes to the conditions column for V_{LINE}, V_{OM}, F_{PSRR}, F_{OM}, PSRR, and I_{SU} tests as specified under Table I. Make corrections to figure 2 and figure 3. Add paragraph 4.4.4.2. - ro	06-04-05	R. MONNIN
C	Make change to the Charge current test subgroup 3 maximum limit as specified under Table I. - ro	07-11-20	R. HEBER
D	Add device type 02. Make changes to 1.2.2, 1.5, Table I, figure 1, figure 2, Table IIB, and Appendix A. - ro	08-01-29	R. HEBER
E	Correct logic diagram in figure 2. -rrp	08-12-03	R. HEBER
F	Make corrections to figure 3 Irradiation connections. Add Table IB. Make corrections to 4.4.4.2. - ro	10-12-13	C. SAFFLE
G	Add "Analog inputs" parameter under paragraph 1.3, absolute maximum ratings. Add paragraph 6.7. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. - ro	11-02-15	C. SAFFLE
H	Add device types 03, 04, and 05. Delete radiation exposure circuit. Add Clock out to PWM switching delay (t_{PWM}) test under Table IA and timing diagram. Add subgroups 9, 10, and 11 to Table IIA. Update paragraph 2.2. - ro	12-08-22	C. SAFFLE
J	Add device class T to device type 01. - ro	13-08-19	C. SAFFLE

REV																				
SHEET																				
REV	J	J	J	J	J	J	J	J												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
02-02-06

REVISION LEVEL
J

MICROCIRCUIT, LINEAR, RADIATION HARDENED, HIGH SPEED, DUAL OUTPUT PULSE WIDTH MODULATOR WITH SEU PROTECTION, MONOLITHIC SILICON

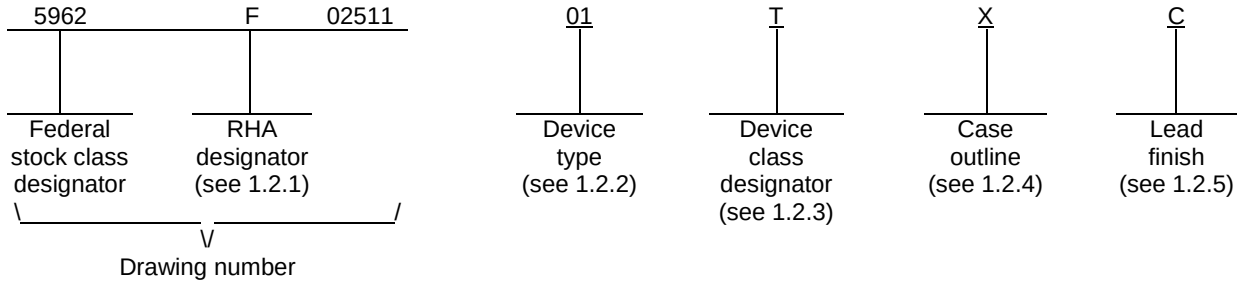
SIZE	CAGE CODE	
A	**67268**	**5962-02511**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	IS-1825ASRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
02	ISL71823ASRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
03	IS-1825BSRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
04	ISL71823BSRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
05	IS-1825BSEH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
X	CDFP4-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage (V_{CC} and V_C) 4/ ..... 35 V dc
Analog inputs (INV, NON-INV, RAMP, ILIM/SD, SOFT START) ..... -0.3 V to V_{CC} + 0.3 V
Power dissipation (P_D) ..... 714 mW
Junction temperature (T_J) ..... +175°C maximum
Lead temperature (soldering, 10 seconds) ..... +260°C maximum
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}):
Case E ..... 18°C/W
Case X ..... 15°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
Case E ..... 70°C/W
Case X ..... 80°C/W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage (V_{CC} and V_C) 4/ ..... 12 V to 20 V
Ambient operating temperature range (T_A) ..... -50°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and ambient temperature range of -50°C to +125°C unless otherwise noted.
4/ V_{CC} and V_C must be at the same potential.

1.5 Radiation features:

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device types 01, 02, 03, 04:
Device classes Q or V ..... 300 krads(Si) 5/
Device class T ..... 100 krads(Si) 5/
Device type 05 ..... 300 krads(Si) 6/

Maximum total dose available (dose rate ≤ 0.01 rads(Si)/s):
Device type 05 ..... 50 krads(Si) 6/

Single event phenomena (SEP):
No Single event latch-up (SEL) occurs at effective LET (see 4.4.4.3) ..... ≤ 87.4 MeV/(mg/cm^2) 7/
No Single event burn out (SEB) occurs at effective LET (see 4.4.4.3) ..... ≤ 87.4 MeV/(mg/cm^2) 8/
Single event transients (SET) observed at an effective LET (see 4.4.3) ..... ≤ 35 MeV / (mg/cm^2) 8/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

_____
5/ Device types 01, 02, 03, and 04 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for classes Q or V and 100 krads(Si) for class T.
6/ Device type 05 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).
7/ Devices 01, 02, 03, 04, and 05 use dielectrically isolated (DI) technology and latch up is physically not possible.
8/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact manufacturer.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-50°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Reference section.							
Output voltage	V_{REF}		01, 02,	1	5.00	5.20	V
			03, 04, 05	2,3	4.920	5.28	
		M,D,P,L,R,F		1	4.920	5.28	
Line regulation	V_{LINE}	$12 V < V_S < 20 V$ 3/	01, 02,	1	-15	15	mV
			03, 04, 05	2,3	-20	20	
		M,D,P,L,R,F		1	-20	20	
Load regulation	V_{LOAD}	$1 mA < I_{OUT} < 10 mA$	01, 02,	1	-25	25	mV
			03, 04, 05	2,3	-50	50	
		M,D,P,L,R,F		1	-50	50	
Total output variation	V_{OM}	V_S = 12 V, 20 V, 3/	01, 02,	1	5.00	5.20	V
		I_L = 1 mA, 10 mA	03, 04, 05	2,3	4.92	5.28	
		M,D,P,L,R,F		1	4.92	5.28	
Short circuit current	I_{SC}	V_{REF} = 0 V	01, 02,	1	30		mA
			03, 04, 05	2,3	20		
		M,D,P,L,R,F		1	20		
Oscillator section.							
Initial accuracy	F_O		01, 02,	4	340	425	kHz
			03, 04, 05	5,6	300	425	
		M,D,P,L,R,F		4	300	425	
Voltage stability	F_{PSRR}	$12 V < V_S < 20 V$ 3/	01, 02,	4	-3	3	%
			03, 04, 05	5,6	-5	5	
		M,D,P,L,R,F		4	-3	3	
Total variation	F_{OM}	V_S = 12 V, 20 V 3/	01, 02,	4	340	425	kHz
			03, 04, 05	5,6	300	425	
		M,D,P,L,R,F		4	300	425	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. – Continued.

Test	Symbol	Conditions 1/ 2/ $-50°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Oscillator section – continued.							
Clock out high voltage	V_{CLKH}		01, 02,	1	4.0		V
			03, 04, 05	2,3	3.75		
		M,D,P,L,R,F		1	3.75		
Clock out low voltage	V_{CLKL}		01, 02,	1,2,3		0.2	V
		M,D,P,L,R,F	03, 04, 05	1		0.2	
Error amplification section.							
Input offset voltage	V_{OS}	V_{CM} = 3.0 V, V_O = 3.0 V	01, 02,	1,2,3	-10	10	mV
		M,D,P,L,R,F	03, 04, 05	1	-10	10	
Input bias current	I_{IB}	V_{CM} = 3.0 V, V_O = 3.0 V	01, 02,	1,2,3	-2	2	µA
		M,D,P,L,R,F	03, 04, 05	1	-2	2	
Input offset current	I_{OS}	V_{CM} = 3.0 V, V_O = 3.0 V	01, 02,	1,2,3	-2	2	µA
		M,D,P,L,R,F	03, 04, 05	1	-2	2	
Open loop gain	A_{VOL}	1 V < V_O < 4 V	01, 02,	4,5,6	60		dB
		M,D,P,L,R,F	03, 04, 05	4	60		
Common mode rejection ratio	CMRR	1.5 V < V_{CM} < 4.0 V	01, 02,	4	65		dB
			03, 04, 05	5,6	45		
		M,D,P,L,R,F		4	65		
Power supply rejection ratio	PSRR	12 V < V_S < 20 V 3/	01, 02,	4,5,6	70		dB
		M,D,P,L,R,F	03, 04, 05	4	70		
Output sink current	I_{OL}	$V_{E/A\ OUT}$ = 1.0 V	01, 02,	1,2,3	1		mA
		M,D,P,L,R,F	03, 04, 05	1	1		
Output source current	I_{OH}	$V_{E/A\ OUT}$ = 4.0 V	01, 02,	1,2,3	-0.5		mA
		M,D,P,L,R,F	03, 04, 05	1	-0.5		
Output high voltage	V_{OH1}	$I_{E/A\ OUT}$ = -0.5 mA	01, 02,	1,2,3	4.0		V
		M,D,P,L,R,F	03, 04, 05	1	4.0		
Output low voltage	V_{OL1}	$I_{E/A\ OUT}$ = 1 mA	01, 02,	1,2,3		1.0	V
		M,D,P,L,R,F	03, 04, 05	1		1.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. – Continued.

Test	Symbol	Test conditions 1/ 2/ $-50°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Pulse width modulator (PWM) comparator section.							
Ramp bias current	I_{RAMP}	V_{RAMP} = 0 V	01, 02,	1,2,3		-8	µA
		M,D,P,L,R,F	03, 04, 05	1		-8	
Duty cycle range	DC_{max}		01, 03, 05	4,5,6	40		%
		M,D,P,L,R,F		4	40		
			02, 04	4,5,6	80		
		M,D,P,L,R,F		4	80		
E/A out zero DC threshold voltage	$RAMP_{offset}$	Ramp voltage = 0 V	01, 02,	1,2,3	0.81		V
		M,D,P,L,R,F	03, 04, 05	1	0.81		
Clock out to PWM switching delay	t_{PWM}	See figure 3.	03, 04, 05	9	200	380	µs
				10	400	660	
				11	100	278	
		M,D,P,L,R,F		9	200	380	
Soft start section.							
Charge current	I_{CHG}	Soft start voltage = 2.5 V	01, 02,	1	8	20	µA
			03, 04, 05	2	8	25	
				3	8	29	
		M,D,P,L,R,F		1	8	25	
Discharge current	I_{DCHG}	Soft start voltage = 2.5 V	01, 02,	1,2,3	0.1	0.50	mA
		M,D,P,L,R,F	03, 04, 05	1	0.1	0.50	
Current limit / Start sequence / Fault section.							
Restart threshold	V_{RS}		01, 02,	1,2,3		0.5	V
		M,D,P,L,R,F	03, 04, 05	1		0.5	
ILIM bias current	I_{BLIM}	$0 < V_{ILIM} < 2$ V	01, 02,	1,2,3		15	µA
		M,D,P,L,R,F	03, 04, 05	1		15	
Current limit threshold	V_{LIMIT}		01, 02,	1,2,3	0.85	1.15	V
		M,D,P,L,R,F	03, 04, 05	1	0.85	1.15	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-50°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Current limit / Start sequence / Fault section – continued.							
Over current threshold	VOVER		01, 02, 03, 04, 05	1,2,3	1.05	1.26	V
		M,D,P,L,R,F		1	1.05	1.26	
Output section.							
Output low saturation 1	V_{SATL1}	I_{OUT} = 20 mA	01, 02,	1		0.8	V
			03, 04, 05	2,3		1.0	
		M,D,P,L,R,F		1		0.8	
Output low saturation 2	V_{SATL2}	I_{OUT} = 200 mA	01, 02,	1,2,3		2.2	V
		M,D,P,L,R,F	03, 04, 05	1		2.2	
Output high saturation 1	V_{SATH1}	I_{OUT} = 20 mA	01, 02,	1,2,3	10		V
		M,D,P,L,R,F	03, 04, 05	1	10		
Output high saturation 2	V_{SATH2}	I_{OUT} = 200 mA	01, 02,	1,2,3	9		V
		M,D,P,L,R,F	03, 04, 05	1	9		
Under voltage lockout (UVLO) output low saturation voltage	$UVLO_{OLS}$	I_O = 20 mA	01, 02, 03, 04, 05	1,2,3		1.2	V
		M,D,P,L,R,F		1		1.2	
Under voltage section.							
Start threshold voltage	V_{START}		01, 02,	1,2,3	8.2	8.8	V
		M,D,P,L,R,F	03, 04, 05	1	8.2	8.8	
Stop threshold voltage	V_{STOP}		01, 02,	1,2,3	7.6	8.4	V
		M,D,P,L,R,F	03, 04, 05	1	7.6	8.4	
Under voltage lockout (UVLO) hysteresis	V_{HYS}		01, 02,	1,2,3	0.3	1.2	V
		M,D,P,L,R,F	03, 04, 05	1	0.3	1.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-50°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Supply current section.							
Startup current	I_{SU}	V_S = 8.0 V 3/	01, 02,	1,2,3		300	µA
		M,D,P,L,R,F	03, 04, 05	1		300	
Supply current	I_{CC}	Inverting input, RAMP, and current LIM / SD voltage = 0 V, Non-inverting input voltage = 1.0 V	01, 02, 03, 04, 05	1,2,3		36	mA
		M,D,P,L,R,F		1		36	

1/ Unless otherwise specified, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = V_C = 12 V.

2/ RHA device types 01, 02, 03, and 04 supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation for device classes Q or V and levels M, D, P, L, and R of irradiation for device class T. However, device types 01, 02, 03, and 04 are only tested at the "F" level for device classes Q or V and the "R" level for device class T in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein). Device types 01, 02, 03, and 04 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects.

RHA device type 05 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and irradiation of M, D, P, and L level for condition D. However, device type 05 is only tested at the "F" level in accordance with MIL-STD-883, method 1019, condition A, and tested at the "L" level in condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ $V_S = V_C = V_{CC}$. Both V_{CC} and V_C must be at the same potential.

TABLE IB. SEP test limits. 1/ 2/ 3/

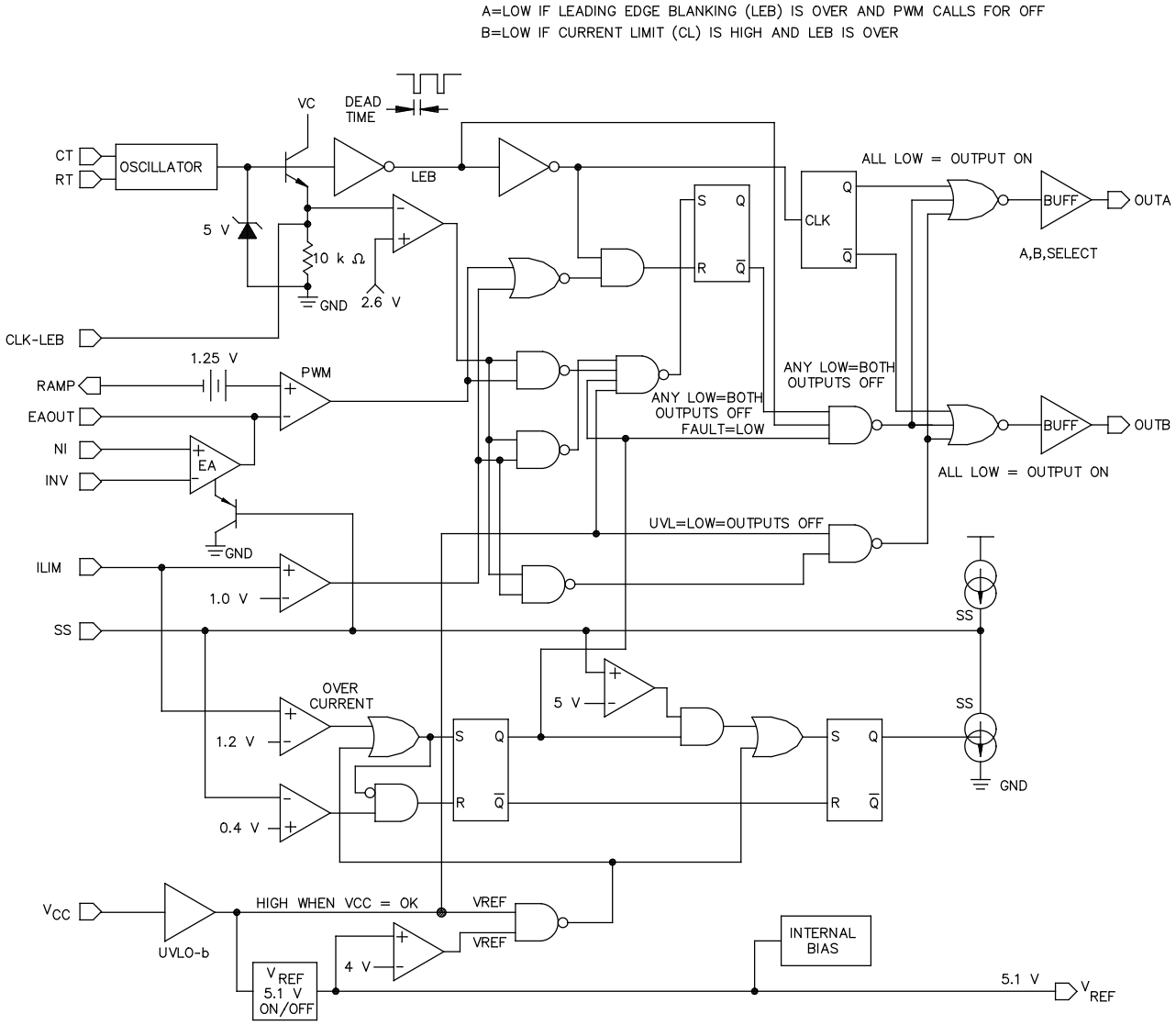
Device type	SEP	Temperature (T_C)	Bias V_{IN}	Effective Linear energy transfer (LET) [MeV/mg/cm^2]	Fluence/cross section
01, 02, 03, 04, 05	No SEL	+125°C	20 V	LET ≤ 87.4	
	No SEB	+125°C	20 V	LET ≤ 87.4	Fluence = 1 x 10^7 ions/cm^2
	SET observed	+25°C	12 V	LET = 35	4/

1/ For SEP test conditions, see 4.4.4.3 herein. For more information on SEP test results, customers are requested to contact manufacturer.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested. See manufacturer's SEE test report for more information.
4/ The destructive SEP (SEL/SEB) test performed at heavy ion facility using Gold (Au) ions which surface LET = 87.4 MeV/mg/cm^2 and fluence level 1 x 10^7 ions/cm^2 and SET test performed using krypton ion at V_{CC} = 12 V, fluence = 1 X10^7 ions/cm^2, f_{OSC} = 400 kHz and duty cycle 20%.

Device types	01, 02, 03, 04, and 05	
Case outlines	E	X
Terminal number	Terminal symbol	
1	INV	NC
2	NON-INV	INV
3	E/A OUT	NON-INV
4	CLOCK	E/A OUT
5	R_T	CLOCK
6	C_T	R_T
7	RAMP	C_T
8	SOFT START	RAMP
9	ILIM/SD	SOFT START
10	GND	NC
11	OUTPUT A	ILIM/SD
12	POWER GND	GND
13	V_C	OUTPUT A
14	OUTPUT B	POWER GND
15	V_{CC}	V_C
16	V_{REF} 5.1 V	V_C
17	---	POWER GND
18	---	OUTPUT B
19	---	V_{CC}
20	---	V_{REF} 5.1 V

NOTES:
1. NC = No connection
2. Case X, PGND pins to be connected to each other.
3. Case X, V_C pins to be connected to each other.

FIGURE 1. Terminal connections.



NOTE: For device types 02 and 04 only, toggles Q and $\overline{Q}$ are always low.

FIGURE 2. Logic diagram.

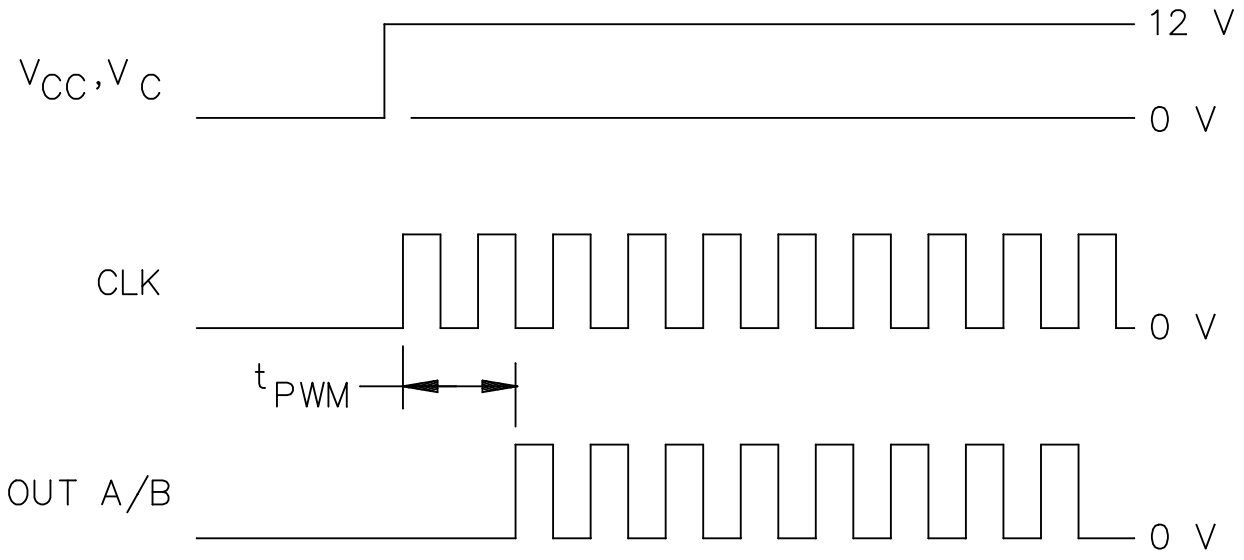


FIGURE 3. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,4,9	1,4,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3, 2/ 3/ 4,5,6,9,10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 3/ 9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9	As specified in QM plan

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 4, and Δ's.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters 1/	Symbol	Device types	Delta limits
Supply current	I_{CC}	01, 02, 03, 04, 05	±2.0 mA
Input bias current	I_{IB}	01, 02, 03, 04, 05	±150 nA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.
2/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, 03, 04, and 05. In addition, for device type 05 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL, SEB, and SET test limits, see Table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Occurrence of latchup (SEL).

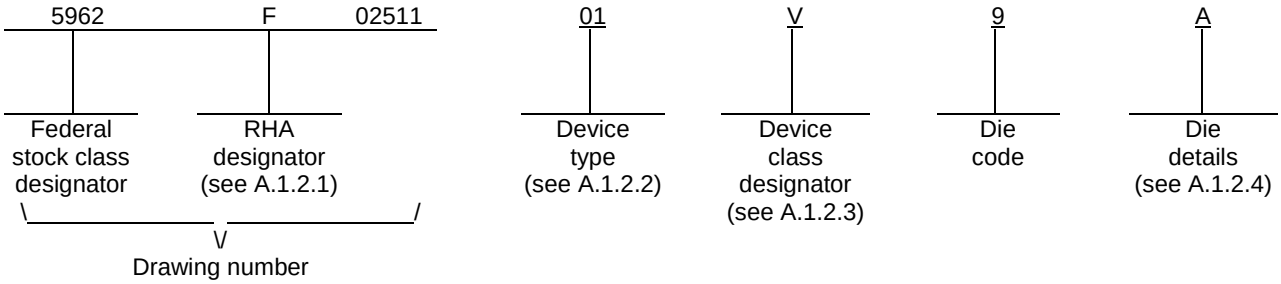
d. Occurrence of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-02511

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	IS-1825ASRH	Radiation hardened DI dual output pulse width modulator with SEU protection
02	ISL71823ASRH	Radiation hardened DI dual output pulse width modulator with SEU protection
03	IS-1825BSRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
04	ISL71823BSRH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection
05	IS-1825BSEH	Radiation hardened, DI dual output pulse width modulator with single event upset (SEU) protection

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04, 05	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04, 05	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04, 05	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04, 05	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime –VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

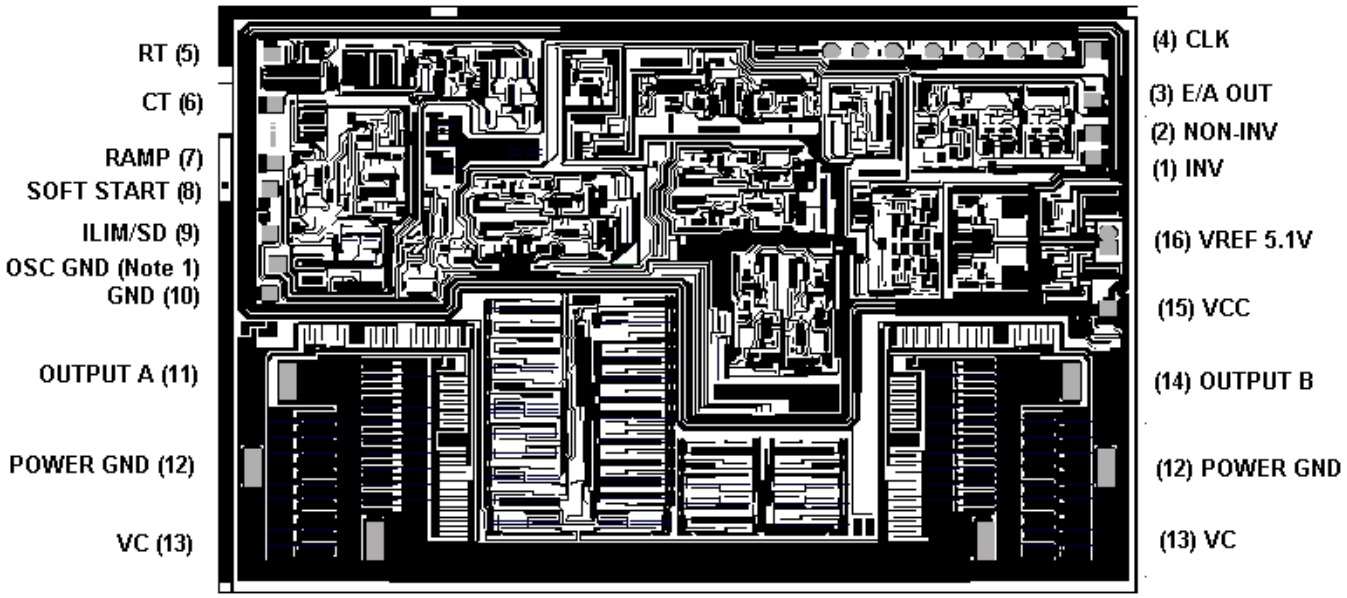
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime –VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime –VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outline E (see figure 1).

Die physical dimensions.
Die size : 4318 microns x 5842 microns.
Die thickness: 19 mils ± 1 mils.

Interface materials.
Top metallization: Al Si Cu 16.0 Kå ± 2 Kå
Backside metallization: None

Glassivation.
Type: PSG
Thickness: 8.0 Kå ± 1.0 Kå

Substrate: DI (dielectric isolation)

Assembly related information.
Substrate potential: Unbiased
Special assembly instructions: Note 1. The oscillator ground (OSC GND) pad must be connected to ground (GND).
Note 2. POWER GND and V_C each require 2 bond pad connections.
Note 3. POWER GND, OUPUT A, and OUTPUT B must be double bonded for current sharing purposes.

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-08-19

Approved sources of supply for SMD 5962-02511 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0251101QEC	34371	IS1-1825ASRH-8
5962F0251101QXC	34371	IS9-1825ASRH-8
5962R0251101TXC	34371	IS9-1825ASRH-T
5962F0251101VEC	34371	IS1-1825ASRH-Q
5962F0251101VXC	34371	IS9-1825ASRH-Q
5962F0251101V9A	34371	IS0-1825ASRH-Q
5962F0251102QEC	34371	ISL71823ASRHQD
5962F0251102QXC	34371	ISL71823ASRHQF
5962F0251102VEC	34371	ISL71823ASRHVD
5962F0251102VXC	34371	ISL71823ASRHVF
5962F0251102V9A	34371	ISL71823ASRHVX
5962F0251103QEC	34371	IS1-1825BSRH-8
5962F0251103QXC	34371	IS9-1825BSRH-8
5962F0251103VEC	34371	IS1-1825BSRH-Q
5962F0251103VXC	34371	IS9-1825BSRH-Q
5962F0251103V9A	34371	IS0-1825BSRH-Q

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0251104QEC	34371	ISL71823BSRHQD
5962F0251104QXC	34371	ISL71823BSRHQF
5962F0251104VEC	34371	ISL71823BSRHVD
5962F0251104VXC	34371	ISL71823BSRHVF
5962F0251104V9A	34371	ISL71823BSRHVX
5962F0251105VEC	34371	IS1-1825BSEH-Q
5962F0251105VXC	34371	IS9-1825BSEH-Q
5962F0251105V9A	34371	IS0-1825BSEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803