REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	08-01-10	Thomas M. Hess

REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49					
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

Charles F. Saffle

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Charles F. Saffle

APPROVED BY

Thomas M. Hess

DRAWING APPROVAL DATE

03-04-22

MICROCIRCUIT, DIGITAL, CMOS, FIXED-POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

REVISION LEVEL

A

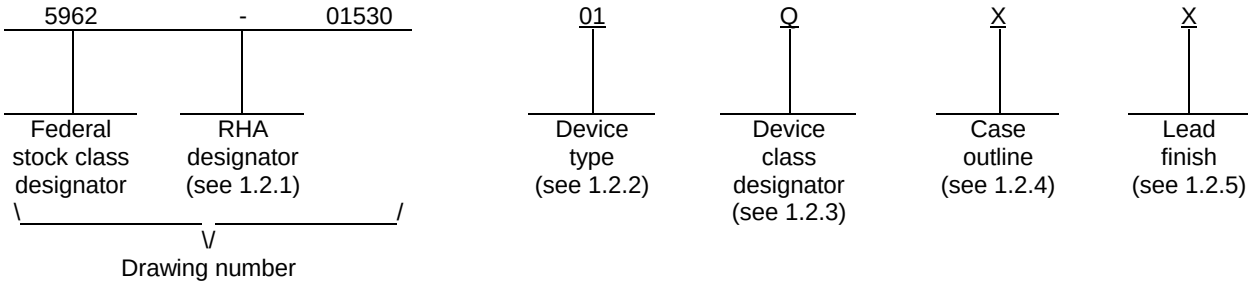
SIZE	CAGE CODE	
A	**67268**	**5962-01530**

SHEET 1 OF 49

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320VC5416	Fixed-point digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
Q or V	Certification and qualification to MIL-PRF-38535.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	164	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage I/O range (DV_{DD})	-0.3 V dc to +4.0 V dc
Supply voltage core range (CV_{DD})	-0.3 V dc to +2.0 V dc
Input voltage range (V_{IN})	-0.3 V dc to +4.5 V dc
Output voltage range (V_{OUT})	-0.3 V dc to +4.5 V dc
Thermal resistance, junction-to-case (θ_{JC})	1.82°C/W
Operating case temperature range (T_C)	-55°C to +115°C
Storage temperature range (T_{stg})	-55°C to +150°C

1.4 Recommended operating conditions.

Supply voltage I/O range (DV_{DD})	+2.75 V dc to +3.6 V dc
Supply voltage core range (CV_{DD})	+1.45 V dc to +1.65 V dc
Supply voltage ground (DV_{SS}, CV_{SS})	+0.0 V dc
High level input voltage, I/O (V_{IH}):	
Inputs 2/	+2.4 V to DV_{DD} +0.3 V 3/
All other inputs	+2.0 V to DV_{DD} +0.3 V 3/
Low level input voltage (V_{IL}):	
X2/CLKIN	-0.3 V to +0.42 V 4/
All other inputs	-0.3 V to +0.8 V 4/
Maximum high level output current (I_{OH})	-8 mA 5/
Maximum low level output current (I_{OL})	+8 mA 5/
Operating case temperature range (T_C)	-55°C to +115°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ For inputs: RS, INTn, NMI, X2/CLKIN, CLKMDn, BCLKRn, BCLKXn, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, $\overline{HAS}$, $\overline{TRST}$, $\overline{BIO}$, Dn, An, HDn, and TCK
3/ Maximum limit not production tested.
4/ Minimum limit not production tested.
5/ Maximum output currents are DC values only. Transient currents may exceed these values.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH} 1/	DV_{DD} = 2.75 V to 3 V, I_{OH} = -8 mA		1, 2, 3	All	2.2		V
		DV_{DD} = 3 V to 3.6 V, I_{OH} = -8 mA				2.4		
Low level output voltage	V_{OL} 1/	I_{OL} = 8 mA		1, 2, 3	All		0.4	V
Input current (V_{IN} = DV_{SS} to DV_{DD})	I_{IN}	X2/CLKIN		1, 2, 3	All	-40	40	µA
		$\overline{TRST}$, HPI16	With internal pulldown.			-10	800	
		HPIENA	With internal pulldown, $\overline{RS}$ = 0			-10	400	
		TMS, TCK, TDI, HPI 2/	With internal pullups			-400	10	
		A[17:0], D[15:0], HD[7:0]	Bus holders enabled, DV_{DD} = 3.6 V 3/			-275	275	
		All other input-only pins				-5	5	
Supply current, core CPU	I_{DDC}	CV_{DD} = 1.6 V, fx = 100 MHz, T_C = 25°C 4/		1, 2, 3	All	60 TYP 5/ 6/		mA
Supply current pins	I_{DDP}	DV_{DD} = 3.0 V, fx = 100 MHz, T_C = 25°C 4/		1, 2, 3	All	40 TYP 6/ 7/		mA
Supply current, standby	I_{DD}	IDLE2	PLL X 1 mode, 20 MHz input	1, 2, 3	All	2 TYP 6/		mA
		IDLE3 Divide-by-two mode, CLKIN stopped	T_C = 25°C			1 TYP 6/		
			T_C = 115°C			38 TYP 6/		
Input capacitance	C_{IN}	See 4.4.1b		4	All		15	pF
Output capacitance	C_{OUT}	See 4.4.1b		4	All		15	pF
Functional tests		DV_{DD} = 2.75 V to 3.6 V CV_{DD} = 1.45 V to 1.65 V See 4.4.1c		7, 8	All			
Input Clock Frequency Characteristics								
Input clock frequency	f_x			9, 10, 11	All	10 8/	20 9/	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Divide-By-2 and Divide-By-4 Clock Options Timing Requirements ($H = 0.5t_{c(CO)}$)							
Cycle time, X2/CLKIN	$t_{c(CI)}$	See figure 4	9, 10, 11	All	20.0		ns
Fall time, X2/CLKIN	$t_{f(CI)}$		9, 10, 11	All		4.0 10/	ns
Rise time, X2/CLKIN	$t_{r(CI)}$		9, 10, 11	All		4.0 10/	ns
Pulse duration, X2/CLKIN low	$t_{w(CIL)}$		9, 10, 11	All	4.0 10/		ns
Pulse duration, X2/CLKIN high	$t_{w(CIH)}$		9, 10, 11	All	4.0 10/		ns
Divide-By-2 and Divide-By-4 Clock Options Switching Characteristics ($H = 0.5t_{c(CO)}$)							
Cycle time, CLKOUT	$t_{c(CO)}$	See figure 4	9, 10, 11	All	10.0 11/	8/	ns
Delay time, X2/CLKIN high to CLKOUT high/low	$t_{d(CIH-CO)}$		9, 10, 11	All	4.0	11.0	ns
Fall time, CLKOUT	$t_{f(CO)}$		9, 10, 11	All		2.0 10/	ns
Rise time, CLKOUT	$t_{r(CO)}$		9, 10, 11	All		2.0 10/	ns
Pulse duration, CLKOUT low	$t_{w(COL)}$		9, 10, 11	All	H-3 10/	H+1 10/	ns
Pulse duration, CLKOUT high	$t_{w(COH)}$		9, 10, 11	All	H-2 10/	H+1 10/	ns
Multiply-By-N Clock Option Timing Requirements ($H = 0.5t_{c(CO)}$)							
Cycle time, X2/CLKIN	$t_{c(CI)}$	See figure 4 Integer PLL multiplier N (N = 1-15) 12/	9, 10, 11	All	20.0	200.0	ns
		See figure 4 PLL multiplier N = x.5 12/			20.0	100.0	
		See figure 4 PLL multiplier N = x.25, x.75 12/			20.0	50.0	
Fall time, X2/CLKIN	$t_{f(CI)}$	See figure 4	9, 10, 11	All		4.0 10/	ns
Rise time, X2/CLKIN	$t_{r(CI)}$		9, 10, 11	All		4.0 10/	ns
Pulse duration, X2/CLKIN low	$t_{w(CIL)}$		9, 10, 11	All	4.0 10/		ns
Pulse duration, X2/CLKIN high	$t_{w(CIH)}$		9, 10, 11	All	4.0 10/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Multiply-By-N Clock Option Switching Requirements ($H = 0.5t_{c(CO)}$)							
Cycle time, CLKOUT	$t_{c(CO)}$	See figure 4	9, 10, 11	All	10.0		ns
Delay time, X2/CLKIN high/low to CLKOUT high/low	$t_{d(CI-CO)}$		9, 10, 11	All	4.0	11.0	ns
Fall time, CLKOUT	$t_{f(CO)}$		9, 10, 11	All		2.0 10/	ns
Rise time, CLKOUT	$t_{r(CO)}$		9, 10, 11	All		2.0 10/	ns
Pulse duration, CLKOUT low	$t_{w(COL)}$		9, 10, 11	All	H-3 10/	H+1 10/	ns
Pulse duration, CLKOUT high	$t_{w(COH)}$		9, 10, 11	All	H-2 10/	H+1 10/	ns
Transitory phase, PLL lock-up time	t_p		9, 10, 11	All		30.0 10/	µs
Memory Read Timing Requirements ($\overline{MSTRB} = 0$ and $H = 0.5t_{c(CO)}$)							
Access time, read data access from address valid, first read access	$t_{a(A)M1}$ 13/	See figure 4	9, 10, 11	All		4H-9	ns
Access time, read data access from address valid, consecutive read accesses	$t_{a(A)M2}$ 13/		9, 10, 11	All		2H-9	ns
Setup time, read data valid before CLKOUT low	$t_{su(D)R}$		9, 10, 11	All	7.0		ns
Hold time, read data valid after CLKOUT low	$t_{h(D)R}$		9, 10, 11	All	0.0		ns
Memory Read Switching Characteristics ($\overline{MSTRB} = 0$ and $H = 0.5t_{c(CO)}$)							
Delay time, CLKOUT low to address valid	$t_{d(CLKL-A)}$ 13/	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to MSTRB low	$t_{d(CLKL-MSL)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to MSTRB high	$t_{d(CLKL-MSH)}$		9, 10, 11	All	-1.0 10/	4.0 10/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Memory Write Switching Characteristics ($\overline{MSTRB}$ = 0 and H = $0.5t_{c(CO)}$)							
Delay time, CLKOUT low to address valid	$t_{d(CLKL-A)}$ 13/	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Setup time, address valid before MSTRB low	$t_{su(A)MSL}$ 13/		9, 10, 11	All	2H-3		ns
Delay time, CLKOUT low to data valid	$t_{d(CLKL-D)W}$		9, 10, 11	All	-1.0 10/	4.0	ns
Setup time, data valid before MSTRB high	$t_{su(D)MSH}$		9, 10, 11	All	2H-5	2H+6	ns
Hold time, data valid after MSTRB high	$t_{h(D)MSH}$		9, 10, 11	All	2H-5 10/	2H+6 10/	ns
Delay time, CLKOUT low to MSTRB low	$t_{d(CLKL-MSL)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Pulse duration, $\overline{MSTRB}$ low	$t_{w(SL)MS}$		9, 10, 11	All	2H-3.2 10/		ns
Delay time, CLKOUT low to MSTRB high	$t_{d(CLKL-MSH)}$		9, 10, 11	All	-1.0 10/	4.0 10/	ns
I/O Read Timing Requirements ($\overline{IOSTRB}$ = 0 and H = $0.5t_{c(CO)}$)							
Access time, read data access from address valid, first read access	$t_{a(A)M1}$ 13/	See figure 4	9, 10, 11	All		4H-9	ns
Setup time, read data valid before CLKOUT low	$t_{su(D)R}$		9, 10, 11	All	7.0		ns
Hold time, read data valid after CLKOUT low	$t_{h(D)R}$		9, 10, 11	All	0.0		ns
I/O Read Switching Characteristics ($\overline{IOSTRB}$ = 0 and H = $0.5t_{c(CO)}$)							
Delay time, CLKOUT low to address valid	$t_{d(CLKL-A)}$ 13/	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to IOSTRB low	$t_{d(CLKL-IOSL)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to IOSTRB high	$t_{d(CLKL-IOSH)}$		9, 10, 11	All	-1.0 10/	4.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O Write Switching Characteristics ($\overline{IOSTRB}$ = 0 and H = $0.5t_{c(CO)}$)							
Delay time, CLKOUT low to address valid	$t_{d(CLKL-A)}$ 13/	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Setup time, address valid before IOSTRB low	$t_{su(A)IOSL}$ 13/		9, 10, 11	All	2H-3		ns
Delay time, CLKOUT low to write data valid	$t_{d(CLKL-D)W}$		9, 10, 11	All	-1.0 10/	4.0	ns
Setup time, data valid before IOSTRB high	$t_{su(D)IOSH}$		9, 10, 11	All	2H-5	2H+6 10/	ns
Hold time, data valid after IOSTRB high	$t_{h(D)IOSH}$		9, 10, 11	All	2H-5 10/	2H+6 10/	ns
Delay time, CLKOUT low to IOSTRB low	$t_{d(CLKL-IOSL)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Pulse duration, $\overline{IOSTRB}$ low	$t_{w(SL)IOS}$		9, 10, 11	All	2H-2 10/		ns
Delay time, CLKOUT low to IOSTRB high	$t_{d(CLKL-IOSH)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Ready Timing Requirements for Externally Generated Wait States (H = $0.5t_{c(CO)}$) 14/							
Setup time, READY before CLKOUT low	$t_{su(RDY)}$	See figure 4	9, 10, 11	All	7.0		ns
Hold time, READY after CLKOUT low	$t_{h(RDY)}$		9, 10, 11	All	0.0		ns
Valid time, READY after MSTRB low	$t_{v(RDY)MSTRB}$ 15/		9, 10, 11	All		4H-6.2 10/	ns
Hold time, READY after MSTRB low	$t_{h(RDY)MSTRB}$ 15/		9, 10, 11	All	4H 10/		ns
Valid time, READY after IOSTRB low	$t_{v(RDY)IOSTRB}$ 15/		9, 10, 11	All		4H-6 10/	ns
Hold time, READY after IOSTRB low	$t_{h(RDY)IOSTRB}$ 15/		9, 10, 11	All	4H 10/		ns
Ready Switching Characteristics for Externally Generated Wait States (H = $0.5t_{c(CO)}$) 14/							
Delay time, CLKOUT low to MSC low	$t_{d(MSCL)}$	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to MSC high	$t_{d(MSCH)}$		9, 10, 11	All	-1.0 10/	4.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{HOLD}$ and $\overline{HOLDA}$ Timing Requirements ($H = 0.5t_{c(CO)}$)							
Pulse duration, HOLD low duration	$t_{w(HOLD)}$	See figure 4	9, 10, 11	All	4H+8 10/		ns
Setup time, HOLD before CLKOUT low	$t_{su(HOLD)}$ 16/		9, 10, 11	All	7.0		ns
$\overline{HOLD}$ and $\overline{HOLDA}$ Switching Characteristics ($H = 0.5t_{c(CO)}$)							
Disable time, Address, PS, DS, IS high impedance from CLKOUT low	$t_{dis(CLKL-A)}$	See figure 4	9, 10, 11	All		3.0 10/	ns
Disable time, R/$\overline{W}$ high impedance from CLKOUT low	$t_{dis(CLKL-RW)}$		9, 10, 11	All		3.0 10/	ns
Disable time, $\overline{MSTRB}$, IOSTRB high impedance from CLKOUT low	$t_{dis(CLKL-S)}$		9, 10, 11	All		3.0 10/	ns
Enable time, Address, PS, DS, IS valid from CLKOUT low	$t_{en(CLKL-A)}$		9, 10, 11	All		2H+3 10/	ns
Enable time, R/$\overline{W}$ enabled CLKOUT low	$t_{en(CLKL-RW)}$		9, 10, 11	All		2H+3 10/	ns
Enable time, $\overline{MSTRB}$, IOSTRB enabled from CLKOUT low	$t_{en(CLKL-S)}$		9, 10, 11	All	2.0	2H+3 10/	ns
Valid time, $\overline{HOLDA}$ low afterCLKOUT low	$t_{v(HOLDA)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Valid time, $\overline{HOLDA}$ high afterCLKOUT low			9, 10, 11	All	-1.0 10/	4.0 10/	ns
Pulse duration, $\overline{HOLDA}$ low duration	$t_{w(HOLDA)}$		9, 10, 11	All	2H-3 10/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reset, $\overline{BIO}$, Interrupt, and MP/$\overline{MC}$ Timing Requirements (H = $0.5t_{c(CO)}$)							
Hold time, $\overline{RS}$ after CLKOUT low	$t_{h(RS)}$ 17/	See figure 4	9, 10, 11	All	2.0 10/		ns
Hold time, $\overline{BIO}$ after CLKOUT low	$t_{h(BIO)}$ 17/		9, 10, 11	All	4.0		ns
Hold time, $\overline{INTn}$, $\overline{NMI}$ after CLKOUT low	$t_{h(INT)}$ 17/ 18/		9, 10, 11	All	0.0		ns
Hold time, MP/$\overline{MC}$ after CLKOUT low	$t_{h(MPMC)}$ 17/		9, 10, 11	All	4.0 10/		ns
Pulse duration, $\overline{RS}$ low	$t_{w(RSL)}$ 19/ 20/		9, 10, 11	All	4H+3 10/		ns
Pulse duration, $\overline{BIO}$ low, synchronous	$t_{w(BIO)S}$		9, 10, 11	All	2H+3 10/		ns
Pulse duration, $\overline{BIO}$ low, asynchronous	$t_{w(BIO)A}$		9, 10, 11	All	4H 10/		ns
Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (synchronous)	$t_{w(INTH)S}$		9, 10, 11	All	2H+2 10/		ns
Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (asynchronous)	$t_{w(INTH)A}$		9, 10, 11	All	4H 10/		ns
Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (synchronous)	$t_{w(INTL)S}$		9, 10, 11	All	2H+2 10/		ns
Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (asynchronous)	$t_{w(INTL)A}$		9, 10, 11	All	4H 10/		ns
Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low for IDLE2/IDLE3 wakeup	$t_{w(INTL)WKP}$		9, 10, 11	All	7.0 10/		ns
Setup time, $\overline{RS}$ before X2CLKIN low	$t_{su(RS)}$ 17/ 21/		9, 10, 11	All	3.0 10/		ns
Setup time, $\overline{BIO}$ before CLKOUT low	$t_{su(BIO)}$ 17/		9, 10, 11	All	7.0		ns
Setup time, $\overline{INTn}$, $\overline{NMI}$, $\overline{RS}$ before CLKOUT low	$t_{su(INT)}$ 17/		9, 10, 11	All	7.0		ns
Setup time, MP/$\overline{MC}$ before CLKOUT low	$t_{su(MPMC)}$ 17/		9, 10, 11	All	5.0 10/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Switching Characteristics ($H = 0.5t_{c(CO)}$)							
Delay time, CLKOUT low to IAQ low	$t_{d(CLKL-IAQL)}$	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to IAQ high	$t_{d(CLKL-IAQH)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to IACK low	$t_{d(CLKL-IACKL)}$		9, 10, 11	All	-1.2 10/	4.0	ns
Delay time, CLKOUT low to IACK high	$t_{d(CLKL-IACKH)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to address valid	$t_{d(CLKL-A)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Pulse duration, $\overline{IAQ}$ low	$t_{w(IAQL)}$		9, 10, 11	All	2H-2 10/		ns
Pulse duration, $\overline{IACK}$ low	$t_{w(IACKL)}$		9, 10, 11	All	2H-3 10/		ns
External Flag (XF) and TOUT Switching Characteristics ($H = 0.5t_{c(CO)}$)							
Delay time, CLKOUT low to XF high	$t_{d(XF)}$	See figure 4	9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to XF low			9, 10, 11	All	-1.0 10/	4.0	ns
Delay time, CLKOUT low to TOUT high	$t_{d(TOUTH)}$		9, 10, 11	All	-1.0 10/	4.0 10/	ns
Delay time, CLKOUT low to TOUT low	$t_{d(TOUTL)}$		9, 10, 11	All	-1.0 10/	4.0	ns
Pulse duration, TOUT	$t_{w(TOUT)}$		9, 10, 11	All	2H-4 10/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +115°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
McBSP Transmit and Receive Timing Requirements 22/								
Cycle time, BCLKR/X	$t_{c(BCKRX)}$ 23/	See figure 4	BCLKR/X ext	9, 10, 11	All	4P 24/		ns
Pulse duration, BCLKR/X high or BCLKR/X low	$t_{w(BCKRX)}$ 23/		BCLKR/X ext	9, 10, 11	All	2P-1 10/ 24/		ns
Setup time, external BFSR high before BCLKR low	$t_{su(BFRH-BCKRL)}$		BCLKR int	9, 10, 11	All	8.0		ns
			BCLKR ext			1.0		
Hold time, external BFSR high after BCLKR low	$t_{h(BCKRL-BFRH)}$		BCLKR int	9, 10, 11	All	1.0		ns
			BCLKR ext			2.0		
Setup time, BDR valid before BCLKR low	$t_{su(BDRV-BCKRL)}$		BCLKR int	9, 10, 11	All	7.0		ns
			BCLKR ext			1.0		
Hold time, BDR valid after BCLKR low	$t_{h(BCKRL-BDRV)}$		BCLKR int	9, 10, 11	All	2.0		ns
			BCLKR ext			3.0		
Setup time, external BFSX high before BCLKX low	$t_{su(BFXH-BCKXL)}$		BCLKX int	9, 10, 11	All	8.0		ns
			BCLKX ext			1.0		
Hold time, external BFSX high after BCLKX low	$t_{h(BCKXL-BFXH)}$		BCLKX int	9, 10, 11	All	0.0		ns
			BCLKX ext			2.0		
Rise time, BCKR/X	$t_{r(BCKRX)}$		BCLKR/X ext	9, 10, 11	All		6.0 10/	ns
Fall time, BCKR/X	$t_{f(BCKRX)}$		BCLKR/X ext	9, 10, 11	All		6.0 10/	ns
McBSP Transmit and Receive Switching Characteristics 22/								
Cycle time, BCLKR/X	$t_{c(BCKRX)}$ 23/	See figure 4	BCLKR/X int	9, 10, 11	All	4P 24/		ns
Pulse duration, BCLKR/X high	$t_{w(BCKRXH)}$ 23/		BCLKR/X int	9, 10, 11	All	D-1 10/ 25/	D+1 10/ 25/	ns
Pulse duration, BCLKR/X low	$t_{w(BCKRXL)}$ 23/		BCLKR/X int	9, 10, 11	All	C-1 10/ 25/	C+1 10/ 25/	ns
Delay time, BCLKR high to internal BFSR valid	$t_{d(BCKRH-BFRV)}$		BCLKR int	9, 10, 11	All	-3.0 10/	3.0	ns
			BCLKR ext			0.0 10/	11.0	
Delay time, BCLKX high to internal BFSX valid	$t_{d(BCKXH-BFXV)}$		BCLKX int	9, 10, 11	All	-1.0 10/	5.0	ns
			BCLKX ext			3.0 10/	11.0	
Disable time, BCLKX high to BDX high impedance following last data bit of transfer	$t_{dis(BCKXH-BDXHZ)}$		BCLKX int	9, 10, 11	All		6.0 10/	ns
			BCLKX ext				10.0 10/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
McBSP Transmit and Receive Switching Characteristics - Continued 22/								
Delay time, BCLKX high to BDX valid	$t_{d(BCKXH-BDXV)}$	DXENA = 0 See figure 4	BCLKX int	9, 10, 11	All	-1.0 10/ 26/	10.0	ns
			BCLKX ext			3.0 10/	20.0	
		DXENA = 1 See figure 4	BCLKX int			-1.0 10/ 26/	20.0	
			BCLKX ext			2.8 10/	30.0	
Delay time, BFSX high to BDX valid (Only applies when in data delay 0 (XDATDLY = 00b) mode.)	$t_{d(BFXH-BDXV)}$	See figure 4	BFSX int	9, 10, 11	All	-1.2 10/ 26/	7.0 10/	ns
			BFSX ext			3.0 10/	11.0 10/	
McBSP General-Purpose I/O Timing Requirements								
Setup time, BGPIOx input mode before CLKOUT high	$t_{su(BGPIO-COH)}$ 27/	See figure 4		9, 10, 11	All	7.0		ns
Hold time, BGPIOx input mode after CLKOUT high	$t_{h(COH-BGPIO)}$ 27/			9, 10, 11	All	0.0		ns
McBSP General-Purpose I/O Switching Characteristics								
Delay time, CLKOUT high to BGPIOx output mode	$t_{d(COH-BGPIO)}$ 28/	See figure 4		9, 10, 11	All	-2.0 10/	4.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0) 29/							
Setup time, BDR valid before BCLKX low	$t_{su(BDRV-BCKXL)}$	MASTER See figure 4	9, 10, 11	All	12.0		ns
		SLAVE See figure 4			2.2-6P 10/ 24/		
Hold time, BDR valid after BCLKX low	$t_{h(BCKXL-BDRV)}$	MASTER See figure 4	9, 10, 11	All	4.0		ns
		SLAVE See figure 4			5+12P 10/ 24/		
McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0) 29/							
Hold time, BFSX low after BCLKX low	$t_{h(BCKXL-BFXL)}$ 30/	MASTER 31/ See figure 4	9, 10, 11	All	T-3 10/	T+4	ns
		SLAVE See figure 4					
Delay time, BFSX low to BCLKX high	$t_{d(BFXL-BCKXH)}$ 32/	MASTER 31/ See figure 4	9, 10, 11	All	C-4 10/	C+3 10/	ns
		SLAVE See figure 4					
Delay time, BCLKX high to BDX valid	$t_{d(BCKXH-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	-4.0 10/	5.0	ns
		SLAVE See figure 4			6P+2 10/ 24/	10P+17 24/	
Disable time, BDX high impedance following last data bit from BCLKX low	$t_{dis(BCKXL-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All	C-2 10/	C+3 10/	ns
		SLAVE See figure 4					
Disable time, BDX high impedance following last data bit from BFSX high	$t_{dis(BFXH-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All			ns
		SLAVE See figure 4			2P-4 10/ 24/	6P+17 10/ 24/	
Delay time, BFSX low to BDX valid	$t_{d(BFXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All			ns
		SLAVE See figure 4			4P+2 10/ 24/	8P+17 10/ 24/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0) 29/							
Setup time, BDR valid before BCLKX low	$t_{su(BDRV-BCKXL)}$	MASTER See figure 4	9, 10, 11	All	12.0		ns
		SLAVE See figure 4			2.2-6P 10/ 24/		
Hold time, BDR valid after BCLKX high	$t_{h(BCKXH-BDRV)}$	MASTER See figure 4	9, 10, 11	All	4.0		ns
		SLAVE See figure 4			5+12P 10/ 24/		
McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0) 29/							
Hold time, BFSX low after BCLKX low	$t_{h(BCKXL-BFXL)}$ 30/	MASTER 31/ See figure 4	9, 10, 11	All	C-3 10/	C+4	ns
		SLAVE See figure 4					
Delay time, BFSX low to BCLKX high	$t_{d(BFXL-BCKXH)}$ 32/	MASTER 31/ See figure 4	9, 10, 11	All	T-4 10/	T+3 10/	ns
		SLAVE See figure 4					
Delay time, BCLKX low to BDX valid	$t_{d(BCKXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	-4.0 10/	5.0	ns
		SLAVE See figure 4			6P+2 10/ 24/	10P+17 24/	
Disable time, BDX high impedance following last data bit from BCLKX low	$t_{dis(BCKXL-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All	-2.0 10/	4.0 10/	ns
		SLAVE See figure 4			6P-4 10/ 24/	10P+17 10/ 24/	
Delay time, BFSX low to BDX valid	$t_{d(BFXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	D-2 10/	D+4 10/	ns
		SLAVE See figure 4			4P+2 10/ 24/	8P+17 10/ 24/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1) 29/							
Setup time, BDR valid before BCLKX high	$t_{su(BDRV-BCKXH)}$	MASTER See figure 4	9, 10, 11	All	12.0		ns
		SLAVE See figure 4			2-6P 10/ 24/		
Hold time, BDR valid after BCLKX high	$t_{h(BCKXH-BDRV)}$	MASTER See figure 4	9, 10, 11	All	4.0		ns
		SLAVE See figure 4			5+12P 10/ 24/		
McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1) 29/							
Hold time, BFSX low after BCLKX high	$t_{h(BCKXH-BFXL)}$ 30/	MASTER 31/ See figure 4	9, 10, 11	All	T-3 10/	T+4	ns
		SLAVE See figure 4					
Delay time, BFSX low to BCLKX low	$t_{d(BFXL-BCKXL)}$ 32/	MASTER 31/ See figure 4	9, 10, 11	All	D-4 10/	D+3 10/	ns
		SLAVE See figure 4					
Delay time, BCLKX low to BDX valid	$t_{d(BCKXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	-4.0 10/	5.0	ns
		SLAVE See figure 4			6P+2 10/ 24/	10P+17 24/	
Disable time, BDX high impedance following last data bit from BCLKX high	$t_{dis(BCKXH-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All	D-2 10/	D+3 10/	ns
		SLAVE See figure 4					
Disable time, BDX high impedance following last data bit from BFSX high	$t_{dis(BFXH-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All			ns
		SLAVE See figure 4			2P-4 10/ 24/	6P+17 10/ 24/	
Delay time, BFSX low to BDX valid	$t_{d(BFXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All			ns
		SLAVE See figure 4			4P+2 10/ 24/	8P+17 10/ 24/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1) 29/							
Setup time, BDR valid before BCLKX low	$t_{su(BDRV-BCKXL)}$	MASTER See figure 4	9, 10, 11	All	12.0		ns
		SLAVE See figure 4			2-6P 10/ 24/		
Hold time, BDR valid after BCLKX low	$t_{h(BCKXL-BDRV)}$	MASTER See figure 4	9, 10, 11	All	4.0		ns
		SLAVE See figure 4			5+12P 10/ 24/		
McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1) 29/							
Hold time, BFSX low after BCLKX high	$t_{h(BCKXH-BFXL)}$ 30/	MASTER 31/ See figure 4	9, 10, 11	All	D-3 10/	D+4	ns
		SLAVE See figure 4					
Delay time, BFSX low to BCLKX low	$t_{d(BFXL-BCKXL)}$ 32/	MASTER 31/ See figure 4	9, 10, 11	All	T-4 10/	T+3 10/	ns
		SLAVE See figure 4					
Delay time, BCLKX high to BDX valid	$t_{d(BCKXH-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	-4.0 10/	5.0	ns
		SLAVE See figure 4			6P+2 10/ 24/	10P+17 24/	
Disable time, BDX high impedance following last data bit from BCLKX high	$t_{dis(BCKXH-BDXHZ)}$	MASTER 31/ See figure 4	9, 10, 11	All	-2.0 10/	4.0 10/	ns
		SLAVE See figure 4			6P-4 10/ 24/	10P+17 10/ 24/	
Delay time, BFSX low to BDX valid	$t_{d(BFXL-BDXV)}$	MASTER 31/ See figure 4	9, 10, 11	All	C-2 10/	C+4 10/	ns
		SLAVE See figure 4			4P+2 10/ 24/	8P+17 10/ 24/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +115°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HPI8 Mode Timing Requirements							
Setup time, HBIL valid before DS low (when HAS is not used), or HBIL valid before HAS low	$t_{su(HBV-DSL)}$	See figure 4	9, 10, 11	All	6.0		ns
Hold time, HBIL valid after DS low (when HAS is not used), or HBIL valid after HAS low	$t_{h(DSL-HBV)}$		9, 10, 11	All	3.0		ns
Setup time, HAS low before DS low	$t_{su(HSL-DSL)}$		9, 10, 11	All	8.0 10/		ns
Pulse duration, DS low	$t_{w(DSL)}$		9, 10, 11	All	13.0 10/		ns
Pulse duration, DS high	$t_{w(DSH)}$		9, 10, 11	All	7.0 10/		ns
Setup time, HD valid before DS high, HPI write	$t_{su(HDV-DSH)}$		9, 10, 11	All	3.0		ns
Hold time, HD valid after DS high, HPI write	$t_{h(DSH-HDV)W}$		9, 10, 11	All	2.0		ns
Setup time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	$t_{su(GPIO-COH)}$		9, 10, 11	All	6.0 10/		ns
Hold time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	$t_{su(GPIO-COH)}$		9, 10, 11	All	0.0 10/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HPI8 Mode Switching Characteristics							
Enable time, HD driven from DS low	$t_{en(DSL-HD)}$	See figure 4	9, 10, 11	All	0.0 10/	10.0 10/	ns
Delay time, DS low to HD valid for first byte of an HPI read	$t_{d(DSL-HDV1)}$	See figure 4 Case 1a: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} < 36P$. 33/	9, 10, 11	All		36P+10 $-t_{w(DSH)}$ 10/	ns
		See figure 4 Case 1b: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} \ge 36P$. 33/				10.0 10/	
		See figure 4 Case 1c: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} < 18P$. 33/				18P+10 $-t_{w(DSH)}$ 10/	
		See figure 4 Case 1d: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} \ge 18P$. 33/				10.0 10/	
		See figure 4 Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)} < 10P$. 33/				10P+10 $-t_{w(DSH)}$ 10/	
		See figure 4 Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \ge 10P$. 33/				10.0 10/	
		See figure 4 Case 3: Register accesses.				10.0 10/	
Delay time, DS low to HD valid for second byte of an HPI read	$t_{d(DSL-HDV2)}$	See figure 4	9, 10, 11	All		10.0 10/	ns
Hold time, HD valid after DS high, for a HPI read	$t_{d(DSH-HDV)R}$		9, 10, 11	All	0.0 10/		ns
Valid time, HD valid after HRDY high	$t_{v(HYH-HDV)}$		9, 10, 11	All		2.0 10/	ns
Delay time, DS high to HRDY low	$t_{d(DSH-HYL)}$ 34/		9, 10, 11	All		8.0 10/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HPI8 Mode Switching Characteristics - Continued.							
Delay time, DS high to HRDY high	$t_{d(DSH-HYH)}$ 34/	See figure 4 Case 1a: Memory accesses when DMAC is active in 16-bit mode. 33/	9, 10, 11	All		18P+6 10/	ns
		See figure 4 Case 1b: Memory accesses when DMAC is active in 32-bit mode. 33/				36P+6 10/	
		See figure 4 Case 2: Memory accesses when DMAC is inactive. 33/				10P+6 10/	
		See figure 4 Case 3: Write accesses to HPIC register. 35/				6P+6 10/	
Delay time, $\overline{HCS}$ low/high to HRDY low/high	$t_{d(HCS-HRDY)}$	See figure 4	9, 10, 11	All		6.0 10/	ns
Delay time, CLKOUT high to HRDY high	$t_{d(COH-HYH)}$		9, 10, 11	All		9.0	ns
Delay time, CLKOUT high to HINT change	$t_{d(COH-HTX)}$		9, 10, 11	All		6.0	ns
Delay time, CLKOUT high to HDx output change. HDx is configured as a general-purpose output.	$t_{d(COH-GPIO)}$		9, 10, 11	All		5.0 10/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
HPI16 Mode Timing Requirements								
Setup time, HR/$\overline{W}$ valid before DS falling edge	$t_{su(HBV-DSL)}$	See figure 4		9, 10, 11	All	6.0		ns
Hold time, HR/$\overline{W}$ valid after DS falling edge	$t_{h(DSL-HBV)}$			9, 10, 11	All	5.0		ns
Setup time, address valid before DS rising edge (write)	$t_{su(HAV-DSH)}$			9, 10, 11	All	5.0 10/		ns
Setup time, address valid before DS falling edge (read)	$t_{su(HAV-DSL)}$			9, 10, 11	All	-(4P-6) 10/		ns
Hold time, address valid after DS rising edge	$t_{h(DSH-HAV)}$			9, 10, 11	All	1.0 10/		ns
Pulse duration, DS low	$t_{w(DSL)}$			9, 10, 11	All	30.0 10/		ns
Pulse duration, DS high	$t_{w(DSH)}$			9, 10, 11	All	10.0 10/		ns
Cycle time, DS rising edge to next DS rising edge	$t_{c(DSH-DSH)}$	See figure 4 Memory accesses with no DMA activity	Reads	9, 10, 11	All	10P+30 10/		ns
			Writes			10P+10 10/		
		See figure 4 Memory accesses with 16-bit DMA activity	Reads			16P+30 10/		
			Writes			16P+10 10/		
		See figure 4 Memory accesses with 32-bit DMA activity	Reads			24P+30 10/		
			Writes			24P+10 10/		
Setup time, HD valid before DS rising edge (write)	$t_{su(HDV-DSH)W}$	See figure 4		9, 10, 11	All	8.0		ns
Hold time, HD valid after DS rising edge (write)	$t_{h(DSH-HDV)W}$			9, 10, 11	All	2.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HPI16 Mode Switching Characteristics							
Delay time, DS low to HD driven	$t_{d(DSL-HDD)}$	See figure 4	9, 10, 11	All	0.0 10/	10.0 10/	ns
Delay time, DS low to HD valid for first word of an HPI read	$t_{d(DSL-HDV1)}$	See figure 4 Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 32-bit mode and $t_{w(DSH)}$ was < 26P.	9, 10, 11	All		48P+20 $-t_{w(DSH)}$ 10/	ns
		See figure 4 Case 1b: Memory accesses not immediately following a write when DMAC is active in 32-bit mode.				24P+20 10/	
		See figure 4 Case 1c: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 18P.				32P+20 $-t_{w(DSH)}$ 10/	
		See figure 4 Case 1d: Memory accesses not immediately following a write when DMAC is active in 16-bit mode.				16P+20 10/	
		See figure 4 Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_{w(DSH)}$ was < 10P.				20P+20 $-t_{w(DSH)}$ 10/	
		See figure 4 Case 2b: Memory accesses not immediately following a write when DMAC is inactive.				10P+20 10/	
Delay time, DS high to HRDY high	$t_{d(DSH-HYH)}$	See figure 4 Memory writes when no DMA is active.	9, 10, 11	All		10P+5 10/	ns
		See figure 4 Memory writes with one or more 16-bit DMA channels active.				16P+5 10/	
		See figure 4 Memory writes with one or more 32-bit DMA channels active.				24P+5 10/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HPI16 Mode Switching Characteristics - Continued.							
Valid time, HD valid after HRDY high	$t_{v(HYH-HDV)}$	See figure 4	9, 10, 11	All		7.0 10/	ns
Hold time, HD valid after DS rising edge (read)	$t_{h(DSH-HDV)R}$		9, 10, 11	All	1.0 10/	6.0 10/	ns
Delay time, CLKOUT rising edge to HRDY high	$t_{d(COH-HYH)}$		9, 10, 11	All		5.0	ns
Delay time, DS low to HRDY low	$t_{d(DSL-HYL)}$		9, 10, 11	All		12.0 10/	ns
Delay time, DS high to HRDY low	$t_{d(DSH-HYL)}$		9, 10, 11	All		12.0 10/	ns

1/ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$ - $\overline{INT3}$, $\overline{NMI}$, X2/CLKIN, CLKMD1 - CLKMD3, BCLKRn, BCLKXn, $\overline{HCS}$, $\overline{HAS}$, $\overline{HDS1}$, $\overline{HDS2}$, BIO, TCK, $\overline{TRST}$, Dn, An, and HDn are LVTTL-compatible.

2/ HPI input signals except for HPIENA and HPI16, when HPIENA = 0.

3/ $V_{IL(MIN)} \le V_{IN} \le V_{IL(MAX)}$ or $V_{IH(MIN)} \le V_{IN} \le V_{IH(MAX)}$.

4/ Clock mode: PLL x 1 with external source.

5/ This value was obtained with 50% usage of MAC and 50%usage of NOP instructions. Actual operating current varies with program being executed.

6/ TYP = typical value, which is neither a minimum value or a maximum value. The value provided as a typical value is a normal operating value.

7/ This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF.

8/ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞.

9/ It is recommended that the PLL multiply by N clocking option be used for maximum frequency operation.

10/ This parameter is not production tested. This parameter is established by design, or is only characterized at initial release and after changes which may affect performance.

11/ It is recommended that the PLL clocking option be used for maximum frequency operation.

12/ N is the multiplication factor.

13/ Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

14/ The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.

15/ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

16/ This input can be driven from an asynchronous source, therefore, there are no specific timing requirements with respect to CLKOUT, however, if this timing is met, the input will be recognized on the CLKOUT edge referenced.

TABLE I. Electrical performance characteristics – Continued.

17/ These inputs can be driven from an asynchronous source, therefore, there are no specific timing requirements with respect to CLKOUT, however, if setup and hold timings are met, the input will be recognized on the CLKOUT edge referenced.

18/ The external interrupts ($\overline{INT0}$-$\overline{INT3}$, $\overline{NMI}$) are synchronized to the core CPU by way of a two flip-flop synchronizer that samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

19/ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{RS}$ must be held low for at least 50 μs to ensure synchronization and lock-in of the PLL.

20/ Note that $\overline{RS}$ may cause a change in clock frequency, therefore changing the value of H.

21/ The diagram assumes clock mode is divide-by-2 and the CLKOUT divide factor is set to no-divide mode (DIVFCT = 00 field in the BSCR).

22/ CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

23/ Note that in some cases, for example when driving another 54x device McBSP, maximum serial port clocking rates may not be achievable at maximum CPU clock frequency due to transmitted data timings and corresponding receive timing requirements. A separate detailed timing analysis should be performed for each specific McBSP interface.

24/ P = 1/(2 x processor clock).

25/ T = BCLKRX period = (1 + CLKGDV) x 2P.
C = BCLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) x 2P when CLKGDV is even.
D = BCLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) x 2P when CLKGDV is even.

26/ Minimum delay times also represent minimum output hold times.

27/ BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

28/ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

29/ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

30/ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP.
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.

31/ T = BCLKX period = (1 + CLKGDV) x 2P.
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) x 2P when CLKGDV is even.

32/ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

33/ DMAC stands for direct memory access controller (DMAC). The HPI8 shares the internal DMA bus with the DMAC, thus HPI8 access times are affected by DMAC activity.

34/ The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.

35/ This timing applies when writing a one to the DSPINT bit or $\overline{HINT}$ bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.

Case X

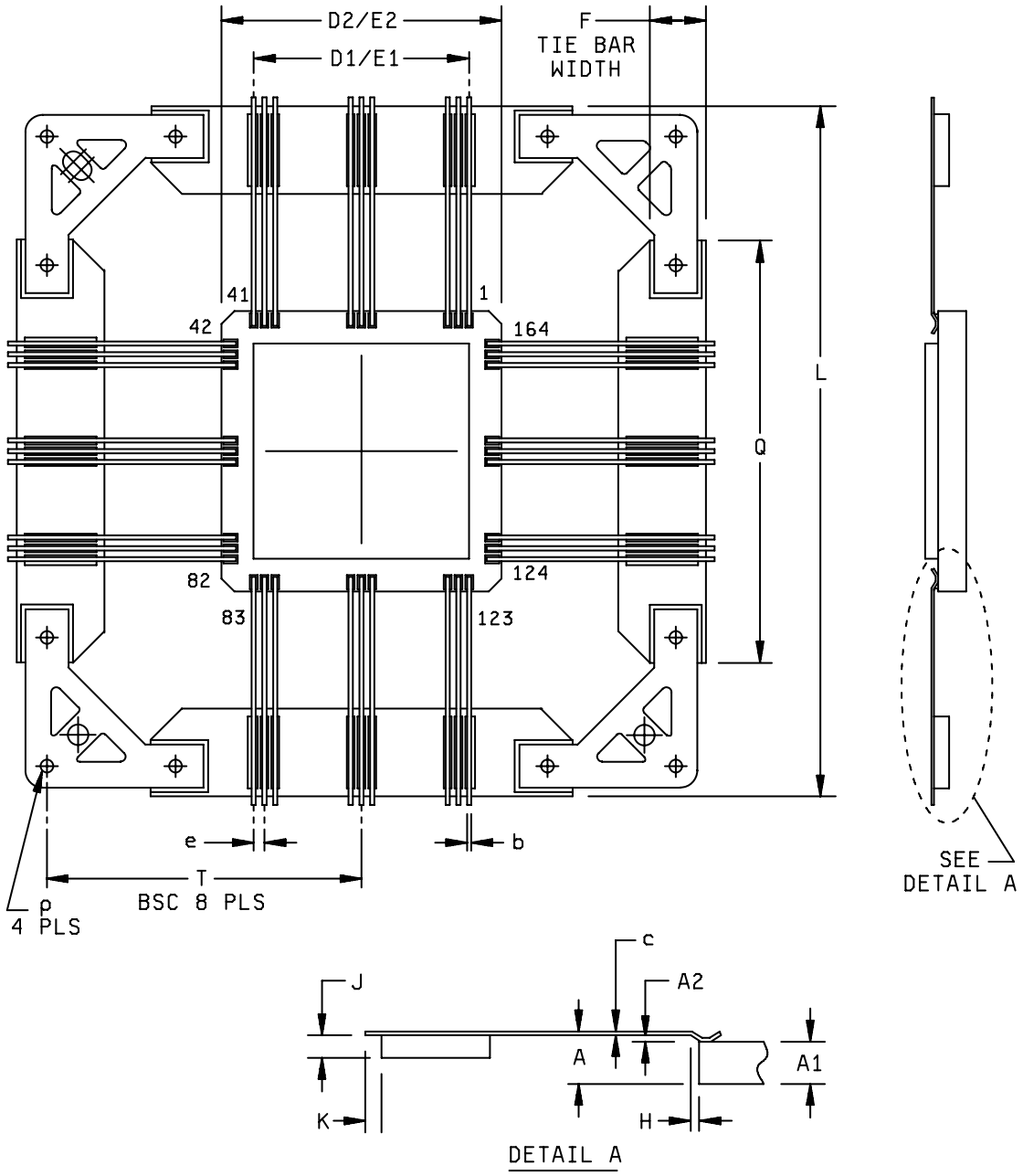


FIGURE 1. Case outline.

Case outline	X			
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.30		0.130
A1		2.67		0.105
A2	0.05	0.36	0.002	0.014
b	0.15	0.25	0.006	0.010
c	0.10	0.23	0.004	0.009
D1/E1	25.40 BSC		1.000 BSC	
D2/E2	28.45	28.96	1.120	1.140
e	0.64		0.025	
F	6.99	8.26	0.275	0.325
H		0.46		0.018
J	0.76	1.02	0.030	0.040
K		0.51		0.020
L	63.12	63.63	2.485	2.505
P	1.50	1.55	0.059	0.061
Q	37.59	38.61	1.480	1.520
T	29.21 BSC		1.150 BSC	

NOTES:
1. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
2. This package is hermetically sealed with a metal lid.
3. The leads are gold plated and can be solder dipped.
4. Leads not shown for clarity purposes.

FIGURE 1. Case outline – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	41	BFSR1
2	NC	42	V_{SS}
3	A22	43	BCLKR1
4	NC	44	HCNTL0
5	V_{SS}	45	V_{SS}
6	DV_{DD}	46	BCLKR0
7	A10	47	BCLKR2
8	HD7	48	BFSR0
9	A11	49	BFSR2
10	A12	50	BDR0
11	A13	51	HCNTL1
12	A14	52	V_{SS}
13	A15	53	BDR2
14	NC	54	CV_{DD}
15	CV_{DD}	55	BCLKX0
16	HAS	56	BCLKX2
17	V_{SS}	57	NC
18	CV_{DD}	58	V_{SS}
19	HCS	59	HINT
20	HR/W	60	NC
21	READY	61	CV_{DD}
22	PS	62	BFSX0
23	CV_{DD}	63	BFSX2
24	DS	64	HRDY
25	V_{SS}	65	DV_{DD}
26	IS	66	V_{SS}
27	R/W	67	HD0
28	MSTRB	68	BDX0
29	IOSTRB	69	BDX2
30	MSC	70	CV_{DD}
31	XF	71	IACK
32	HOLDA	72	V_{SS}
33	IAQ	73	HBIL
34	HOLD	74	NMI
35	BIO	75	INT0
36	MP/MC	76	INT1
37	DV_{DD}	77	INT2
38	NC	78	INT3
39	V_{SS}	79	NC
40	BDR1	80	CV_{DD}

NC = No connection

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
81	HD1	123	A18
82	NC	124	A19
83	V_{SS}	125	A20
84	BCLKX1	126	NC
85	BFSX1	127	V_{SS}
86	BDX1	128	DV_{DD}
87	DV_{DD}	129	D6
88	CLKMD1	130	D7
89	CLKMD2	131	D8
90	CLKMD3	132	D9
91	HPI16	133	D10
92	HD2	134	D11
93	TOUT	135	V_{SS}
94	EMU0	136	CV_{DD}
95	EMU1/OFF	137	D12
96	TD0	138	HD4
97	V_{SS}	139	D13
98	TDI	140	D14
99	CV_{DD}	141	D15
100	TRST	142	HD5
101	TCK	143	V_{SS}
102	TMS	144	NC
103	V_{SS}	145	HDS1
104	NC	146	V_{SS}
105	CV_{DD}	147	HDS2
106	HPIENA	148	DV_{DD}
107	V_{SS}	149	A0
108	CV_{DD}	150	A1
109	CLKOUT	151	CV_{DD}
110	HD3	152	A2
111	X1	153	V_{SS}
112	X2/CLKIN	154	A3
113	RS	155	HD6
114	D0	156	A4
115	D1	157	A5
116	D2	158	A6
117	D3	159	A7
118	D4	160	A8
119	D5	161	A9
120	A16	162	CV_{DD}
121	V_{SS}	163	A21
122	A17	164	V_{SS}

NC = No connection

FIGURE 2. Terminal connections – Continued.

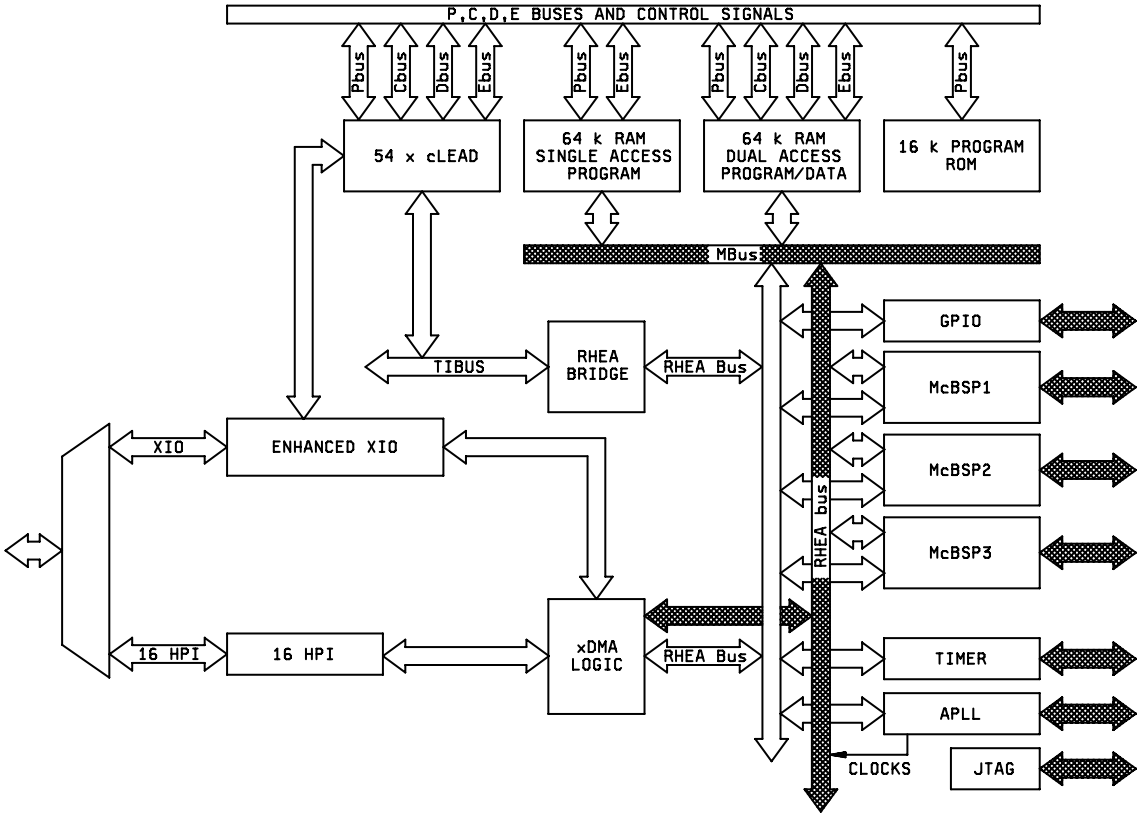
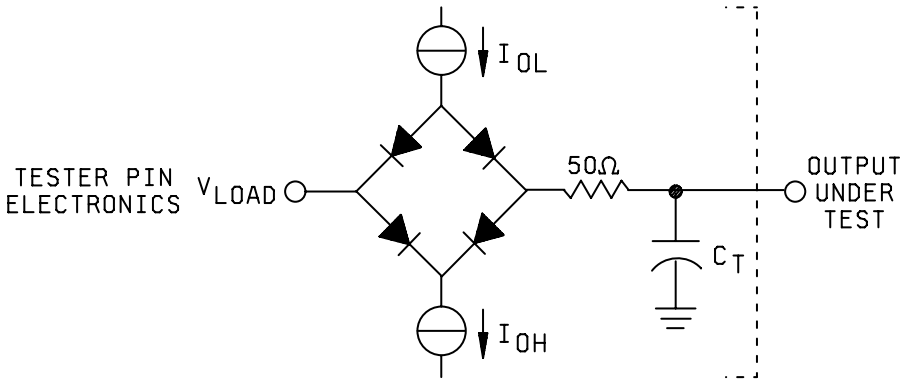
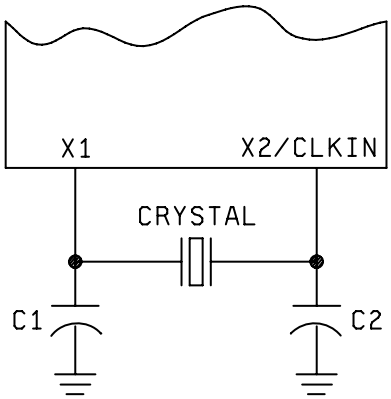


FIGURE 3. Block diagram.



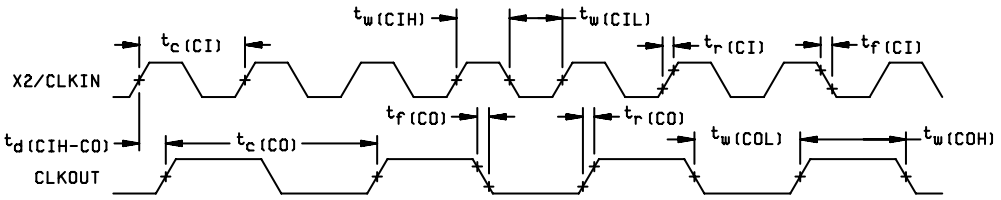
3.3 V Test Load Circuit

Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{LOAD} = 1.5 V
C_T = 20 pF typical load circuit capacitance



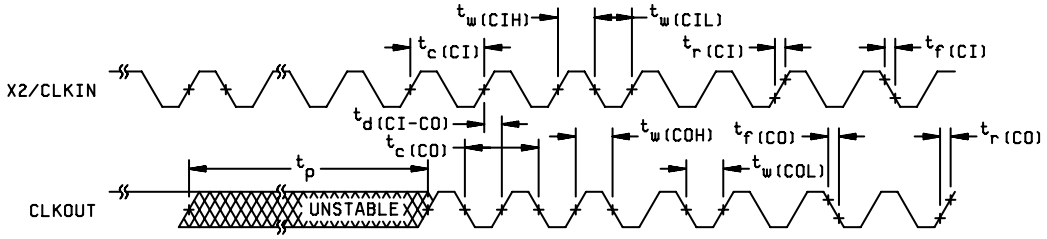
INTERNAL DIVIDE-BY-TWO CLOCK
OPTION WITH EXTERNAL CRYSTAL

FIGURE 4. Test circuit and switching waveforms.



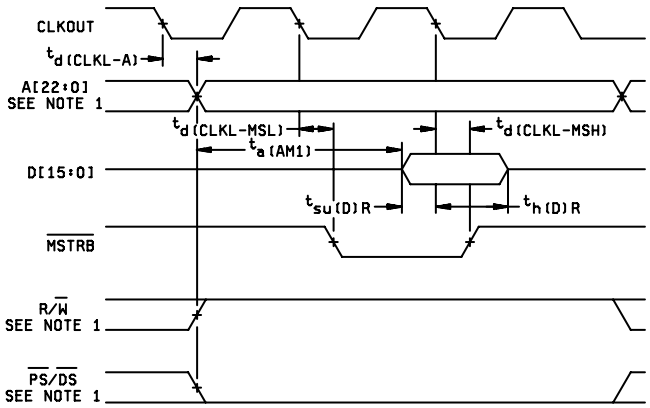
EXTERNAL DIVIDE-BY-TWO CLOCK TIMING

Note: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.



MULTIPLY-BY-ONE CLOCK TIMING

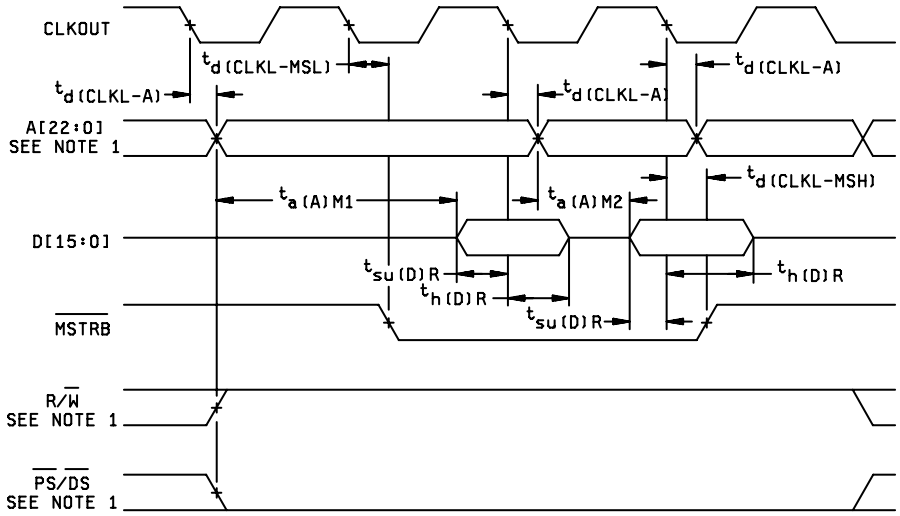
Note: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.



NONCONSECUTIVE MODE MEMORY READS

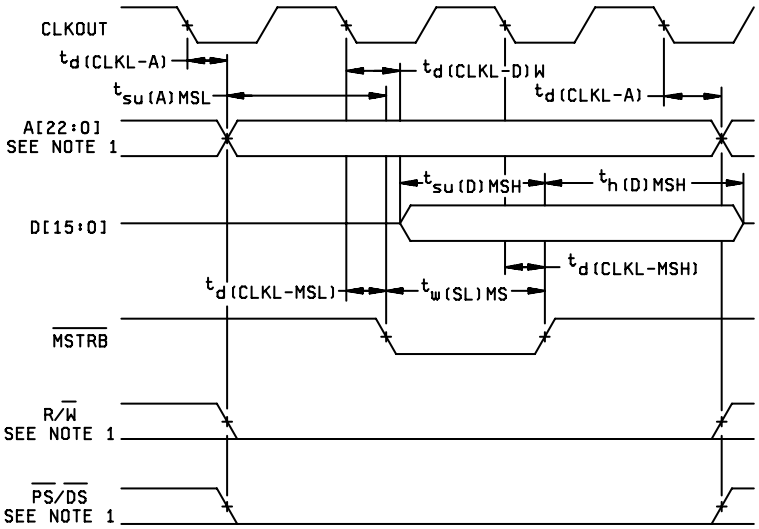
Note 1. Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

FIGURE 4. Test circuit and switching waveforms – Continued.



CONSECUTIVE MODE MEMORY READS

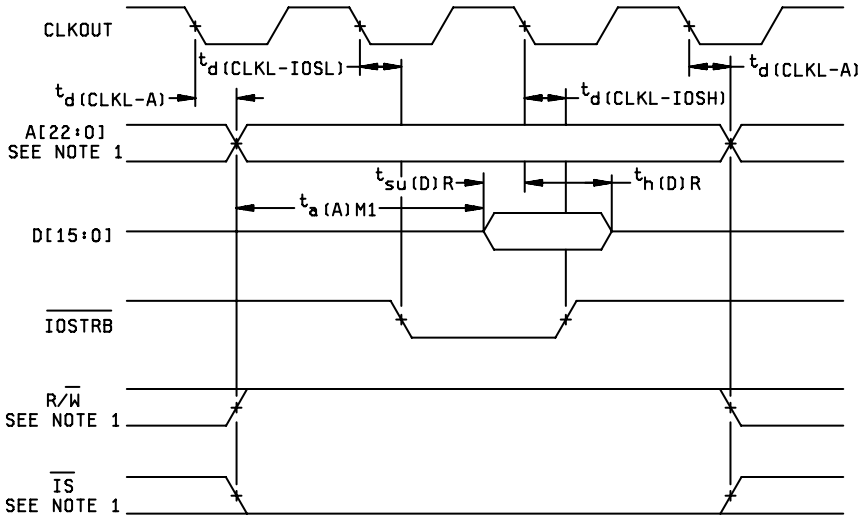
Note 1. Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.



MEMORY WRITE ($\overline{MSTRB}$=0)

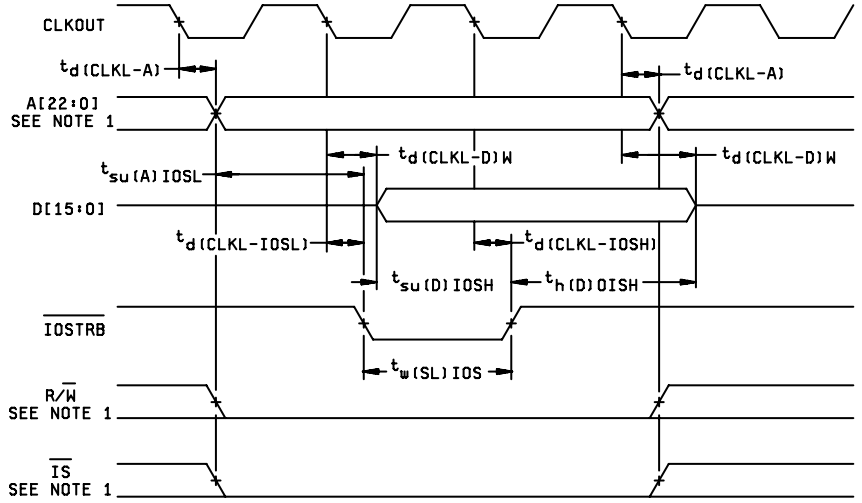
Note 1. Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

FIGURE 4. Test circuit and switching waveforms – Continued.



PARALLEL I/O PORT READ($\overline{\text{IOSTRB}}$=0)

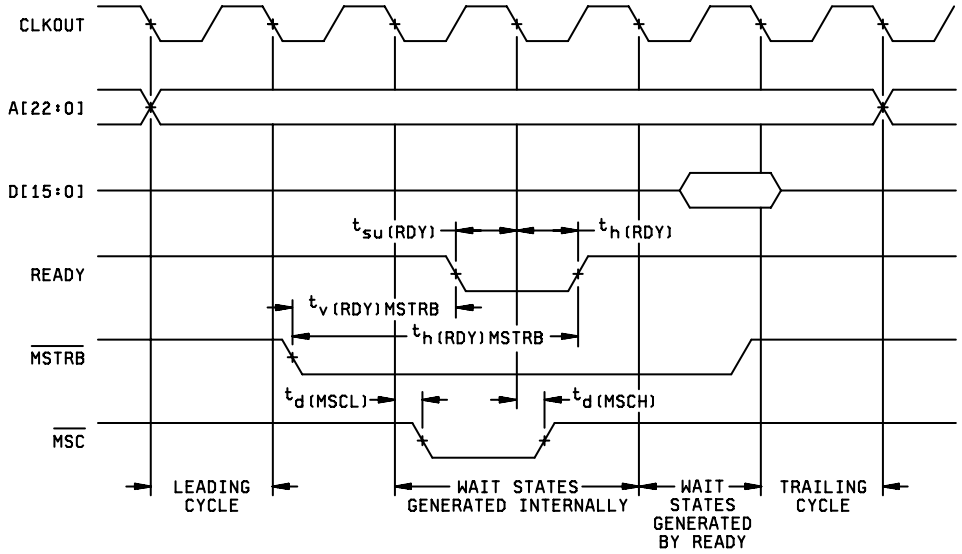
Note 1. Address, R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



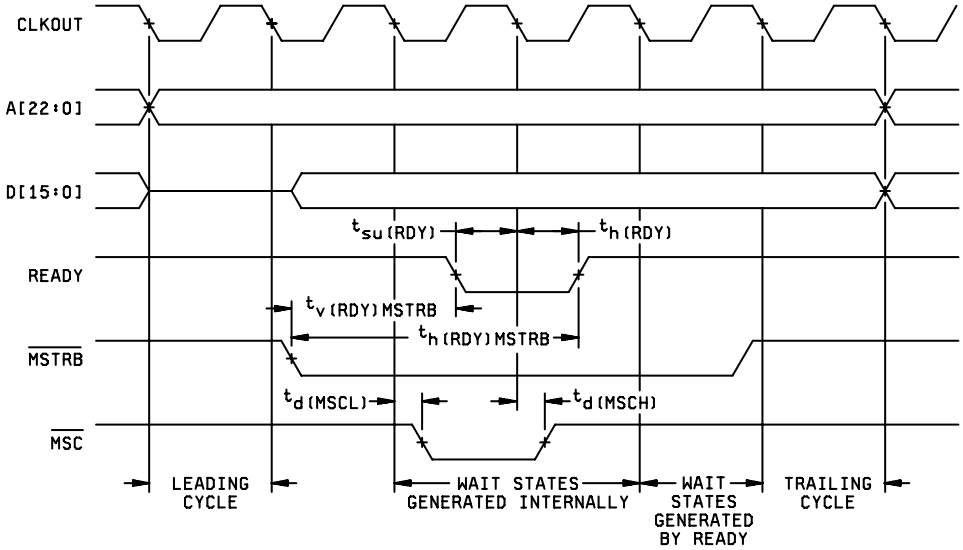
PARALLEL I/O PORT WRITE ($\overline{\text{IOSTRB}}$=0)

Note 1. Address, R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

FIGURE 4. Test circuit and switching waveforms – Continued.

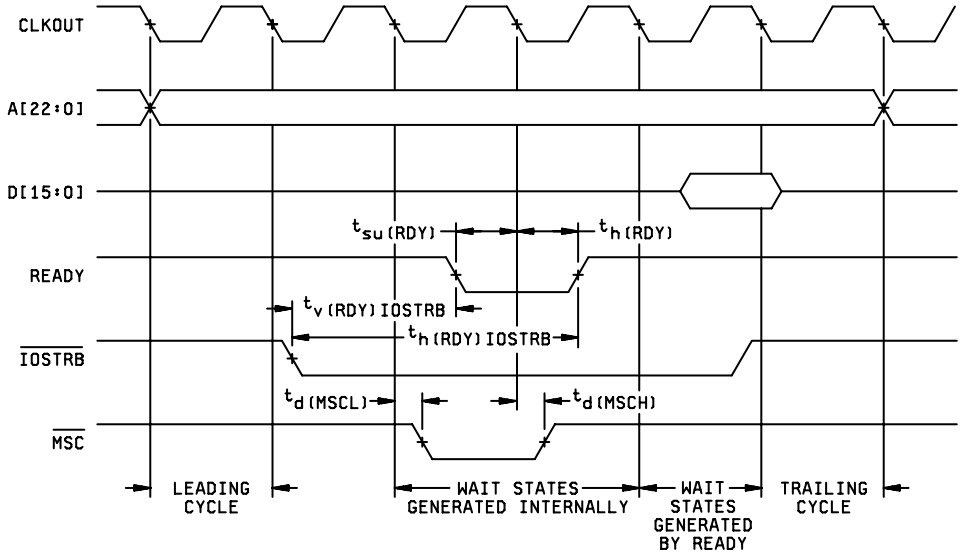


MEMORY READ WITH EXTERNALLY GENERATED WAIT STATES

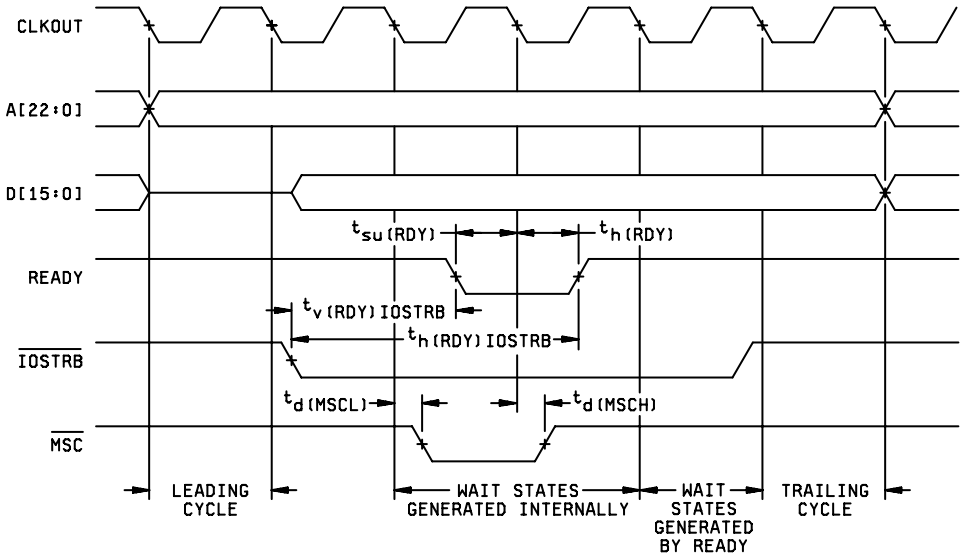


MEMORY WRITE WITH EXTERNALLY GENERATED WAIT STATES

FIGURE 4. Test circuit and switching waveforms – Continued.

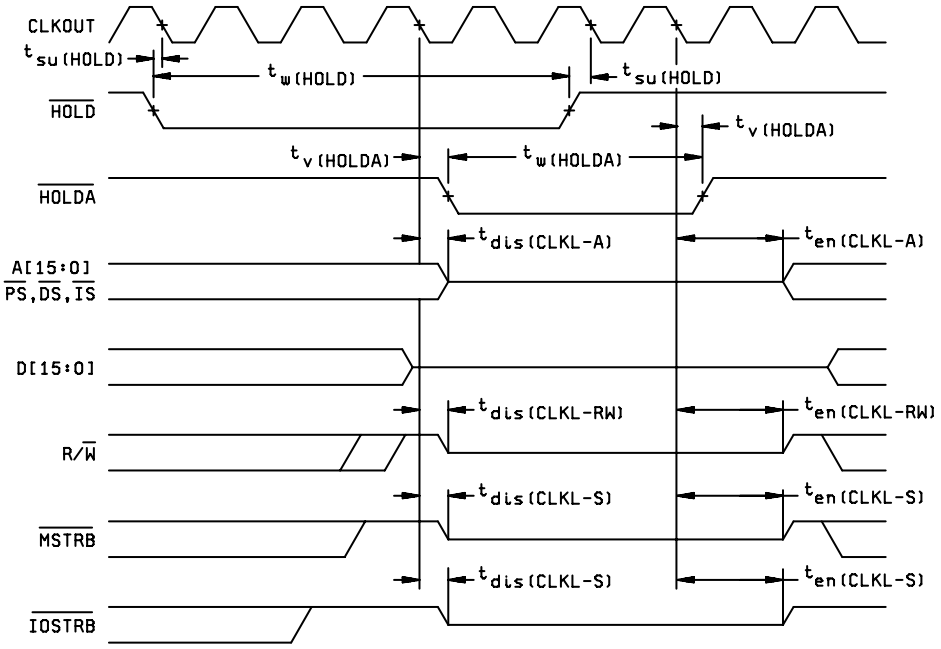


I/O READ WITH EXTERNALLY GENERATED WAIT STATES



I/O WRITE WITH EXTERNALLY GENERATED WAIT STATES

FIGURE 4. Test circuit and switching waveforms – Continued.



HOLD AND HOLDA TIMINGS(HM=1)

FIGURE 4. Test circuit and switching waveforms – Continued.

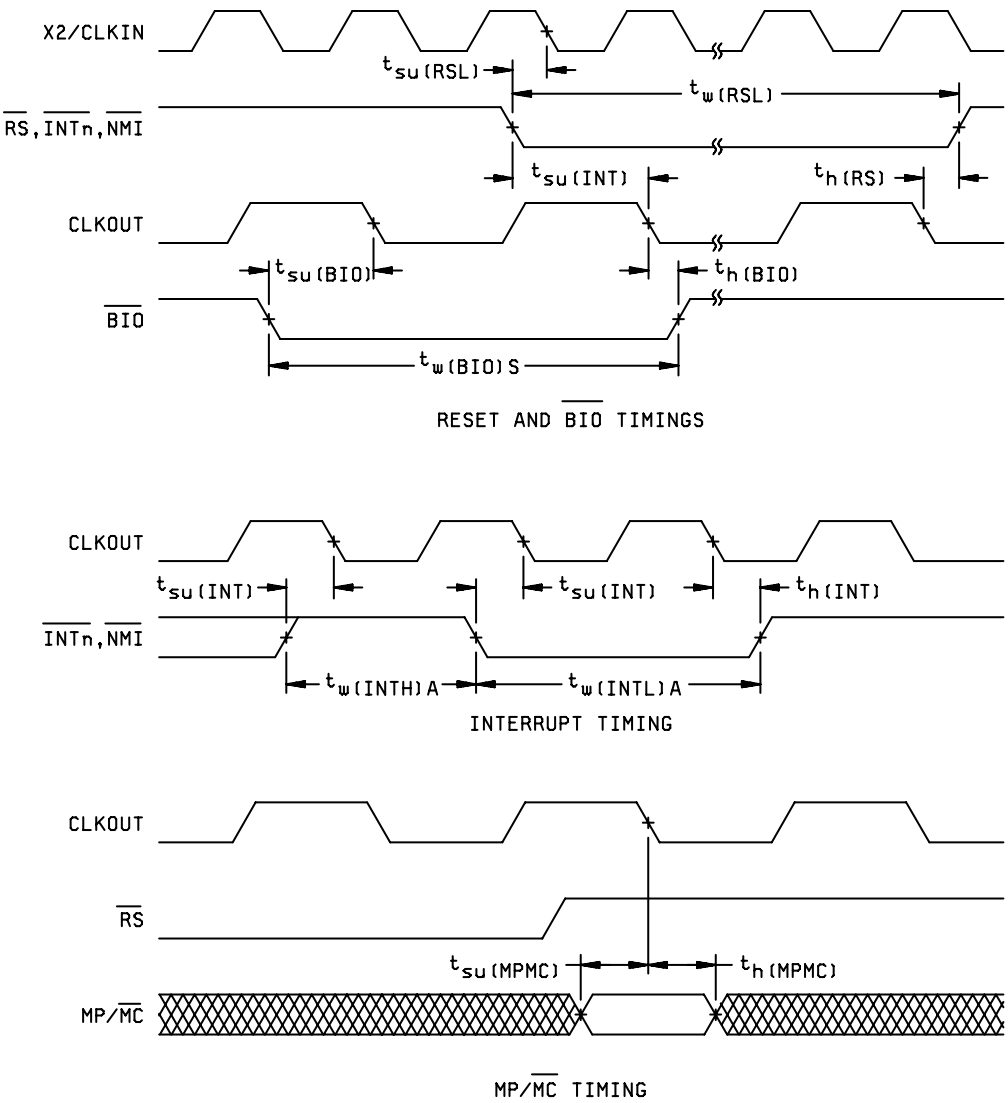
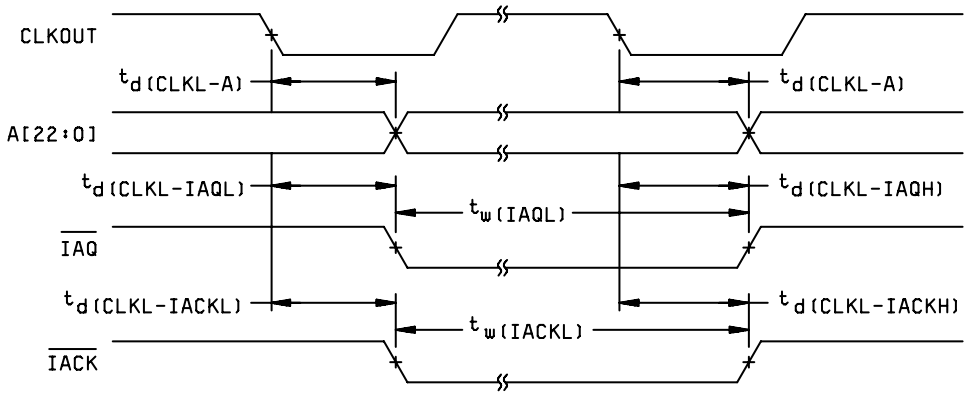
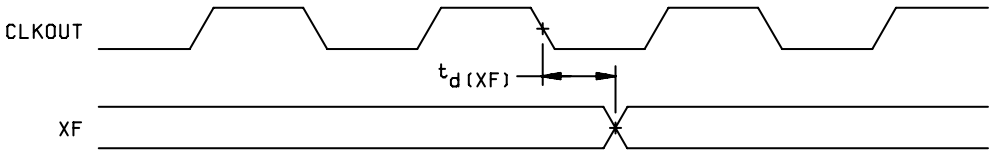


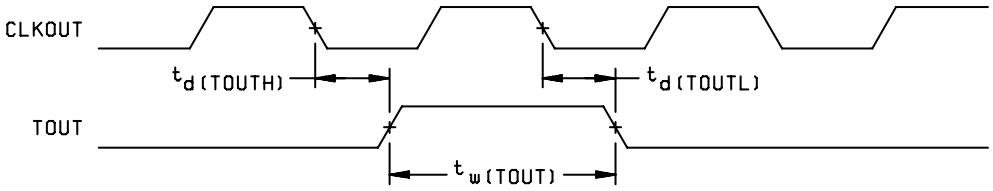
FIGURE 4. Test circuit and switching waveforms – Continued.



INSTRUCTION ACQUISITION ($\overline{IAQ}$) AND INTERRUPT ACKNOWLEDGE ($\overline{IACK}$) TIMINGS

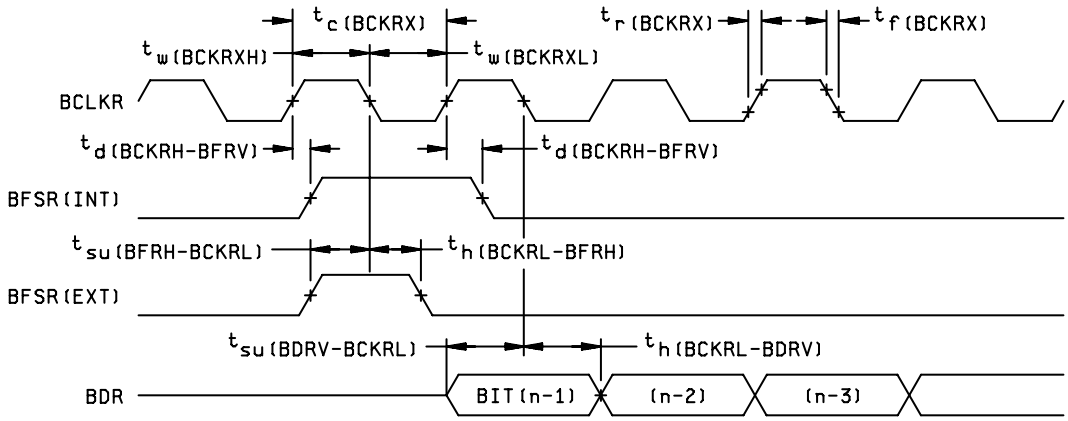


EXTERNAL FLAG (XF) TIMING

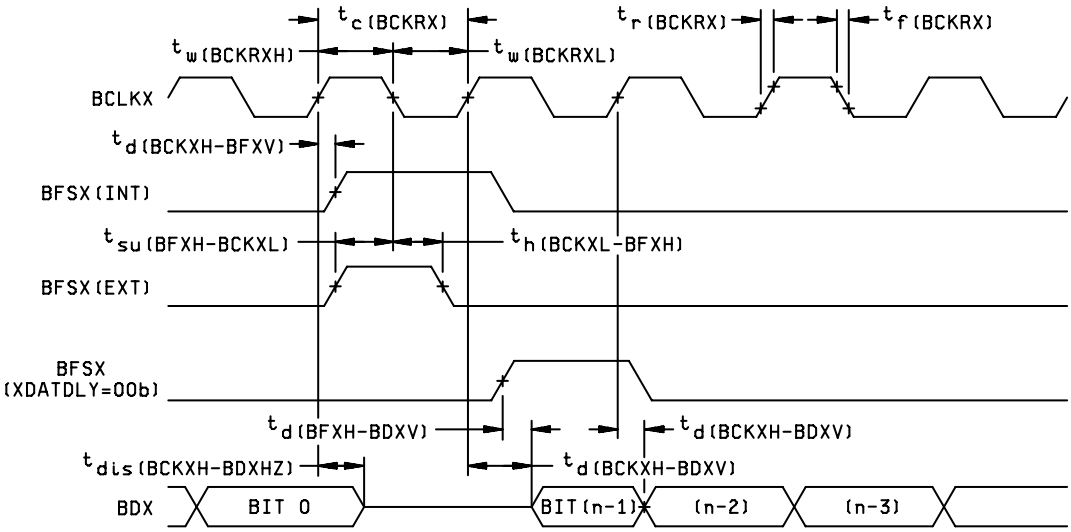


TOUT TIMING

FIGURE 4. Test circuit and switching waveforms – Continued.

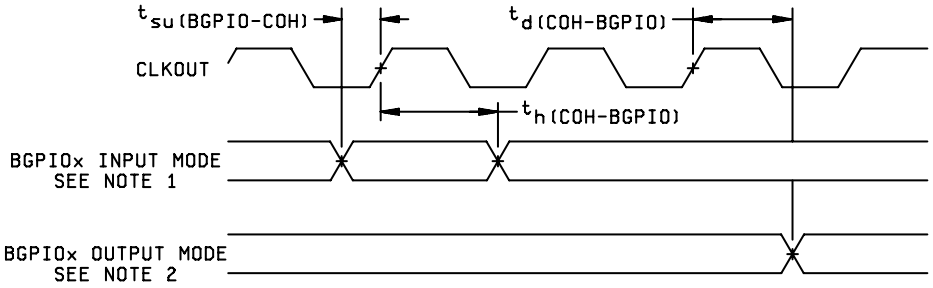


McBSP RECEIVE TIMINGS



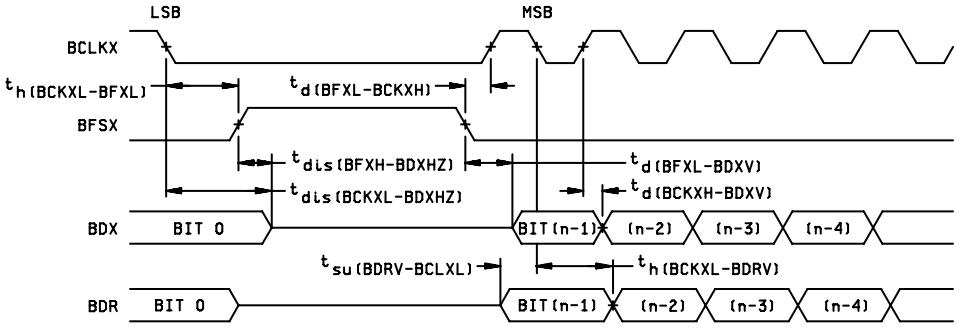
McBSP TRANSMIT TIMINGS

FIGURE 4. Test circuit and switching waveforms – Continued.

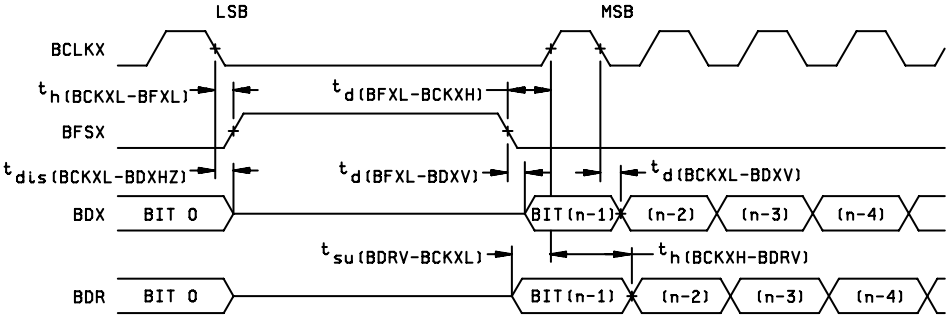


McBSP GENERAL PURPOSE I/O TIMINGS

Note 1. BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.
Note 2. BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx or BDXx when configured as a general-purpose output.

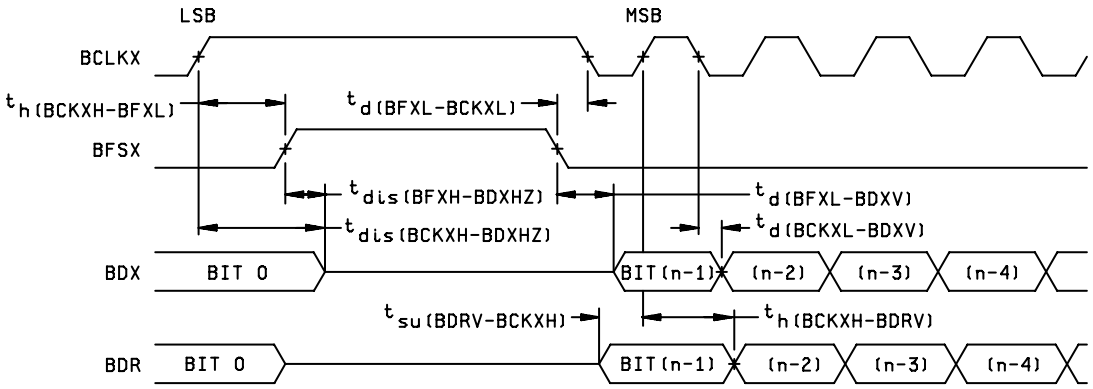


McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b,CLKXP=0

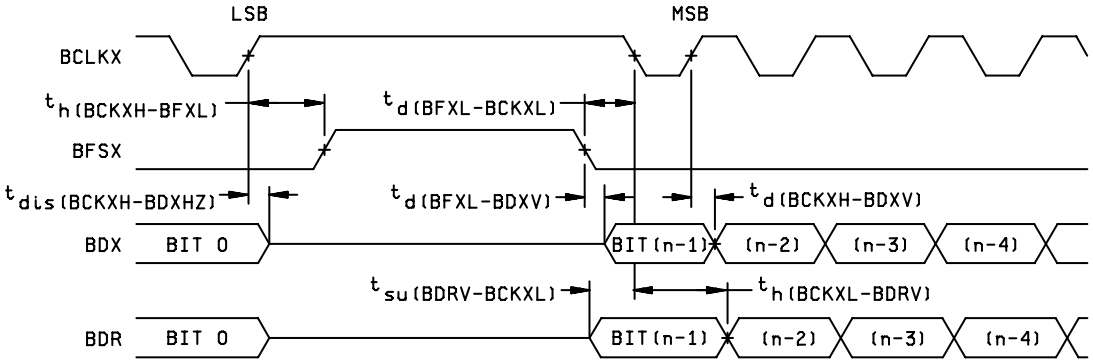


McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b,CLKXP=0

FIGURE 4. Test circuit and switching waveforms – Continued.

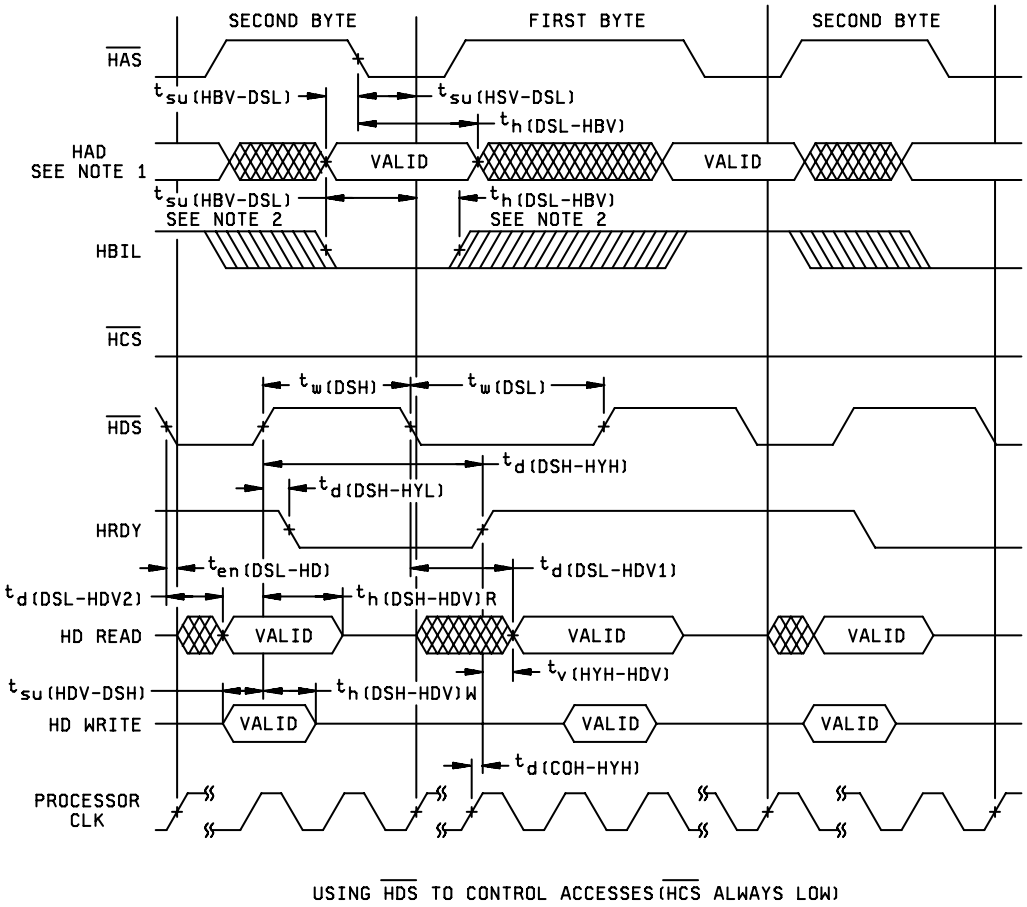


McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b,CLKXP=1



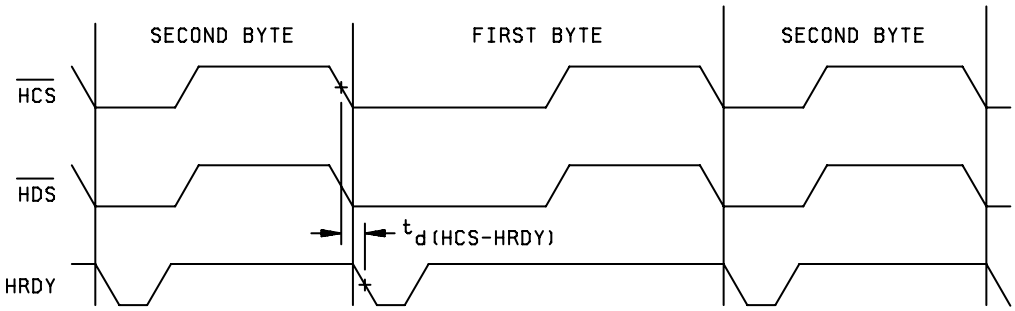
McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b,CLKXP=1

FIGURE 4. Test circuit and switching waveforms – Continued.

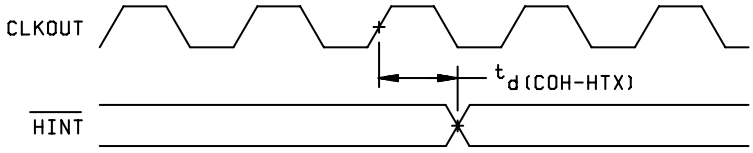


Note 1. HAD refers to HCNTL0, HCNTL1, and HR/$\overline{W}$.
Note 2. When HAS is not used (HAS always high).

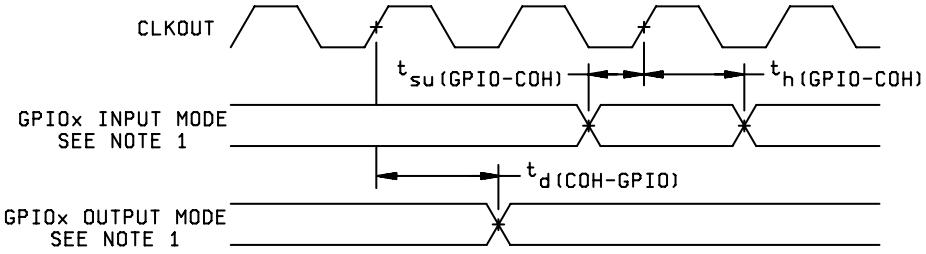
FIGURE 4. Test circuit and switching waveforms – Continued.



USING $\overline{HCS}$ TO CONTROL ACCESSES



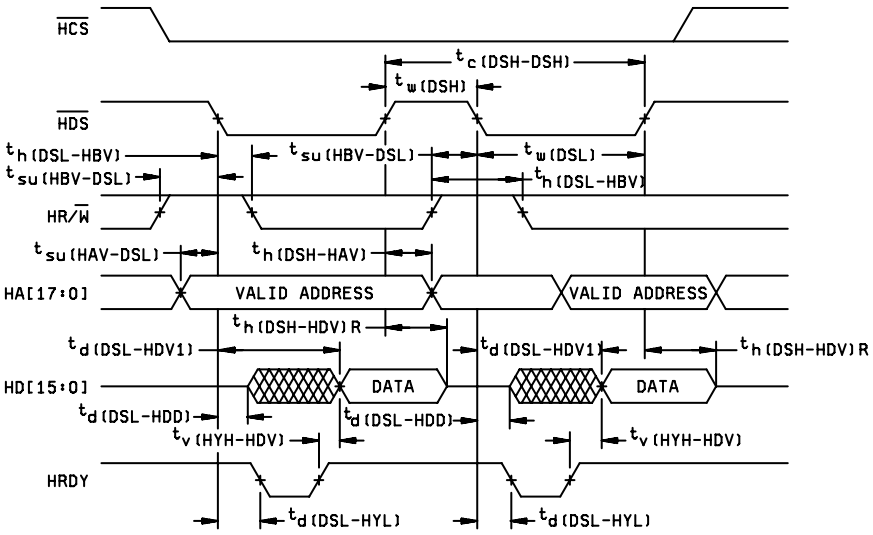
$\overline{HINT}$ TIMING



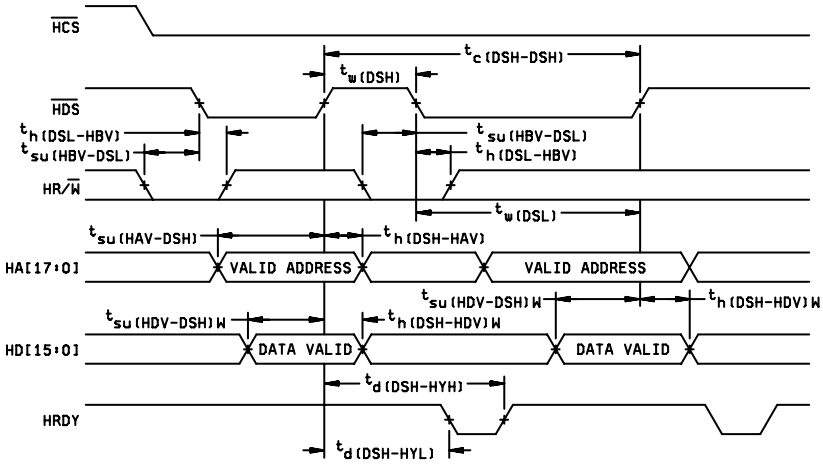
GPIOx TIMING
SEE NOTE 1

Note 1. GPIOx refers to HD0, HD1, HD2, HD7, when the HD bus is configured for general-purpose input/output (I/O).

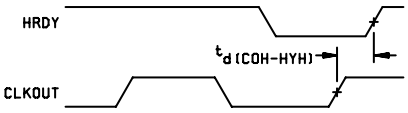
FIGURE 4. Test circuit and switching waveforms – Continued.



NONMULTIPLEXED READ TIMINGS



NONMULTIPLEXED WRITE TIMINGS



HRDY RELATIVE TO CLKOUT

FIGURE 4. Test circuit and switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of 5 devices with zero rejects shall be required.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-01-10

Approved sources of supply for SMD 5962-01530 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0153001QXA	01295	SMJ320VC5416HFG

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

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