

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update and part of five year review. tcr	07-02-07	Joseph Rodenbeck
B	Update drawing to meet current MIL-PRF-38535 requirements. - glg	15-07-10	Charles Saffle



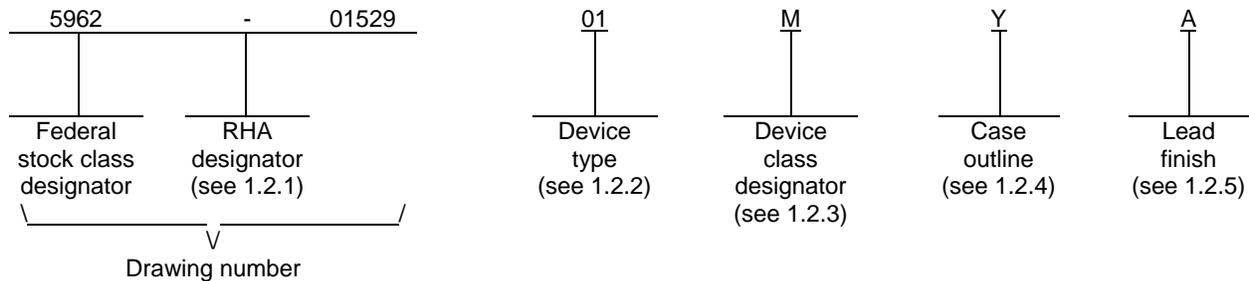
REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	
REV STATUS OF SHEETS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Kenneth Rice	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p> <p align="center"><b>MICROCIRCUIT, MEMORY, DIGITAL,                  CMOS, 16K X 1 STATIC RANDOM                  ACCESS MEMORY, (SRAM),                  MONOLITHIC SILICON</b></p>																
<p align="center"><b>STANDARD                  MICROCIRCUIT                  DRAWING</b></p> <p align="center">THIS DRAWING IS                  AVAILABLE                  FOR USE BY ALL                  DEPARTMENTS                  AND AGENCIES OF THE                  DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Raj Pithadia																	
	APPROVED BY Raymond Monnin																	
	DRAWING APPROVAL DATE 2001 December 12																	
	REVISION LEVEL B	SIZE A	CAGE CODE 67268	<b>5962-01529</b>														
		SHEET 1 OF 17																

## 1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	4C167	16K X 1 CMOS SRAM	45 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	CQCC3-N20	20	Rectangular leadless Chip-Carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.3 V dc to +7.0 V dc 2/
Storage temperature range .....	-65°C to +150°C
Maximum power dissipation ( $P_D$ ) .....	1.0 W
Lead temperature (soldering, 10 seconds) .....	+270°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+150°C 3/

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	4.5 V dc to 5.5 V dc
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of this document are available on line at <http://www.jedec.org> or from JEDEC - Solid State Technology Association, 3103 North 10<sup>th</sup> Street, Suite 247, Arlington, VA 22201)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
 2/ All voltages referenced to  $V_{SS}$ .  
 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Serialization for device class V. All class V devices shall be serialized in accordance with MIL-PRF-38535.

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

##### 4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 4.5 V to 5.5 V V <sub>SS</sub> = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I <sub>CC1</sub>	t <sub>AVAV</sub> = t <sub>AVAV</sub> (minimum), I <sub>O</sub> = 0.0 A, $\overline{CE} = V_{IL}$	1, 2, 3	01		155	mA
Standby power supply current TTL	I <sub>CC2</sub>	Address stable, I <sub>O</sub> = 0.0 A $\overline{CE} = \overline{WE} = V_{IH}$	1, 2, 3	All		20	mA
Input leakage current	I <sub>IL</sub>	V <sub>IN</sub> = 0 V to 5.5 V	1, 2, 3	All		±10	μA
High-impedance output leakage current	I <sub>OHZ</sub> I <sub>OLZ</sub>	V <sub>OUT</sub> = GND $\overline{CE} = V_{IH}$	1, 2, 3	All		±20	μA
Output high voltage	V <sub>OH</sub>	I <sub>OUT</sub> = -4.0 mA, V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 8.0 mA, V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.2 V	1, 2, 3	All		0.4	V
Low level input voltage	V <sub>IL</sub>		1, 2, 3	All		0.8	V
High level input voltage	V <sub>IH</sub>		1, 2, 3	All	2.2		V
Input capacitance <u>2/</u>	C <sub>IN</sub>	V <sub>CC</sub> = 0 V, V <sub>IN</sub> = GND f = 1.0 MHz, T <sub>C</sub> = 25°C, See 4.4.1e	4	All		8	pF
Output capacitance <u>2/</u>	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V, V <sub>CC</sub> = GND f = 1.0 MHz, T <sub>C</sub> = 25°C, See 4.4.1e	4	All		10	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 3/ 4/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 4.5 V to 5.5 V V <sub>SS</sub> = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read or write cycle time	t <sub>AVAV</sub>	See figure 3	9, 10, 11	01	45		ns
Address access time	t <sub>AVQV</sub>	See figure 3	9, 10, 11	01		45	ns
Chip enable access time	t <sub>ELQV</sub>		9, 10, 11	01		45	ns
Output hold after address change <u>2/</u>	t <sub>AVQX</sub>	See figure 3	9, 10, 11	01	2.0		ns
Chip enable to output active <u>2/</u>	t <sub>ELQX</sub>		9, 10, 11	01	2.0		ns
Chip disable to output In high-Z <u>2/</u>	t <sub>EHQZ</sub>		9, 10, 11	01	0	25	ns
Write pulse width	t <sub>WLWH</sub>		9, 10, 11	01	30		ns
Chip enable to end of write	t <sub>ELWH</sub>		9, 10, 11	01	35		ns
Data setup to end of write	t <sub>DVWH</sub>		9, 10, 11	01	25		ns
Data hold after end of write	t <sub>WHDX</sub>		9, 10, 11	01	5		ns
Address setup to end of write	t <sub>AVWH</sub>		9, 10, 11	01	35		ns
Address hold after end of write <u>2/</u>	t <sub>WHAV</sub>		9, 10, 11	01	5		ns
Write enable low to output in high-Z <u>2/</u>	t <sub>WLQZ</sub>		9, 10, 11	01		30	ns
Write enable high to output invalid <u>2/</u>	t <sub>WHQX</sub>		9, 10, 11	01	0		ns
Address setup before Write low	t <sub>AVWL</sub>		9, 10, 11	All	5		ns

1/ All voltages referenced to V<sub>SS</sub>.

2/ Tested initially and after any design or process change which may affect this parameter.

3/ AC measurements assume signal transition times of 5 ns or less and input pulse levels of 0 V to 3.0 V. Output timing reference is 1.5 V. See figure 5.

4/ For timing waveforms see figure 4.

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All device type	
All case outlines	
Terminal number	
1	A0
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	QOUT
9	$\overline{WE}$
10	$V_{SS}$
11	$\overline{CE}$
12	DIN
13	A7
14	A8
15	A9
16	A10
17	A11
18	A12
19	A13
20	VCC

FIGURE 1. Terminal connections.

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Device type 01

$\overline{\text{CE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
H	X	Standby	High Z	Standby
L	H	Read	D <sub>OUT</sub>	Active
L	L	Write	High Z	Active

H = Logic "1" state

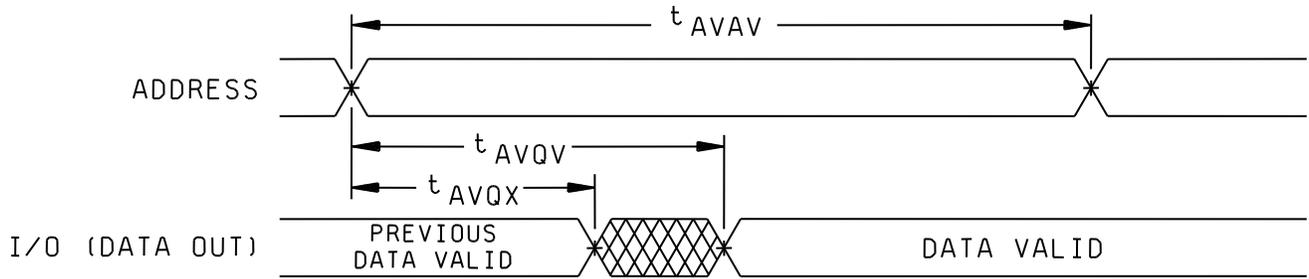
L = Logic "0" state

X = Don't care

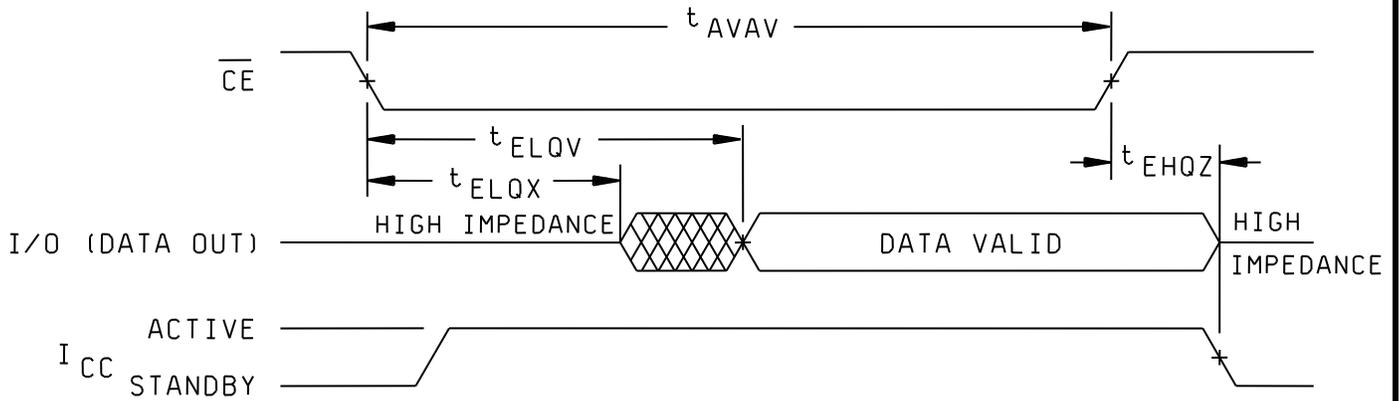
FIGURE 2. Truth table.

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READ CYCLE NO. 1 ( $\overline{WE}$  HIGH,  $\overline{CE}$  LOW) (See notes 1, 2, and 3)



READ CYCLE NO. 2 ( $\overline{WE}$  HIGH) (See notes 1 and 2)



NOTES:

1.  $\overline{WE}$  is high for entire cycle.
2.  $\overline{CE}$  and  $\overline{WE}$  must transition between  $V_{IH}$  (min) to  $V_{IL}$  (max) or  $V_{IL}$  (max) to  $V_{IH}$  (min) in monotonic fashion.
3. Device is continuously selected,  $\overline{CE}$  low.

FIGURE 3. Read cycle timing diagrams.

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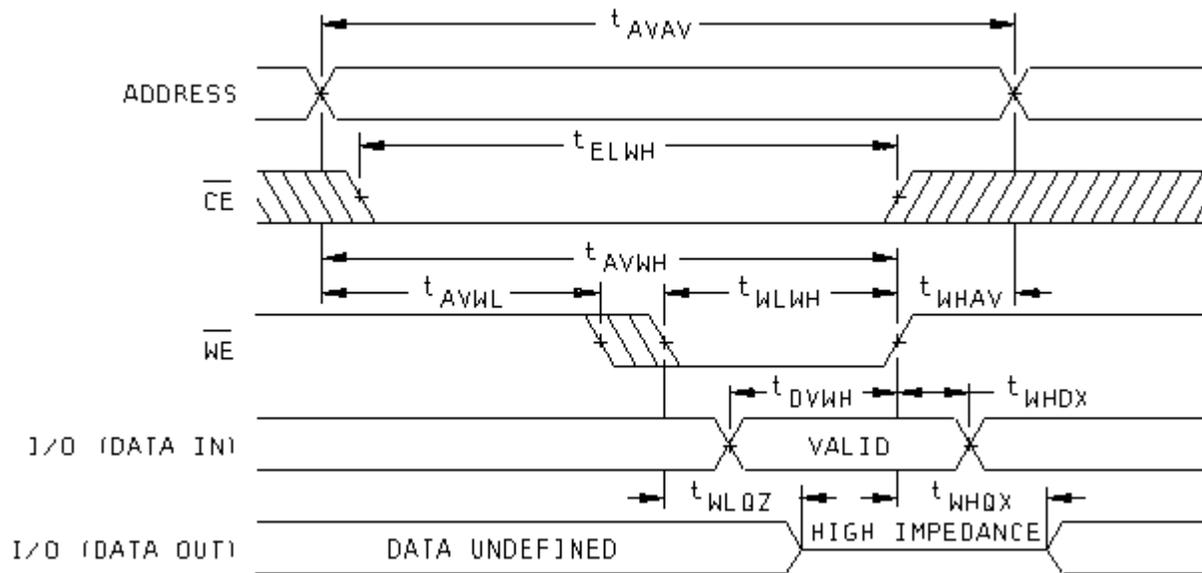
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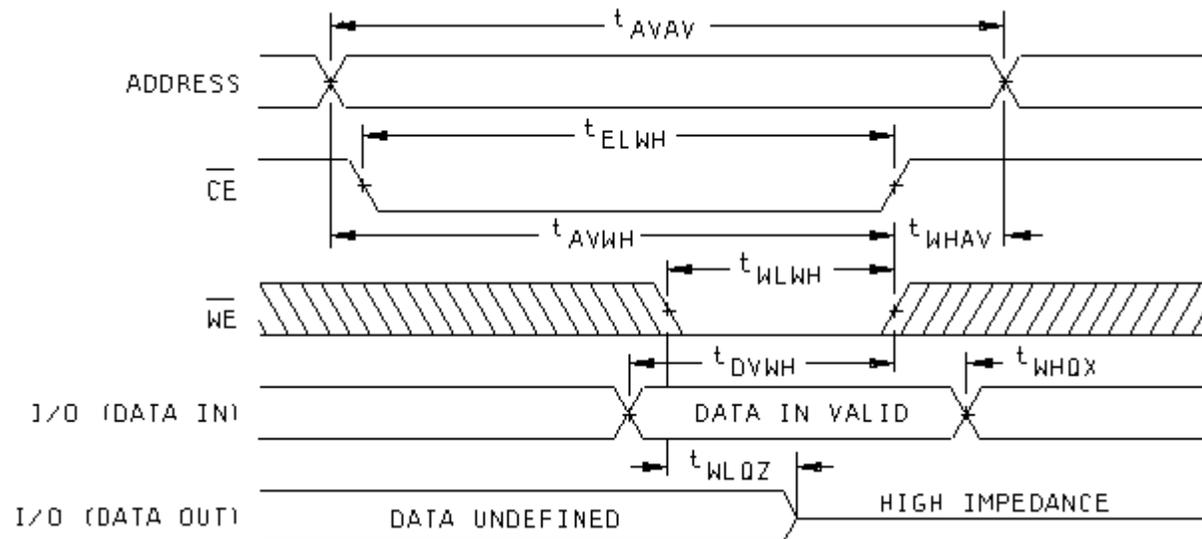
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WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED) (See notes 1 and 2)



WRITE CYCLE NO. 2 ( $\overline{CE}$  CONTROLLED) (See notes 1 and 2)



NOTES:

1.  $\overline{CE}$  and  $\overline{WE}$  must transition between  $V_{IH}$  (min) to  $V_{IL}$  (max) to  $V_{IH}$  (min) in monotonic fashion.
2.  $\overline{CE}$  and  $\overline{WE}$  must be  $\geq V_{IH}$  during address transitions.

FIGURE 4. Write cycle timing diagram.

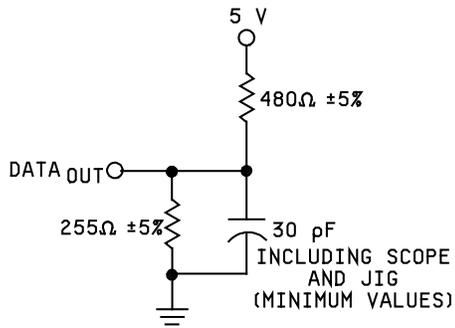
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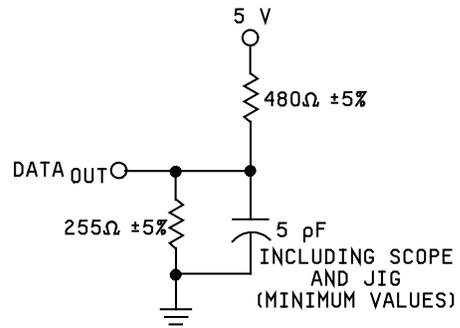
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CIRCUIT A

OUTPUT LOAD



CIRCUIT B

(for  $t_{ELQX}$ ,  $t_{WLQZ}$ ,  $t_{EHQZ}$ ,  $t_{WHQX}$ )

AC test conditions	
Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Output load circuits.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)		
		Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 9	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 8A, 10 or 1, 7, 9	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 8A, 10 or 1, 7, 9	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

- 1/ Blank spaces indicates tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed testers.
- 3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
- 4/ \* indicates PDA applies to subgroup 1 and 7.
- 5/ \*\* see 4.4.1e.
- 6/ Δ indicates delta limits (see table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
- 7/ See 4.4.1d.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD78 may be used for reference.
- e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

Table IIB. Delta limits at +25°C.

Test <sup>1/</sup>	All device types
$I_{CC3}$ standby	±10% of specified value in table IA
$I_{ILK}, I_{OLK}$	±10% of specified value in table IA

<sup>1/</sup> The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life test to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter test, subgroups 1, 7, and 9.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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APPENDIX A

APPENDIX A forms a part of 5962-01529

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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APPENDIX A - Continued

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A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-07-10

Approved sources of supply for SMD 5962-01529 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0152901MYA	3DTT2	P4C167-45L20MB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

Vendor name  
and address

3DTT2

Pyramid Semiconductor Corporation  
1249 Reamwood Avenue  
Sunnyvale, CA 94089

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