REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Changed input capacitance (C_{IN}) from 40 pF to 32 pF and Bi-directional (I/O) capacitance ($C_{I/O}$) from 20 pF to 16 pF. ksr	03-06-30	Raymond Monnin
E	Add device 02 and package Y. 5-year review boilerplate update. ksr	07-09-28	Robert Heber
F	Made changes to Figure 1 Case outline X dimensions A and A1. Corrected temperature symbol for device 01 from T_A to T_C in sections 1.3 and 1.4 also in Table IA. ksr	09-09-10	Charles F. Saffle
G	Added device 03. Added or modified existing paragraphs to accommodate the addition of device type 03. ksr	10-07-30	Charles F. Saffle
H	Update RHA features in section 1.5 and add SEP table IB. Update drawing to meet current MIL-PRF-38535 requirements. - glg	17-08-22	Charles F. Saffle
J	Corrections to Table IA and Figure 5. - glg	19-04-01	Charles F. Saffle
K	Update 1.2 through 1.5; Tables IA, IB, and IIB; and Figures 1, 4, and 5 for increased RHA and addition of device 04. EOL device type 02-03 due to die revision. Update to current MIL-PRF-38535 requirements. - llb	20-07-09	James R. Eschmeyer

REV																				
SHEET																				
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

REV STATUS	REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Gary Gross

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
00-12-19

REVISION LEVEL
K

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K x 32-BIT, RADIATION-HARDENED SRAM, MULTICHIP MODULE

SIZE	CAGE CODE	
A	**67268**	**5962-01511**

SHEET 1 OF 33

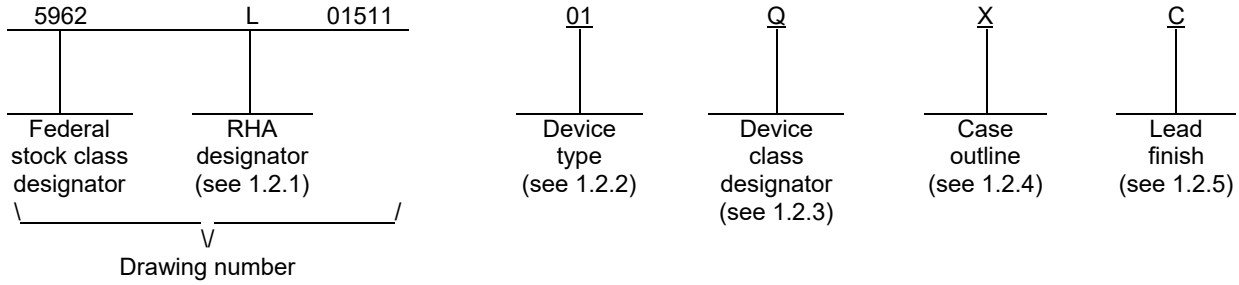
DSCC FORM 2233
APR 97

5962-E262-20

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	9Q512K32	512K X 32-bit Radiation-hardened SRAM	25 ns
02	9Q512K32E	512K X 32-bit Radiation-hardened SRAM	25 ns
03	9Q512K32E	512K X 32-bit Radiation-hardened SRAM	25 ns 2/
04	9Q512K32E	512K X 32-bit Radiation-hardened SRAM	25 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Dual cavity quad flat pack
Y	See figure 1	68	Dual cavity quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.
2/ Device type 03 provides QML class Q product with additional testing as specified in paragraph 4.2.1d herein.

1.3 Absolute maximum ratings. 3/ 4/

Supply voltage range, (V_{DD})	-0.5 V dc to +7.0 V dc
Voltage range on any input pin	-0.5 V dc to +7.0 V dc
Voltage range on any output pin	-0.5 V dc to +7.0 V dc
Input current, dc	+ 10 mA
Power dissipation	1.0 W per byte 5/
Operating case temperature range, (T_C) Device 01	-40°C to +125°C
Operating case temperature range, (T_C) Devices 02, 03 and 04	-40°C to +105°C
Storage temperature range, (T_{STG})	-65°C to +150°C
Junction temperature, (T_J)	+150°C
Thermal resistance, junction-to-case, (θ_{JC}): Cases X and Y	+10°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{DD})	+4.5 V dc to +5.5 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to V_{DD}
Operating case temperature, (T_C) Device 01	-40°C to +125°C
Operating case temperature, (T_C) Devices 02, 03 and 04	-40°C to +105°C

1.5 Radiation features

Maximum total dose available (dose rate = 50 – 300 Rad(Si)/s):	
For device types 01 – 03	50 krads(Si) 6/
For device types 04	100 krads 6/
Single event phenomenon (SEP):	
For device type 01:	
No SEL occur at effective LET (see 4.4.4.2)	≤ 80 MeV-cm^2/mg 7/
No SEU at threshold LET (see 4.4.4.2)	≤ 1 MeV-cm^2/mg 7/
For device types 02, 03 and 04:	
No SEL occur at effective LET (see 4.4.4.2)	≤ 110 MeV-cm^2/mg 7/
No SEU at threshold LET (see 4.4.4.2)	≤ 2.8 MeV-cm^2/mg 7/

1.6 Digital logic testing for device classes T, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ All voltage values in this drawing are with respect to V_{SS}.
5/ This part is capable of being used in a X 8, X 16, X 24, or X 32 configuration. When used in a X 8-bit configuration, the power dissipation is 1.0 W when used in a X 16-bit configuration, the power dissipation is 2.0 W.
6/ The manufacturer supplying device types 01, 02, and 03 has performed total ionizing dose(TID) test wafer by wafer basis in accordance with MIL-STD-883 method 1019 condition A to a maximum total dose of 50 krads(Si). However, device type 04 has performed total ionizing dose(TID) test as a wafer lot acceptance in accordance with MIL-STD-883 method 1019 condition A to a maximum total dose of 100 krads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.
7/ Contact the device manufacturer for detailed lot information.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation test circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q, T and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions (Device 01) $-40°C \le T_C \le +125°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}			1, 2, 3	01	2.0		V
			M, D, P, L	1 1/		2/		
Low-level input voltage	V_{IL}			1, 2, 3	01		0.8	V
			M, D, P, L	1 1/			2/	
High-level output voltage	V_{OH1}	I_{OH} = -4mA, V_{DD} = 4.5 V		1, 2, 3	01	2.4		V
			M, D, P, L	1 1/		2/		
High-level output voltage	V_{OH2}	I_{OH} = -200µA, V_{DD} = 4.5 V		1, 2, 3	01	3.0		V
			M, D, P, L	1 1/		2/		
Low-level output voltage	V_{OL1}	I_{OL} = 8.0mA, V_{DD} = 4.5 V		1, 2, 3	01		0.4	V
			M, D, P, L	1 1/			2/	
Low-level output voltage	V_{OL2}	I_{OL} = 200 µA, V_{DD} = 4.5V		1, 2, 3	01		0.08	V
			M, D, P, L	1 1/			2/	
Input capacitance	C_{IN}	see 4.4.1e,	V_{IN} = 25 mV	4	01		32	pF
Bi-directional I/O capacitance	$C_{I/O}$	f = 1 MHz at 0 V, T_C = 25°C 3/	$V_{I/O}$ = 25 mV	4	01		16	pF
Input current (leakage)	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$		1, 2, 3	01	-2.0	+2.0	µA
		$V_{DD} = V_{DD}$ (max)	M, D, P, L	1 1/		2/	2/	
Three-state output current (leakage)	I_{OZ}	0 V ≤ V_O ≤ V_{DD}, $V_{DD} = V_{DD}$ (max)		1, 2, 3	01	-2.0	+2.0	µA
		$\overline{G} = V_{DD}$ (max)	M, D, P, L	1 1/		2/	2/	
Short-circuit output current 4/ 5/	I_{OS}	0 V ≤ V_O ≤ V_{DD}		1, 2, 3	01	-90	+90	mA
			M, D, P, L	1 1/		2/	2/	
Operating supply current at 1 MHz (per byte) 6/	I_{DD}	Inputs: $V_{IL} = V_{SS}$ + 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA		1, 2, 3	01		125	mA
		$V_{DD} = V_{DD}$ (max)	M, D, P, L	1 1/			2/	
Operating supply current at 40 MHz (per byte) 6/	I_{DD1}	Inputs: $V_{IL} = V_{SS}$ + 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA		1, 2, 3	01		180	mA
		$V_{DD} = V_{DD}$ (max)	M, D, P, L	1 1/			2/	
Standby supply current at 0 MHz (per byte) 6/	I_{DD2}	$\overline{E} = V_{DD}$ -0.5 V, $V_{DD} = V_{DD}$(max)		1, 3	01		6	mA
		$V_{IH} = V_{DD}$ -0.5 V	M, D, P, L	1 1/			2/	
		Inputs: $V_{IL} = V_{SS}$		2			12	mA
		I_{OUT} = 0 mA	M, D, P, L	1 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions (Device 01) $-40°C \le T_C \le +125°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test		See 4.4.1c, $V_{IH} = V_{DD}$ -0.5 V	7, 8A, 8B	01			
		M, D, P, L	7 1/			2/	
Read cycle time 7/	t_{AVAV}	See figures 4 and 5	9, 10, 11	01	25		ns
		M, D, P, L	9 1/		2/		
Read access time	t_{AVQV}		9, 10, 11	01		25	ns
		M, D, P, L	9 1/			2/	
Output hold time	t_{AXQX}		9, 10, 11	01	3		ns
		M, D, P, L	9 1/		2/		
$\overline{G}$-controlled output enable time 8/	t_{GLQX}		9, 10, 11	01	0		ns
		M, D, P, L	9 1/		2/		
$\overline{G}$-controlled output enable time (read cycle 3)	t_{GLQV}		9, 10, 11	01		10	ns
		M, D, P, L	9 1/			2/	
$\overline{G}$-controlled output three-state time 8/	t_{GHQZ}		9, 10, 11	01		10	ns
		M, D, P, L	9 1/			2/	
$\overline{E}$-controlled output enable time 8/ 9/	t_{ETQX}		9, 10, 11	01	3		ns
		M, D, P, L	9 1/		2/		
$\overline{E}$-controlled access time 9/	t_{ETQV}		9, 10, 11	01		25	ns
		M, D, P, L	9 1/			2/	
$\overline{E}$-controlled output three-state time 7/ 8/ 10/	t_{EFQZ}		9, 10, 11	01		10	ns
		M, D, P, L	9 1/			2/	
Write cycle time 11/	t_{AVAV}		9, 10, 11	01	25		ns
		M, D, P, L	9 1/		2/		
Device enable to end of write	t_{ETWH}		9, 10, 11	01	20		ns
		M, D, P, L	9 1/		2/		
Address setup time for write ($\overline{E}$-controlled)	t_{AVET}		9, 10, 11	01	1		ns
		M, D, P, L	9 1/		2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions (Device 01) $-40°C \le T_C \le +125°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}	See figures 4 and 5	9, 10, 11	01	0		ns
		M, D, P, L	9 1/		2/		
Write pulse width	t_{WLWH}		9, 10, 11	01	20		ns
		M, D, P, L	9 1/		2/		
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	01	0		ns
		M, D, P, L	9 1/		2/		
Address hold time for device enable ($\overline{E}$-controlled)	t_{EFAX}		9, 10, 11	01	0		ns
		M, D, P, L	9 1/		2/		
$\overline{W}$-controlled three-state time 8/	t_{WLQZ}		9, 10, 11	01		10	ns
		M, D, P, L	9 1/			2/	
$\overline{W}$-controlled output enable time 8/	t_{WHQX}		9, 10, 11	01	5		ns
		M, D, P, L	9 1/		2/		
Device enable pulse width ($\overline{E}$-controlled)	t_{ETEF}		9, 10, 11	01	20		ns
		M, D, P, L	9 1/		2/		
Data setup time	t_{DVWH}		9, 10, 11	01	15		ns
		M, D, P, L	9 1/		2/		
Data hold time	t_{WHDX}		9, 10, 11	01	2		ns
		M, D, P, L	9 1/		2/		
Device enable controlled write pulse width	t_{WLEF}		9, 10, 11	01	20		ns
		M, D, P, L	9 1/		2/		
Data setup time	t_{DVEF}		9, 10, 11	01	15		ns
		M, D, P, L	9 1/		2/		
Data hold time	t_{EFDX}		9, 10, 11	01	2		ns
		M, D, P, L	9 1/		2/		
Address valid to end of write	t_{AVWH}		9, 10, 11	01	20		ns
		M, D, P, L	9 1/		2/		
Write disable time 11/	t_{WHWL}		9, 10, 11	01	5		ns
		M, D, P, L	9 1/		2/		

See footnotes at end of table.

The following pages of Table IA reference devices 02 – 04; the footnotes at the end of the table apply to all of Table IA.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions (Devices 02 – 04) $-40°C \le T_C \le +105°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}			1, 2, 3	02 – 04	2.0		V
			M, D, P, L, R	1 1/		2/		
Low-level input voltage	V_{IL}			1, 2, 3	02 – 04		0.8	V
			M, D, P, L, R	1 1/			2/	
High-level output voltage	V_{OH1}	I_{OH} = -4 mA, V_{DD} = 4.5 V		1, 2, 3	02 – 04	2.4		V
			M, D, P, L, R	1 1/		2/		
High-level output voltage	V_{OH2}	I_{OH} = -200 µA, V_{DD} = 4.5 V		1, 2, 3	02 – 04	3.0		V
			M, D, P, L, R	1 1/		2/		
Low-level output voltage	V_{OL1}	I_{OL} = 8.0 mA, V_{DD} = 4.5 L		1, 2, 3	02 – 04		0.4	V
			M, D, P, L, R	1 1/			2/	
Low-level output voltage	V_{OL2}	I_{OL} = 200 µA, V_{DD} = 4.5 V		1, 2, 3	02 – 04		0.08	V
			M, D, P, L, R	1 1/			2	
Input capacitance	C_{IN}	See 4.4.1e	V_{IN} = 25 mV	4	02, 03		45	pF
Input capacitance, All address and Output Enable pins	C_{IN1}	See 4.4.1e, f = 1 MHz at 0V, T_C = 25°C 3/	V_{IN} = 25 mV	4	04		45	pF
Input capacitance, All Enable and Write Enable pins	C_{IN2}	See 4.4.1e, f = 1 MHz at 0 V T_C = 25°C 3/	V_{IN} = 25 mV	4	04		18	pF
Bi-directional I/O capacitance	$C_{I/O}$	f = 1 MHz at 0 V	$V_{I/O}$ = 25 mV	4	02 – 04		25	pF
Input current (leakage)	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$		1, 2, 3	02 – 04	-2.0	+2.0	µA
		$V_{DD} = V_{DD}$(max)	M, D, P, L, R	1 1/		2/	2/	
Three-state output current (leakage)	I_{OZ}	0 V ≤ $V_O \le V_{DD}$, $V_{DD} = V_{DD}$(max)		1, 2, 3	02 – 04	-2.0	+2.0	µA
		$\overline{G} = V_{DD}$(max)	M, D, P, L, R	1 1/		2/	2/	
Short-circuit output current 4/ 5/	I_{OS}	0 V ≤ $V_O \le V_{DD}$		1, 2, 3	02 – 04	-90	+90	mA
			M, D, P, L, R	1 1/		2/	2/	
Operating supply current at at 1 MHz (per byte) 6/	I_{DD}	Inputs: $V_{IL} = V_{SS}$ + 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA		1, 2, 3	02 – 04		40	mA
		$V_{DD} = V_{DD}$(max)	M, D, P, L, R	1 1/			2/	
Operating supply current at 40 MHz (per byte) 6/	I_{DD1}	Inputs: $V_{IL} = V_{SS}$ + 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA		1, 2, 3	02 – 04		70	mA
		$V_{DD} = V_{DD}$(max)	M, D, P, L, R	1 1/			2/	
Standby supply current at 0 MHz (per byte) 6/	I_{DD2}	Inputs: $V_{IL} = V_{SS}$		1, 3	02, 03		9	mA
		I_{OUT} = 0 mA	M, D, P, L, R	1 1/			2/	
		$\overline{E} = V_{DD}$ -0.5 V, $V_{DD} = V_{DD}$(max)		1, 3	04		16	
		$V_{IH} = V_{DD}$ -0.5 V	M, D, P, L, R	1 1/			2/	
				2	02 – 04		24	
			M, D, P, L, R	1 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions (Devices 02 – 04) $-40°C \le T_C \le +105°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test		See 4.4.1c, $V_{IH} = V_{DD}$ -0.5 V	7, 8A, 8B	02 – 04			
		M, D, P, L, R	7 1/			2/	
Read cycle time 7/ 13/	t_{AVAV}	See figures 4 and 5	9, 10, 11	02 – 04	25		ns
		M, D, P, L, R	9 1/		2/		
Address valid to address valid skew time 12/	t_{AVSK}		9, 10, 11	02 – 04		4	ns
		M, D, P, L, R	9 1/			2/	
Read access time	t_{AVQV}		9, 10, 11	02 – 04		25	ns
		M, D, P, L, R	9 1/			2/	
Output hold time	t_{AXQX}		9, 10, 11	02 – 04	3		ns
		M, D, P, L, R	9 1/		2/		
$\overline{G}$-controlled output enable time 8/	t_{GLQX}		9, 10, 11	02 – 04	0		ns
		M, D, P, L, R	9 1/		2/		
$\overline{G}$-controlled output enable time (read cycle 3)	t_{GLQV}		9, 10, 11	02 – 04		10	ns
		M, D, P, L, R	9 1/			2/	
$\overline{G}$-controlled output three-state time 8/	t_{GHQZ}		9, 10, 11	02 – 04		10	ns
		M, D, P, L, R	9 1/			2/	
$\overline{E}$-controlled output enable time 8/ 9/	t_{ETQX}		9, 10, 11	02 – 04	3		ns
		M, D, P, L, R	9 1/		2/		
$\overline{E}$-controlled address setup time for read 12/	t_{AVET2}		9, 10, 11	02 – 04	-4		ns
		M, D, P, L, R	9 1/		2/		
$\overline{E}$-controlled access time 9/	t_{ETQV}		9, 10, 11	02 – 04		25	ns
		M, D, P, L, R	9 1/			2/	
$\overline{E}$-controlled output three-state time 7/ 8/ 10/	t_{EFQZ}		9, 10, 11	02 – 04		10	ns
		M, D, P, L, R	9 1/			2/	
Write cycle time 11/	t_{AVAV}		9, 10, 11	02 – 04	25		ns
		M, D, P, L, R	9 1/		2/		
Device enable to end of write	t_{ETWH}		9, 10, 11	02 – 04	20		ns
		M, D, P, L, R	9 1/		2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions (Devices 02 – 04) $-40°C \le T_C \le +105°C$ $+4.5°V \le V_{DD} \le +5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup time for write ($\overline{E}$-controlled)	t_{AVET}	See figures 4 and 5	9, 10, 11	02 – 04	1		ns
		M, D, P, L, R	9 1/		2/		
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}		9, 10, 11	02 – 04	0		ns
		M, D, P, L, R	9 1/		2/		
Write pulse width	t_{WLWH}		9, 10, 11	02 – 04	20		ns
		M, D, P, L, R	9 1/		2/		
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	02 – 04	0		ns
		M, D, P, L, R	9 1/		2/		
Address hold time for device enable ($\overline{E}$-controlled)	t_{EFAX}		9, 10, 11	02 – 04	0		ns
		M, D, P, L, R	9 1/		2/		
$\overline{W}$-controlled three-state time 8/	t_{WLQZ}		9, 10, 11	02 – 04		10	ns
		M, D, P, L, R	9 1/			2/	
$\overline{W}$-controlled output enable time 8/	t_{WHQX}		9, 10, 11	02 – 04	5		ns
		M, D, P, L, R	9 1/		2/		
Device enable pulse width ($\overline{E}$-controlled)	t_{ETEF}		9, 10, 11	02 – 04	20		ns
		M, D, P, L, R	9 1/		2/		
Data setup time	t_{DVWH}		9, 10, 11	02 – 04	15		ns
		M, D, P, L, R	9 1/		2/		
Data hold time	t_{WHDX}		9, 10, 11	02 – 04	2		ns
		M, D, P, L, R	9 1/		2/		
Device enable controlled write pulse width	t_{WLEF}		9, 10, 11	02 – 04	20		ns
		M, D, P, L, R	9 1/		2/		
Data setup time	t_{DVEF}		9, 10, 11	02 – 04	15		ns
		M, D, P, L, R	9 1/		2/		
Data hold time	t_{EFDX}		9, 10, 11	02 – 04	2		ns
		M, D, P, L, R	9 1/		2/		
Address valid to end of write	t_{AVWH}		9, 10, 11	02 – 04	20		ns
		M, D, P, L, R	9 1/		2/		
Write disable time 11/	t_{WHWL}		9, 10, 11	02 – 04	5		ns
		M, D, P, L, R	9 1/		2/		

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C. For devices 02 – 04, the post irradiation limits are based on the hot spec for I_{DD}.
2/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values, unless otherwise specified.
3/ Measured only for initial qualification and after any design or process changes which may affect this parameter.
4/ Supplied as a design limit but not guaranteed or tested.
5/ Not more than one output may be shorted at a time for maximum duration of one second.
6/ This part is capable of being used in a X 8, X 16, X 24, or X 32 configuration. When used in a X 8-bit configuration, the supply current is as stated in table IA; if used in a X 16-bit configuration, the listed supply current is doubled, etc.

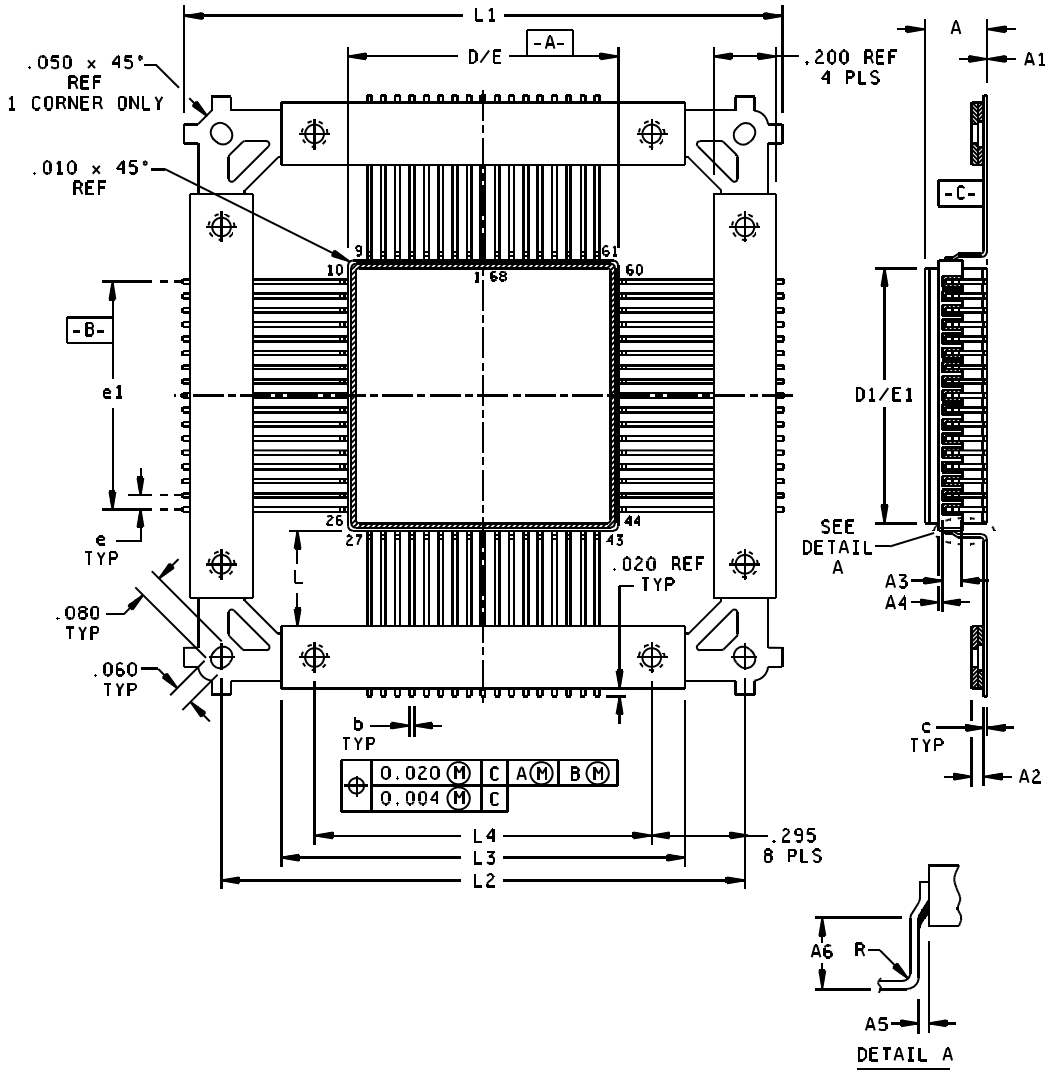
7/ This is a functional test.
8/ See figure 5, timing waveforms (High-Z to active level and active to High-Z level waveform).
9/ The ET (enable true) notation refers to the falling edge of $\overline{E}$. SEU immunity does not affect the read parameters.
10/ The EF (enable false) notation refers to the rising edge of $\overline{E}$. SEU immunity does not affect the read parameters.
11/ Functional test performed with outputs disabled ($\overline{G}$ high).
12/ Guaranteed by design.
13/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation.
14/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

Table IB. SEP test limits. 1/ 2/

Device type	Single Event Upset (SEU) V_{DD} = 4.5 V 3/ No single event upsets (SEU) occurs at threshold LET	Single Event Latch-up (SEL) Bias V_{DD} = 5.5 V 4/ No single event latch-up occurs at effective LET
01	LET ≤ 1.0 MeV/(mg/cm^2)	LET ≤ 80 MeV/(mg/cm^2)
02 – 04	LET ≤ 2.8 MeV/(mg/cm^2)	LET ≤ 110 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved TRB and qualifying activity.
3/ Test temperatures T_A = +25°C ±10°C.
4/ Worst case test temperature T_A = +125°C ±10°C.
5/ Manufacturer also performed heavy ion SEE (SEL, SEU) test and for detailed information of SEE test contact device manufacturer.

Case outline X



Notes:

1. All exposed metallized areas must be gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid and slug are electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Letter designations are provided to cross reference to MIL-STD-1835.
5. Lead position and co-planarity are not measured.
6. Tie bar corners may have notches and tabs different than shown.
7. Package shipped with non-conductive strip. Leads are not trimmed and shall not have been repaired.
8. Constant acceleration method 2001 of MIL-STD-883 shall be performed to condition D.

FIGURE 1. Case outlines.

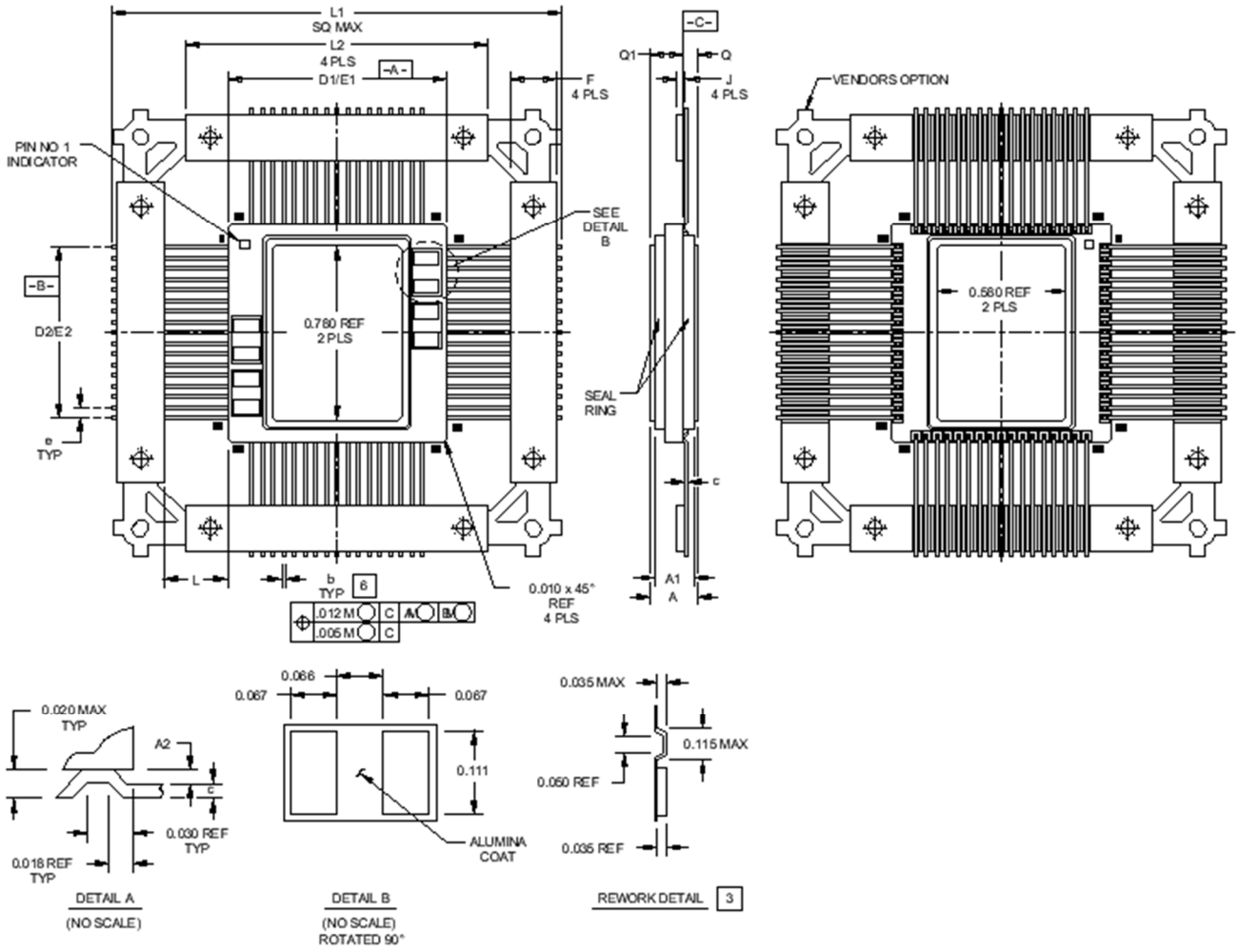
Case outline X – continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.80	5.61	.189	.221
A1	.254	.559	.010	.022
A2	.762	1.02	.030	.040
A3	.254		.010	
A4	1.524		.060	
A5	.254		.010	
A6	1.78	2.29	.070	.090
b	.330	.432	.013	.017
c	.178	.254	.007	.010
D/E	22.12	22.58	.871	.889
D1/E1	21.13	21.54	.832	.848
e	1.27 BSC		.050 BSC	
e1	20.32		.800	
L	7.75 REF		.305 REF	
L1	48.46	49.58	1.908	1.952
L2	42.49	43.36	1.673	1.707
L3	33.27		1.310	
L4	27.66	28.22	1.089	1.111
R	.254		.010	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outlines – Continued.

Case outline Y



Notes:
1. All exposed metalized areas are gold plated over nickel plating per MIL-PRF-38535.
2. Both lids are electrically connected to V_{SS}.
3. Packages may be shipped with repaired leads as shown.
4. Coplanarity requirements do not apply in repaired area.
5. Letter designations are to cross reference to MIL-STD-1835.
6. Lead true position tolerances and coplanarity are not measured.
7. Capacitor pads are sized to fit CDR32 (1206) capacitors.
8. Constant acceleration method 2001 of MIL-STD-883 shall be performed to condition D.
9. Resistance to Solderability method 2036 of MIL-STD-883 shall be performed to condition I.

FIGURE 1. Case outlines – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.775	5.842	.188	.230
A1	3.962	4.876	.156	.192
A2	.203 REF		.008 REF	
b	.330	.432	.013	.017
c	.178	.254	.007	.010
D1/E1	24.638	25.146	.970	.990
D2/E2	20.32 BSC		.800 BSC	
e	1.27 BSC		.050 BSC	
F	4.826 REF		0.190 REF	
J	.762	1.016	.030	.040
L	7.62		.300	
L1		51.993		2.047
L2	35.814		1.410	
Q	1.65 REF		.065 REF	
Q1	3.68 REF		.145 REF	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outlines – Continued.

Device types	01	Device types	01
Case outlines	X	Case outlines	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	35	$\overline{G}$
2	$\overline{E2}$	36	$\overline{E1}$
3	A5	37	A17
4	A4	38	$\overline{W1}$
5	A3	39	$\overline{W2}$
6	A2	40	$\overline{W3}$
7	A1	41	A18
8	A0	42	NC
9	NC	43	NC
10	DQ0(0)	44	DQ7(3)
11	DQ1(0)	45	DQ6(3)
12	DQ2(0)	46	DQ5(3)
13	DQ3(0)	47	DQ4(3)
14	DQ4(0)	48	DQ3(3)
15	DQ5(0)	49	DQ2(3)
16	DQ6(0)	50	DQ1(3)
17	DQ7(0)	51	DQ0(3)
18	V_{SS}	52	V_{SS}
19	DQ0(1)	53	DQ7(2)
20	DQ1(1)	54	DQ6(2)
21	DQ2(1)	55	DQ5(2)
22	DQ3(1)	56	DQ4(2)
23	DQ4(1)	57	DQ3(2)
24	DQ5(1)	58	DQ2(2)
25	DQ6(1)	59	DQ1(2)
26	DQ7(1)	60	DQ0(2)
27	V_{DD}	61	V_{DD}
28	A11	62	A10
29	A12	63	A9
30	A13	64	A8
31	A14	65	A7
32	A15	66	A6
33	A16	67	$\overline{W0}$
34	$\overline{E0}$	68	$\overline{E3}$

FIGURE 2. Terminal connections.

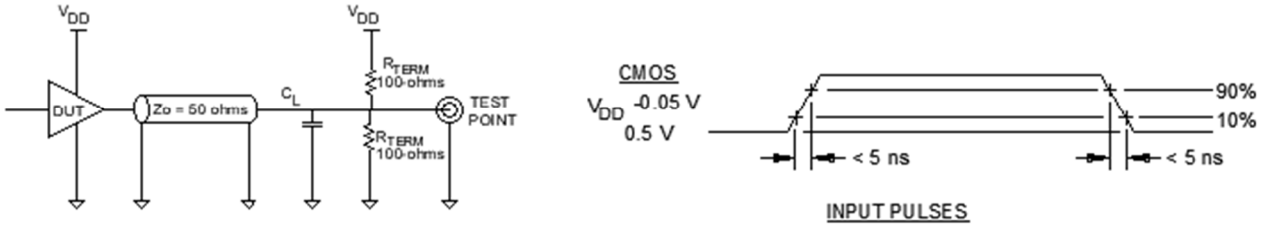
Device types	02 – 04	Device types	02 – 04
Case outlines	Y	Case outlines	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DQ0(0)	35	DQ7(3)
2	DQ1(0)	36	DQ6(3)
3	DQ2(0)	37	DQ5(3)
4	DQ3(0)	38	DQ4(3)
5	DQ4(0)	39	DQ3(3)
6	DQ5(0)	40	DQ2(3)
7	DQ6(0)	41	DQ1(3)
8	DQ7(0)	42	DQ0(3)
9	V_{SS}	43	V_{SS}
10	DQ0(1)	44	DQ7(2)
11	DQ1(1)	45	DQ6(2)
12	DQ2(1)	46	DQ5(2)
13	DQ3(1)	47	DQ4(2)
14	DQ4(1)	48	DQ3(2)
15	DQ5(1)	49	DQ2(2)
16	DQ6(1)	50	DQ1(2)
17	DQ7(1)	51	DQ0(2)
18	V_{DD}	52	V_{DD}
19	A11	53	A10
20	A12	54	A9
21	A13	55	A8
22	A14	56	A7
23	A15	57	A6
24	A16	58	$\overline{W0}$
25	$\overline{E0}$	59	$\overline{E3}$
26	$\overline{G}$	60	V_{SS}
27	$\overline{E1}$	61	$\overline{E2}$
28	A17	62	A5
29	$\overline{W1}$	63	A4
30	$\overline{W2}$	64	A3
31	$\overline{W3}$	65	A2
32	A18	66	A1
33	NC	67	A0
34	NC	68	NC

FIGURE 2. Terminal connections – Continued.

$\overline{G}$	$\overline{Wn}$	$\overline{En}$	I/O Mode	Mode
X 1/	X	1	3-state	Standby
X	0	0	Data-in	Write
1	1	0	3-state	Read 2/
0	1	0	Data out	Read

1/ X is defined as a “don’t care” condition.
2/ Device active; outputs disabled.

FIGURE 3. Truth table.



Notes:
1. 50 pF includes scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

FIGURE 4. Output load circuit and input waveforms.

High-Z to active level and active to High-Z level waveform.

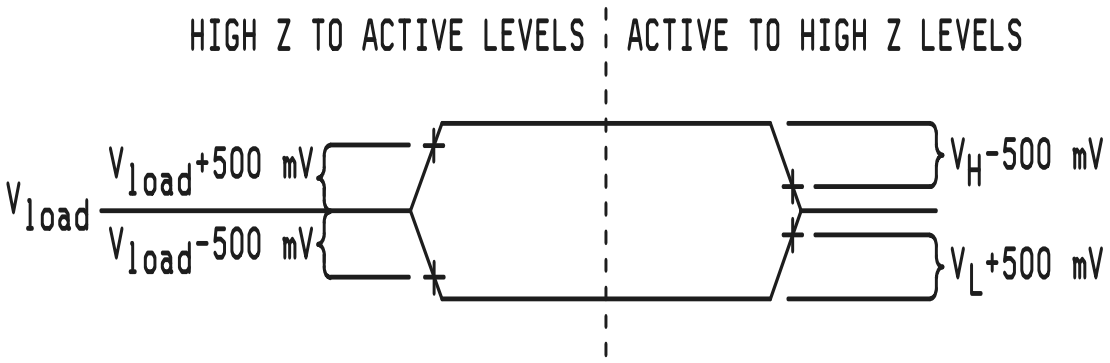
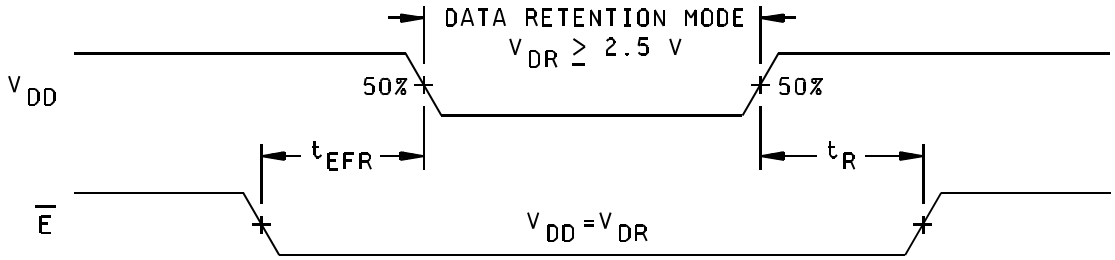


FIGURE 5. Timing waveforms.

Low V_{DD} data retention waveform. (Device 01)



Data retention characteristics (pre/post-irradiation)
(1 second data retention test)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention	2.5	---	V
I_{DDR} 1/ 2/	Data retention current (per byte) 3/	---	5.0	mA
t_{EFR} 1/ 4/	Chip deselect to data retention time	0		ns
t_R 1/ 4/	Operation recovery time	t_{AVAV}		ns

1/ $\overline{En}$ = V_{SS}, all other inputs = V_{DR} or V_{SS}.
2/ Data retention current (I_{DDR}) T_C = 25°C.
3/ This part is capable of being used in a X 8, X 16, X 24, or X 32 configuration. When used in a X 8-bit configuration, the supply current is as stated; if used in a X 16-bit configuration, the listed supply current is doubled etc.
4/ Not guaranteed or tested.

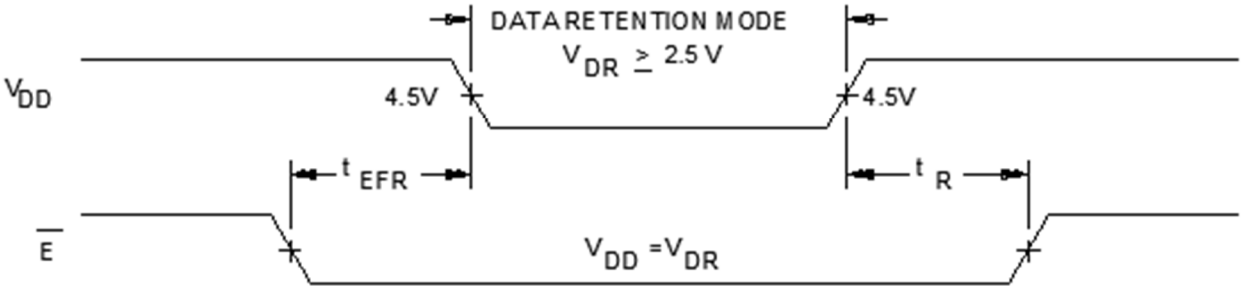
Data retention characteristics (pre/post-irradiation)
(10 second data retention test)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DR} 1/ 4/	V_{DD} for data retention	4.5	5.5	V
t_{EFR} 2/ 3/	Chip deselect to data retention time	0		ns
t_R 2/ 3/	Operation recovery time	t_{AVAV}		ns

1/ Performed at V_{DD} (min) and V_{DD} (max).
2/ $\overline{En}$ = V_{SS}, all other inputs = V_{DR} or V_{SS}.
3/ Not guaranteed or tested.
4/ V_{DD} for data retention (V_{DR}) T_C = -40°C and +125°C.

FIGURE 5. Timing waveforms – Continued.

Low V_{DD} data retention waveform. (Devices 02 – 04)



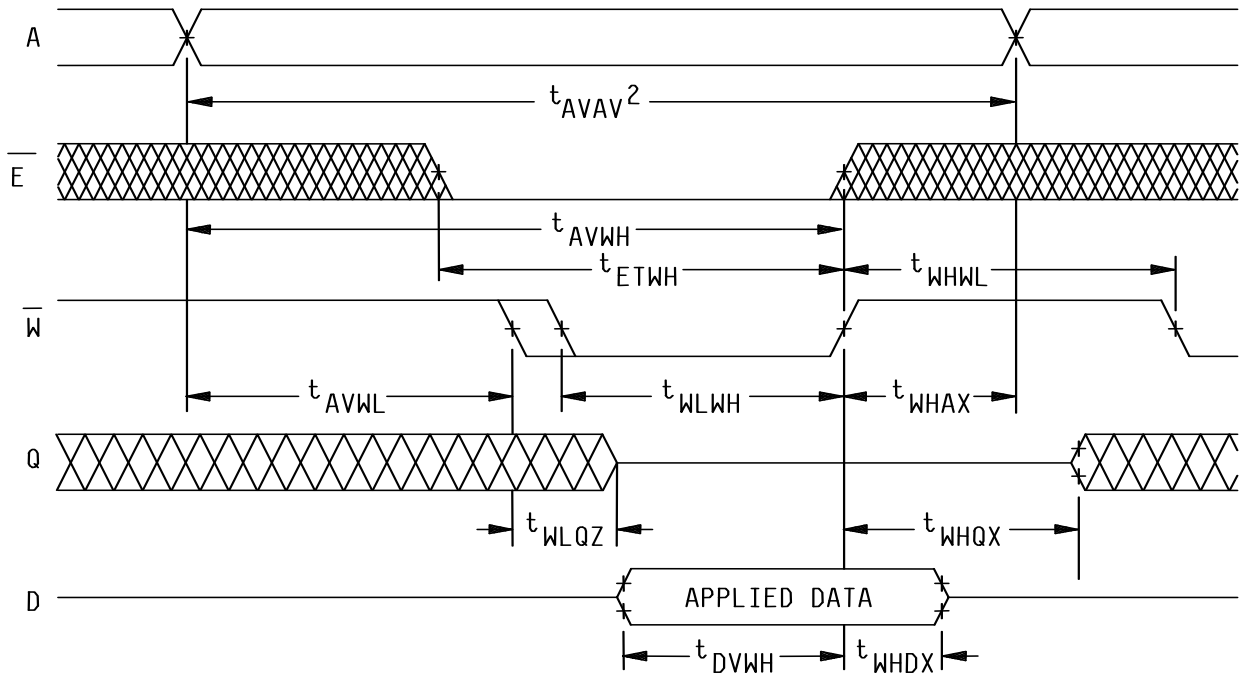
Data retention characteristics (pre/post-irradiation)
(1 second data retention test)

Symbol	Parameter		Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention		2.5	---	V
I_{DDR} 1/	Data retention current (per byte) 2/	-40°C, +25°C	---	16	mA
		+105°C	---	24	mA
t_{EFR} 1/ 3/	Chip deselect to data retention time		0		ns
t_R 1/ 3/	Operation recovery time		t_{AVAV}		ns

1/ $\overline{En}$ = V_{DR}, all other inputs = V_{DR} or V_{SS}.
2/ This part is capable of being used in a X 8, X 16, X 24, or X32 configuration. When used in a X 8-bit configuration, the supply current is as stated; if used in a X 16-bit configuration, the listed supply current is doubled etc.
3/ Not guaranteed or tested.

FIGURE 5. Timing waveforms – Continued.

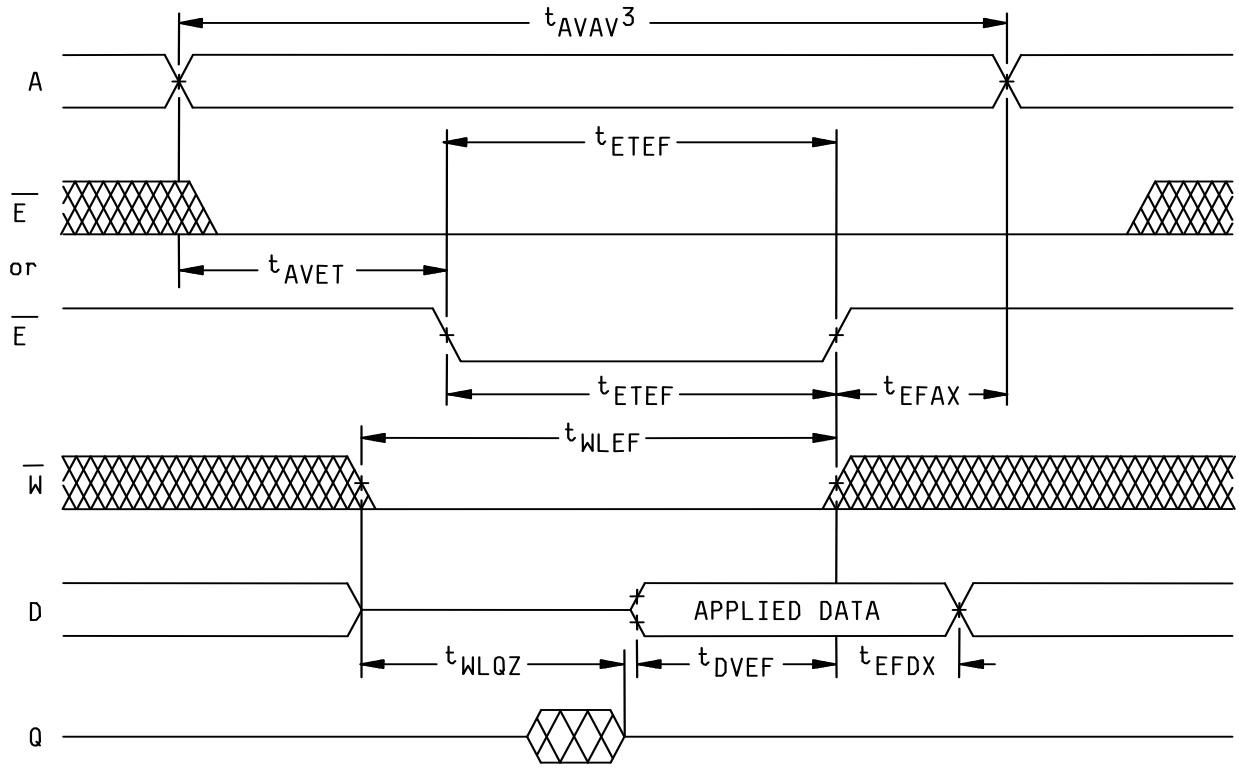
Write cycle 1: write enable-controlled access.



Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.
2. $\overline{G}$ high for t_{AVAV} cycle.

FIGURE 5. Timing waveforms – Continued.

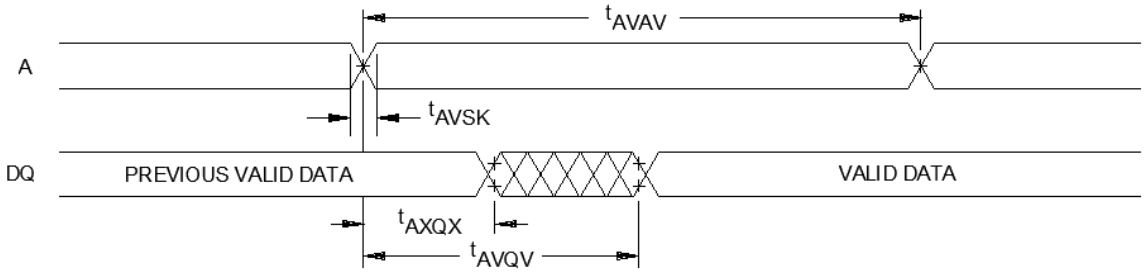
Write cycle 2: chip enable-controlled access.



Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.
2. Either $\overline{E}$ scenario can occur.
3. $\overline{G}$ high for t_{AVAV} cycle.

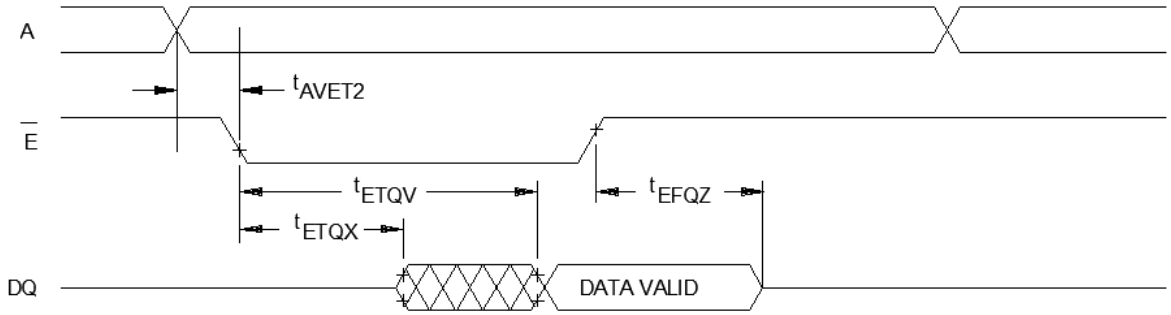
FIGURE 5. Timing waveforms – Continued.

SRAM read cycle 1: address access.



Note: $\overline{E}$ and $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

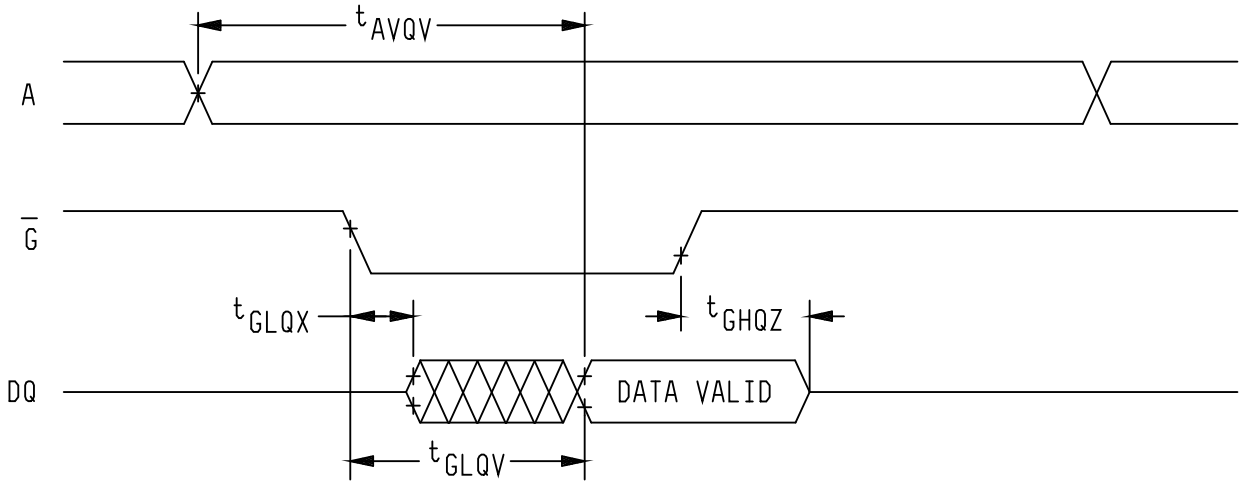
SRAM read cycle 2: chip enable-controlled access.



Note: $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 5. Timing waveforms – Continued.

SRAM read cycle 3: output enable-controlled access.



Note: $\overline{E} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 5. Timing waveforms – Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class Q	Device class V	Device class T
1	Interim electrical parameters (see 4.2)	- - -	1, 7, 9	As specified in QM plan
2	Static burn-in I and II (method 1015)	Not required	Required	
3	Same as line 1	- -	1*, 7* D	
4	Dynamic burn-in (method 1015)	Required	Required	
5	Same as line 1	- - -	1*, 7* D	
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1,2,3,4**,7, 8A, 8B, 9, 10, 11	
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	
10	Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limits shall be required where specified, and the delta values (see table IIB) shall be computed with reference to previous interim electrical parameters (see Line 1).
7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{DD2}	±10% or 35 µA, whichever is greater 2/

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ If device is tested at or below 35 µA, no deltas are required.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

d. Additional screening for device type 03.

(1) 100% internal visual, method 2010, condition A of MIL-STD-883.

(2) 100% PIND (Single Pass).

(3) Serialization.

(4) 100% X-Ray (top view only).

(5) Group A electrical test; -40ºC, 25ºC, 105ºC

(6) Dynamic burn-in, method 1015 condition D of MIL-STD-883, Qidd delta limits, PDA (3%) for Functional Test only, and PDA (5%) for DC, Functional Test, delta limits combined.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q, T, and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.6 herein).

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class T, Q, and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V and T devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm$10°C.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Number of upsets (SEU).

c. Occurrence of latch-up (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-01511

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

FUNCTIONAL ALGORITHMS – Continued.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-07-09

Approved sources of supply for SMD 5962-01511 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L0151101TXC	3/	UT9Q512 K32-SCC
5962L0151101TXA	3/	UT9Q512 K32-SCA
5962L0151101QXC	3/	UT9Q512 K32-SCC
5962L0151101QXA	3/	UT9Q512 K32-SCA
5962L0151102QYC	3/	UT9Q512K32E-SWC
5962L0151102VYC	3/	UT9Q512K32E-SWC
5962L0151103QYC	3/	UT9Q512K32E-SWC
5962R0151104QYC	65342	UT9Q512E-YWC
5962R0151104VYC	65342	UT9Q512E-VWC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486