REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y and footnotes to section 1.2.4. Add missing limits for timing requirements for serial port parameters section in table I. – TVN	02-01-24	Thomas M. Hess
B	Add device type 02. - LTG	02-04-03	Thomas M. Hess
C	Technical changes on sheet 8 for the following tests: Pulse duration, EXTCLK low x1 mode, change from 5.5 ns min to 6.0 ns min. Pulse duration, EXTCLK high x1 mode change from 5.5 ns min to 5.0 ns min. Correct ANSI information in paragraph 2.2 and remove paragraph 3.2.5 Radiation exposure circuit, on sheet 4. - LTG	02-10-24	Thomas M. Hess
D	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-11-19	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-09-11	Thomas M. Hess
F	Update boilerplate to MIL-PRF-38535 requirements. - DRH	24-05-08	Muhammad A. Akbar

REV	F	F	F	F	F	F	F	F	F	F										
SHEET	35	36	37	38	39	40	41	42	43	44										
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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CHECKED BY
Thanh V. Nguyen

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Thomas M. Hess

DRAWING APPROVAL DATE
01-11-16

REVISION LEVEL
F

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-00539**

SHEET 1 OF 44

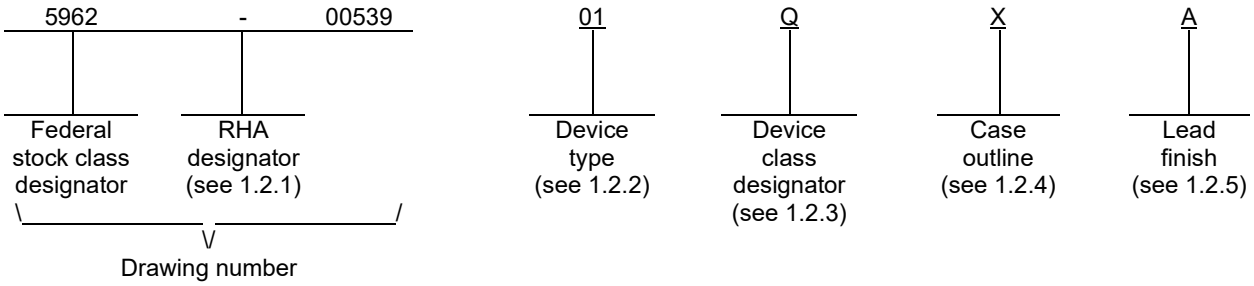
DSCC FORM 2233
APR 97

5962-E347-24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320VC33	Digital signal processor
02	320VC33	Digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X 1/	See figure 1	164	Ceramic quad flat package
Y 2/	See figure 1	164	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Case outline X is not available from an approved of supply.
2/ Case outline Y was originally designated as X. However, the manufacturer has requested that the marking be changed to a Y for standardization purposes.

1.3 Absolute maximum ratings. 3/

Supply voltage range (DV_{DD})	-0.3 V to +4.0 V 4/
Supply voltage range (CV_{DD})	-0.3 V to +2.4 V 4/
Input voltage range (V_{IN})	-1.0 V to +4.6 V 5/
Output voltage range (V_{OUT})	-0.3 V to +4.6 V
Continuous power dissipation (P_D)	500 mW 6/
Storage temperature range (T_{STG})	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	250°C
Thermal resistance, junction-to-case (θ_{JC})	1.82°C/W
Junction temperature (T_J)	125°C

1.4 Recommended operating conditions. 4/ 7/ 8/

Supply voltage range for the core CPU (CV_{DD})	+1.71 V to +1.89 V 9/
Supply voltage range for the I/O pins (DV_{DD})	+3.14 V to +3.46 V 10/
Supply ground (V_{SS})	0.0 V
High level input voltage (V_{IH})	0.7 x DV_{DD} to DV_{DD} + 0.3 V 5/
Low level input voltage (V_{IL})	-0.3 V to 0.3 x DV_{DD} 5/
High level output current (I_{OH})	4.0 mA maximum
Low level output current (I_{OL})	4.0 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C
Capacitive load per output pin (C_L)	30 pF maximum

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ All voltage values are with respect to V_{SS}.
5/ Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of < 2 ns, < 10 mA, and < 1 V amplitude is permissable.
6/ Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the device, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{DD}) current specification in table I herein.
7/ All inputs and I/O pins are configured as inputs.
8/ All inputs and I/O pins use a Schmidt hysteresis inputs except $\overline{SHZ}$ and D0 – D31. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 x DV_{DD}.
9/ CV_{DD} should not exceed DV_{DD} by more than 0.7 V. (Use a Schottky clamp diode between these supplies.)
10/ DV_{DD} should not exceed CV_{DD} by more than 2.5 V.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	DV_{DD} = 3.14 V, I_{OH} = 4.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	DV_{DD} = 3.14 V, I_{OL} = 4.0 mA	1, 2, 3	All		0.4	V
High impedance current	I_Z	T_C = 25°C, DV_{DD} = 3.46 V	1	All	-5.0	+5.0	µA
Input current	I_I	T_C = 25°C, V_I = V_{SS} to DV_{DD}	1	All	-5.0	+5.0	µA
Input current (with internal pullup)	I_{IPU}	Inputs with internal pullups 2/	1, 2, 3	All	-600	10	µA
Input current (with internal pulldown)	I_{IPD}	Inputs with internal pulldowns 2/	1, 2, 3	All	600	-10	µA
Input current (with bus keeper) pullup 3/	I_{BKU}	Bus keeper opposes until conditions match	1, 2, 3	All	-600	10	µA
Input current (with bus keeper) pulldown 3/	I_{BKD}		1, 2, 3	All	600	-10	µA
Supply current, pins 4/ 5/	I_{DDD}	DV_{DD} = 3.46 V, f_X = 75 MHz T_C = 25°C	1	01		260	mA
		DV_{DD} = 3.46 V, f_X = 60 MHz T_C = 25°C		02		260	
Supply current, core CPU 4/ 5/	I_{DDC}	CV_{DD} = 1.89 V, f_X = 75 MHz T_C = 25°C	1	01		215	mA
		CV_{DD} = 1.89 V, f_X = 60 MHz T_C = 25°C		02		215	
Input capacitance	C_{IN}	All inputs except XIN See 4.4.1c	4	All		10	pF
		XIN input See 4.4.1c				10	
Output capacitance	C_{OUT}	See 4.4.1c	4	All		10	pF
Functional test		See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Phase-locked loop characteristics using EXTCLK or on-chip crystal oscillator 6/							
Frequency range, PLL input 7/	F_{pllin}		9, 10, 11	All	5	15	MHz
Frequency range, PLL output 7/	F_{pllout}		9, 10, 11	01	25	75	MHz
				02	25	60	
PLL current, CV_{DD} supply 7/	I_{pll}		1, 2, 3	All		2	mA
PLL power, CV_{DD} supply 7/	P_{pll}		1, 2, 3	All		5	mW
PLL output duty cycle at H1 7/	PLL_{dc}		9, 10, 11	All	45	55	%
PLL output jitter, F_{pllout} = 25 MHz 7/	PLLJ		9, 10, 11	All		400	ps
PLL lock time in input cycles	PLL_{LOCK}		9, 10, 11	All		1000	cycles
Circuit parameters for on-chip crystal oscillator 8/							
Fundamental mode frequency range	F_O	See figure 4.	9, 10, 11	All	1	20	MHz
DC bias point (input threshold)	V_{bias}		1, 2, 3	All	40	60	$\%V_O$
Feedback resistance	R_{fbk}		1, 2, 3	All	100	500	kΩ
Small signal ac output impedance	R_{out}		1, 2, 3	All	250	1000	Ω
$V_{xin} = V_{xinh}$, $I_{xout} = 0$, $F_O = 0$ (logic input)	V_{xoutl}		1, 2, 3	All	V_{SS} -0.1	V_{SS} +0.3	V
$V_{xin} = V_{xinl}$, $I_{xout} = 0$, $F_O = 0$ (logic input)	V_{xouth}		1, 2, 3	All	CV_{DD} -0.3	CV_{DD} +0.1	V
When used for logic level input, oscillator enabled 7/	V_{inl}		1, 2, 3	All	-0.3	$0.2V_O$	V
When used for logic level input, oscillator enabled 7/	V_{inh}		1, 2, 3	All	$0.8V_O$	DV_{DD} +0.3	V
When used for logic level input, oscillator disabled	V_{xinh}		1, 2, 3	All	0.7 DV_{DD}	DV_{DD} +0.3	V
XOUT internal load capacitance 7/	C_{xout}		4	All	2	5	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Circuit parameters for on-chip crystal oscillator - Continued 8/								
XIN internal load capacitance 7/	C_{xin}	See figure 4.		4	All	2	5	pF
Delay time, XIN to H1, x1 and x0.5 modes	$t_{d(XIN-H1)}$			9, 10, 11	All	2	8	ns
Input current, feedback enabled, $V_{il} = 0$ 7/	I_{inl}			1, 2, 3	All		50	µA
Input current, feedback enabled, $V_{il} = V_{ih}$ 7/	I_{inh}			1, 2, 3	All		-50	µA
Timing requirements for EXTCLK, all modes								
Rise time, EXTCLK 7/	$t_{r(EXTCLK)}$	See figure 4.	$F = F_{max}$, x0.5 and x1 modes	9, 10, 11	All		1	ns
			$F < F_{max}$				4	
Fall time, EXTCLK 7/	$t_{f(EXTCLK)}$		$F = F_{max}$, x0.5 and x1 modes	9, 10, 11	All		1	ns
			$F < F_{max}$				4	
Pulse duration, EXTCLK low 7/	$t_{w(EXTCLKL)}$		x5 mode	9, 10, 11	All	21		ns
			x1 mode			6.0		
			x0.5 mode			4		
Pulse duration, EXTCLK high 7/	$t_{w(EXTCLKH)}$		x5 mode	9, 10, 11	All	21		ns
			x1 mode			5.0		
			x0.5 mode			4		
Duty cycle, EXTCLK $[t_{w(EXTCLKH)}/t_{c(H)}]$	$t_{dc(EXTCLK)}$		x5 PLL mode 7/	9, 10, 11	All	40	60	%
			x1 and x0.5 modes, $F = F_{max}$			45	55	
			x1 and x0.5 7/ modes, F = 0 Hz			0	100	
Cycle time, EXTCLK	$t_{c(EXTCLK)}$		x5 mode 7/	9, 10, 11	All	66.7	200	ns
			x1 mode		01	13.3		
					02	16.7		
			x0.5 mode 7/		All	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Timing requirements for EXTCLK, all modes – Continued								
Frequency range, $1/t_{c(EXTCLK)}$	F_{ext}	See figure 4.	x5 mode 7/	9, 10, 11	All	5	15	MHz
			x1 mode		01	0	75	
					02	0	60	
			x0.5 mode 7/		All	0	100	
Switching characteristics for EXTCLK over recommended operating conditions, all modes								
Delay time, EXTCLK to H1 and H3 7/	$t_{d(EXTCLK-H)}$	See figure 4.	x1 mode	9, 10, 11	All	2	7	ns
			x0.5 mode			2	7	
Rise time, H1 and H3 7/	$t_{r(H)}$			9, 10, 11	All		3	ns
Fall time, H1 and H3 7/	$t_{f(H)}$			9, 10, 11	All		3	ns
Delay time, from H1 low to H3 high or from H3 low to H1 high 7/	$t_{d(HL-HH)}$			9, 10, 11	All	-1.5	2	ns
Timing requirements for memory read/write 9/								
Setup time, data before H1 low (read) 7/	$t_{su(D-H1L)R}$	See figure 4.		9, 10, 11	All	5		ns
Hold time, data after H1 low (read) 7/	$t_{h(H1L-D)R}$			9, 10, 11	All	-1		ns
Setup time, $\overline{RDY}$ before H1 high	$t_{su(RDY-H1H)}$			9, 10, 11	All	5		ns
Hold time, $\overline{RDY}$ after H1 high 7/	$t_{h(H1H-RDY)}$			9, 10, 11	All	-1		ns
Delay time, address valid to $\overline{RDY}$ 7/	$t_{d(A-RDY)}$			9, 10, 11	All		P-6 10/	ns
Valid time, data valid after address $\overline{PAGEx}$, or $\overline{STRB}$ valid 7/	$t_{v(A-D)}$	See figure 4.	0 wait state, C_L = 30 pF	9, 10, 11	All		6	ns
			1 wait state				$t_{c(H)}$+6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for memory read/write 9/							
Delay time, H1 low to $\overline{STRB}$ low	$t_{d(H1L-SL)}$	See figure 4.	9, 10, 11	All	-1 7/	3	ns
Delay time, H1 low to $\overline{STRB}$ high	$t_{d(H1L-SH)}$		9, 10, 11	All	-1 7/	3	ns
Delay time, H1 high to R/$\overline{W}$ low (write)	$t_{d(H1H-RWL)W}$		9, 10, 11	All	-1 7/	3	ns
Delay time, H1 low to address valid	$t_{d(H1L-A)}$		9, 10, 11	All	-1 7/	3	ns
Delay time, H1 high to R/$\overline{W}$ high (write)	$t_{d(H1H-RWH)W}$		9, 10, 11	All	-1 7/	3	ns
Delay time, H1 high to address valid on back-to-back write cycles (write)	$t_{d(H1H-A)W}$		9, 10, 11	All	-1 7/	3	ns
Valid time, data after H1 low (write)	$t_{v(H1L-D)W}$		9, 10, 11	All		5	ns
Hold time, data after H1 high (write)	$t_{h(H1H-D)W}$		9, 10, 11	All	0 7/	5	ns
Timing requirements for XF0 and XF1 when executing LDFI or LDII							
Setup time, XF1 before H1 low 7/	$t_{su(XF1-H1L)}$	See figure 4.	9, 10, 11	All	4		ns
Hold time, XF1 after H1 low 7/	$t_{h(H1L-XF1)}$		9, 10, 11	All	0		ns
Switching characteristics over recommended operating conditions for XF0 and XF1 when excecuting LDFI or LDII							
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4.	9, 10, 11	All		3	ns
Switching characteristics over recommended operating conditions for XF0 when excecuting STFI or STII							
Delay time, H3 high to XF0 high 11/	$t_{d(H3H-XF0H)}$	See figure 4.	9, 10, 11	All		3	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing requirements for XF0 and XF1 when executing SIGI							
Setup time, XF1 before H1 low 7/	$t_{su(XF1-H1L)}$	See figure 4.	9, 10, 11	All	4		ns
Hold time, XF1 after H1 low 7/	$t_{h(H1L-XF1)}$		9, 10, 11	All	0		ns
Switching characteristics over recommended operating conditions for XF0 and XF1 when excecuting SIGI							
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4.	9, 10, 11	All		3	ns
Delay time, H3 high to XF0 high	$t_{d(H3H-XF0H)}$		9, 10, 11	All		3	ns
Switching characteristics over recommended operating conditions for loading the XF register when configured as an output pin							
Valid time, XFx after H3 high	$t_{v(H3H-XF)}$	See figure 4.	9, 10, 11	All		3	ns
Timing requirements for changing XFx from output to input mode							
Setup time, XFx before H1 low	$t_{su(XF-H1L)}$	See figure 4.	9, 10, 11	All	4		ns
Hold time, XFx after H1 low	$t_{h(H1L-XF)}$		9, 10, 11	All	0		ns
Switching characteristics over recommended operating conditions for changing XFx from output to input mode							
Disable time, XFx after H3 high 7/	$t_{dis(H3H-XF)}$	See figure 4.	9, 10, 11	All		5	ns
Switching characteristics over recommended operating conditions for changing XFx from input to output mode							
Delay time, H3 high to XFx switching from input to output	$t_{d(H3H-XF)}$	See figure 4.	9, 10, 11	All		3	ns
Timing requirements for $\overline{\text{RESET}}$							
Setup time, $\overline{\text{RESET}}$ before EXTCLK low 7/	$t_{su(RESET-EXTCLKL)}$	See figure 4.	9, 10, 11	All	5	P-7 12/	ns
Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	$t_{su(RESETH-H1L)}$		9, 10, 11	All	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for $\overline{RESET}$							
Delay time, EXTCLK high to H1 high 7/	$t_{d(EXTCLKH-H1H)}$	See figure 4.	9, 10, 11	All	2	7	ns
Delay time, EXTCLK high to H1 low 7/	$t_{d(EXTCLKH-H1L)}$		9, 10, 11	All	2	7	ns
Delay time, EXTCLK high to H3 low 7/	$t_{d(EXTCLKH-H3L)}$		9, 10, 11	All	2	7	ns
Delay time, EXTCLK high to H3 high 7/	$t_{d(EXTCLKH-H3H)}$		9, 10, 11	All	2	7	ns
Disable time, data (high impedance) from H1 high 7/ 13/	$t_{dis(H1H-DZ)}$		9, 10, 11	All		6	ns
Disable time, address (high impedance) from H3 high 7/	$t_{dis(H3H-AZ)}$		9, 10, 11	All		6	ns
Delay time, H3 high to control signals high 7/	$t_{d(H3H-CONTROLH)}$		9, 10, 11	All		3	ns
Delay time, H1 high to R/$\overline{W}$ high 7/	$t_{d(H1H-RWH)}$		9, 10, 11	All		3	ns
Delay time, H1 high to $\overline{IACK}$ high 7/	$t_{d(H1H-IACKH)}$		9, 10, 11	All		3	ns
Disable time, asynchronous reset signals disabled (high impedance) from $\overline{RESET}$ low 7/ 14/	$t_{dis(RESETL-ASYNCH)}$		9, 10, 11	All		6	ns
Timing requirements for $\overline{INT3}$ - $\overline{INT0}$ response							
Setup time, $\overline{INT3}$ - $\overline{INT0}$ before H1 low 7/	$t_{su(INT-H1L)}$	See figure 4.	9, 10, 11	All	4		ns
Hold time, $\overline{INT3}$ - $\overline{INT0}$ after H1 low	$t_{h(H1L-INT)}$		9, 10, 11	All		0	ns
Pulse duration, interrupt to ensure only one interrupt 7/ 15/	$t_{w(INT)}$		9, 10, 11	All	P+5	2P-5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Switching characteristics over recommended operating conditions for $\overline{IACK}$								
Delay time, H1 high to $\overline{IACK}$ low	$t_{d(H1H-IACKL)}$	See figure 4.		9, 10, 11	All	1 7/	3	ns
Delay time, H1 high to $\overline{IACK}$ high	$t_{d(H1H-IACKH)}$	See figure 4.		9, 10, 11	All	1 7/	3	ns
Timimg requirements for serial port parameters								
Cycle time, CLKX/R 7/	$t_{c(SCK)}$	See figure 4.	CLKX/R ext	9, 10, 11	All	$t_{c(H)}$x2.6		ns
			CLKX/R int			$t_{c(H)}$x4 16/	$t_{c(H)}x2^{16}$	
Pulse duration, CLKX/R high/low	$t_{w(SCK)}$	See figure 4.	CLKX/R ext	9, 10, 11	All	$t_{c(H)}$+5		ns
			CLKX/R int 7/			$[t_{c(SCK)}/2]$-4	$[t_{c(SCK)}/2]$+4	
Rise time, CLKX/R 7/	$t_{r(SCK)}$	See figure 4.		9, 10, 11	All		3	ns
Fall time, CLKX/R 7/	$t_{f(SCK)}$	See figure 4.		9, 10, 11	All		3	ns
Setup time, DR before CLKR low 7/	$t_{su(DR-CLKRL)}$	See figure 4.	CLKR ext	9, 10, 11	All	4		ns
			CLKR int			5		
Hold time, DR after CLKR low 7/	$t_{h(CLKRL-DR)}$	See figure 4.	CLKR ext	9, 10, 11	All	3		ns
			CLKR int			0		
Setup time, FSR before CLKR low 7/	$t_{su(FSR-CLKRL)}$	See figure 4.	CLKR ext	9, 10, 11	All	4		ns
			CLKR int			5		
Hold time, FSX/R input after CLKX/R low 7/	$t_{h(SCKL-FS)}$	See figure 4.	CLKX/R ext	9, 10, 11	All	3		ns
			CLKX/R int			0		
Setup time, external FSX before CLKX 7/	$t_{su(FSX-CLKX)}$	See figure 4.	CLKX ext	9, 10, 11	All	$-[t_{c(H)}-6]$	$[t_{c(SCK)}/2]$-6	ns
			CLKX int			$-[t_{c(H)}-10]$	$t_{c(SCK)}/2$	
Switching characteristics over recommended operating conditions for serial port parameters								
Delay time, H1 high to internal CLKX/R 7/	$t_{d(H1H-SCK)}$	See figure 4.		9, 10, 11	All		4	ns
Delay time, CLKX to DX valid	$t_{d(CLKX-DX)}$	See figure 4.	CLKX ext	9, 10, 11	All		6	ns
			CLKX int 7/				5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Switching characteristics over recommended operating conditions for serial port parameters – Continued								
Delay time, CLKX to internal FSX high/low	$t_{d(CLKX-FSX)}$	See figure 4.	CLKX ext	9, 10, 11	All		5	ns
			CLKX int 7/				4	
Delay time, CLKX to first DX bit, FSX precedes CLKX high	$t_{d(CLKX-DX)V}$		CLKX ext	9, 10, 11	All		4	ns
			CLKX int 7/				5	
Delay time, FSX to first DX bit, CLKX precedes FSX	$t_{d(FSX-DX)V}$	See figure 4.		9, 10, 11	All		6	ns
Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CLKX-DXZ)}$			9, 10, 11	All		6	ns
Timing requirements for $\overline{HOLD}$ / $\overline{HOLDA}$								
Setup time, $\overline{HOLD}$ before H1 low	$t_{su)HOLD-H1L)}$	See figure 4.		9, 10, 11	All	3		ns
Pulse duration, $\overline{HOLD}$ low 7/	$t_{w(HOLD)}$			9, 10, 11	All	$3t_{c(H)}$		ns
Switching characteristics over recommended operating conditions for $\overline{HOLD}$ / $\overline{HOLDA}$								
Valid time, $\overline{HOLDA}$ after H1 low 7/	$t_{v(H1L-HOLDA)}$	See figure 4.		9, 10, 11	All	1	3	ns
Pulse duration, $\overline{HOLDA}$ low 7/	$t_{w(HOLDA)}$			9, 10, 11	All	$2t_{c(H)}$-4		ns
Delay time, H1 low to $\overline{STRB}$ high for a $\overline{HOLD}$	$t_{d(H1L-SH)H}$			9, 10, 11	All	-1	3	ns
Disable time, $\overline{STRB}$ to the high-impedance state from H1 low	$t_{dis(H1L-S)}$			9, 10, 11	All		4	ns
Enable time, $\overline{STRB}$ enabled (active) from H1 low	$t_{en(H1L-S)}$			9, 10, 11	All		4	ns
Disable time, R/ $\overline{W}$ to the high-impedance state from H1 low 7/	$t_{dis(H1L-RW)}$			9, 10, 11	All		5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Switching characteristics over recommended operating conditions for $\overline{HOLD}$ / $\overline{HOLDA}$ - Continued								
Enable time, R/$\overline{W}$ enabled (active) from H1 low	$t_{en(H1L-RW)}$	See figure 4.		9, 10, 11	All		4	ns
Disable time, address to the high-impedance state from H1 low 7/	$t_{dis(H1L-A)}$			9, 10, 11	All		4	ns
Enable time, address enabled (valid) from H1 low	$t_{en(H1L-A)}$			9, 10, 11	All		5	ns
Disable time, data to the high-impedance state from H1 high 7/	$t_{dis(H1H-D)}$			9, 10, 11	All		4	ns
Timing requirements for peripheral pin general-purpose I/O 17/								
Setup time, general-purpose input before H1 low 7/	$t_{su(GPIO-H1L)}$	See figure 4.		9, 10, 11	All	3		ns
Hold time, general-purpose input after H1 low 7/	$t_{h(H1L-GPIO)}$			9, 10, 11	All	0		ns
Switching characteristics over recommended operating conditions for peripheral pin general-purpose I/O 17/								
Delay time, H1 high to general-purpose output	$t_{d(H1H-GPIO)}$	See figure 4.		9, 10, 11	All		4	ns
Disable time, general-purpose output from H1 high	$t_{dis(H1H)}$			9, 10, 11	All		5	ns
Timing requirements for timer pin								
Setup time, TCLK external before H1 low 7/ 18/	$t_{su(TCLK-H1L)}$	See figure 4.		9, 10, 11	All	3		ns
Hold time, TCLK external after H1 low 18/	$t_{h(H1L-TCLK)}$			9, 10, 11	All	0		ns
Switching characteristics over recommended operating conditions for timer pin								
Delay time, H1 high to TCLK internal valid	$t_{d(H1H-TCLK)}$	See figure 4.		9, 10, 11	All		3	ns
Cycle time, TCLK 7/ 19/	$t_{c(TCLK)}$	See figure 4.	TCLK ext	9, 10, 11	All	$t_{c(H)}x2.6$		ns
			TCLK int			$t_{c(H)}x2$	$t_{c(H)}x2^{32}$	
Pulse duration, TCLK 7/ 19/	$t_{w(TCLK)}$		TCLK ext	9, 10, 11	All	$t_{c(H)}+5$		ns
			TCLK int			$[t_{c(TCLK)}/2]-4$	$[t_{c(TCLK)}/2]+4$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.14\ V \le DV_{DD} \le +3.46\ V$ $+1.71\ V \le CV_{DD} \le +1.89\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for $\overline{SHZ}$							
Disable time, $\overline{SHZ}$ low to all outputs, I/O pins disabled (high impedance) 7/	$t_{dis(SHZ)}$	See figure 4.	9, 10, 11	All	0	8	ns

1/ All voltage values are with respect to V_{SS}.

2/ Pins with internal pullup devices: TDI, TCK, and TMS. Pins with internal pulldown devices: $\overline{TRST}$.

3/ Pins D0 – D31 include internal bus keepers that maintain valid logic levels when the bus is not driven.

4/ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible.

5/ f_x is the PLL output clock frequency.

6/ Duty cycle is defined as $100xt_1/(t_1+t_2)\%$.

7/ Not production tested. V_O = Oscillator internal supply voltage.

8/ This circuit is intended for series resonant fundamental mode operation.

9/ These timings assume a similar loading of 30 pF on all pins.

10/ $P = t_{c(H)}/2$ (when duty cycle equals 50%).

11/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

12/ $P = t_{c(EXTCLK)}$.

13/ High impedance for data bus is limited to nominal bus keeper Z_{OUT} = 15 kΩ.

14/ Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

15/ $P = t_{c(H)}$.

16/ A cycle time of $t_{c(H)}x2$ is possible when the device is operated at lower CPU frequencies.

17/ Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.

18/ These requirements are applicable for a synchronous input clock.

19/ These requirements are applicable for an asynchronous input clock.

Case outlines X and Y

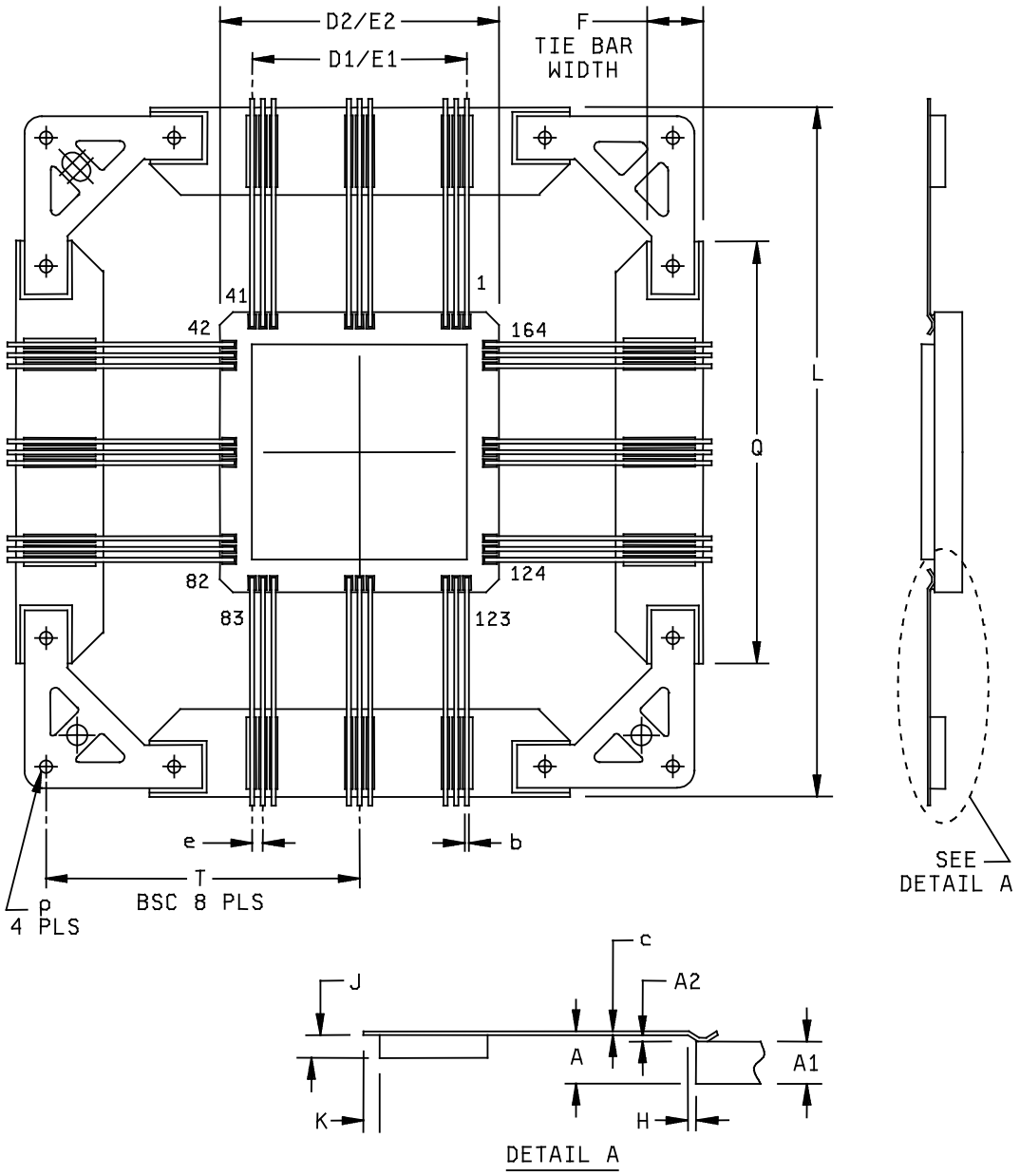


FIGURE 1. Case outlines.

Case outlines X and Y - Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.130		3.30
A1		.105		2.67
A2	.002	.014	0.05	0.36
b	.006	.010	0.15	0.25
c	.004	.009	0.10	0.23
D1	1.000 BSC		25.40 BSC	
D2	1.120	1.140	28.45	28.96
e	.025 BSC		0.64 BSC	
F	.275	.325	6.99	8.26
H		.018		0.46
J	.030	.040	0.76	1.02
K		.020		0.51
L	2.485	2.505	63.12	63.63
P	.059	.061	1.50	1.55
Q	1.480	1.520	37.59	38.61
T	1.150 BSC		29.21 BSC	

FIGURE 1. Case outlines – Continued.

Case outlines	X and Y				
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	NC	29	A3	57	V_{SS}
2	NC	30	A2	58	D31
3	NC	31	CV_{DD}	59	D30
4	A20	32	A1	60	D29
5	V_{SS}	33	A0	61	DV_{DD}
6	A19	34	DV_{DD}	62	D28
7	A18	35	$\overline{PAGE3}$	63	D27
8	A17	36	$\overline{PAGE2}$	64	V_{SS}
9	DV_{DD}	37	V_{SS}	65	D26
10	A16	38	$\overline{PAGE1}$	66	D25
11	A15	39	$\overline{PAGE0}$	67	D24
12	V_{SS}	40	NC	68	DV_{DD}
13	A14	41	NC	69	D23
14	A13	42	NC	70	D22
15	CV_{DD}	43	NC	71	V_{SS}
16	A12	44	NC	72	D21
17	A11	45	DV_{DD}	73	D20
18	DV_{DD}	46	H1	74	CV_{DD}
19	A10	47	H3	75	D19
20	A9	48	V_{SS}	76	D18
21	V_{SS}	49	$\overline{STRB}$	77	DV_{DD}
22	A8	50	R/ $\overline{W}$	78	D17
23	A7	51	DV_{DD}	79	D16
24	A6	52	$\overline{IACK}$	80	V_{SS}
25	A5	53	$\overline{RDY}$	81	NC
26	DV_{DD}	54	CV_{DD}	82	NC
27	A4	55	$\overline{HOLD}$	83	NC
28	V_{SS}	56	$\overline{HOLDA}$	84	NC

FIGURE 2. Terminal connections.

Case outlines	X and Y				
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
85	D15	112	TDI	139	$\overline{INT0}$
86	D14	113	CV_{DD}	140	CV_{DD}
87	D13	114	TMS	141	EDGEMODE
88	D12	115	$\overline{TRST}$	142	MCB/$\overline{MP}$
89	DV_{DD}	116	DR0	143	V_{SS}
90	D11	117	V_{SS}	144	$\overline{RESET}$
91	D10	118	FSR0	145	$\overline{SHZ}$
92	V_{SS}	119	CLKR	146	DV_{DD}
93	D9	120	DV_{DD}	147	EXTCLK
94	D8	121	NC	148	$PLLV_{DD}$
95	CV_{DD}	122	NC	149	XOUT
96	D7	123	NC	150	XIN
97	D6	124	NC	151	$PLLV_{SS}$
98	DV_{DD}	125	NC	152	CLKMD1
99	D5	126	CLKX0	153	CLKMD0
100	D4	127	FSX	154	CV_{DD}
101	V_{SS}	128	DX	155	RSV1
102	D3	129	V_{SS}	156	RSV0
103	D2	130	TCLK1	157	V_{SS}
104	D1	131	TCLK0	158	A23
105	D0	132	DV_{DD}	159	A22
106	DV_{DD}	133	XF1	160	DV_{DD}
107	EMU1	134	XF0	161	A21
108	EMU0	135	V_{SS}	162	NC
109	V_{SS}	136	$\overline{INT3}$	163	NC
110	TCK	137	$\overline{INT2}$	164	NC
111	TDO	138	$\overline{INT1}$		

FIGURE 2. Terminal connections – Continued.

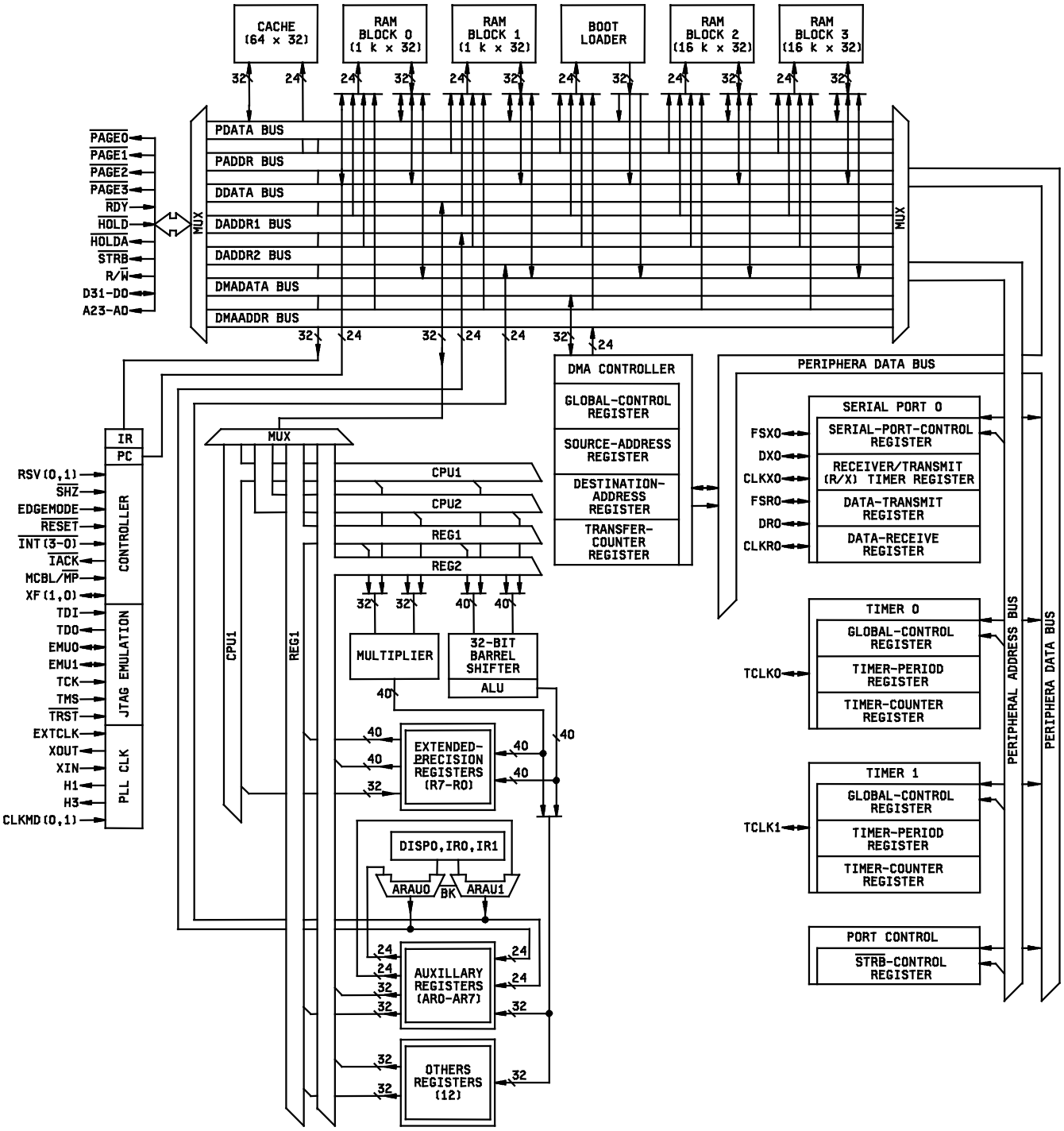
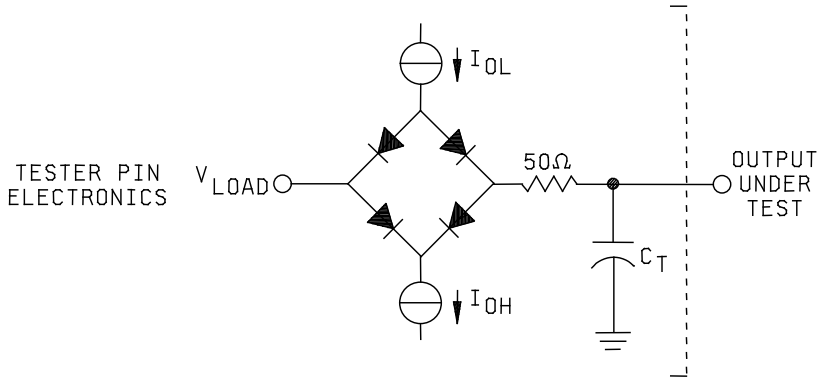
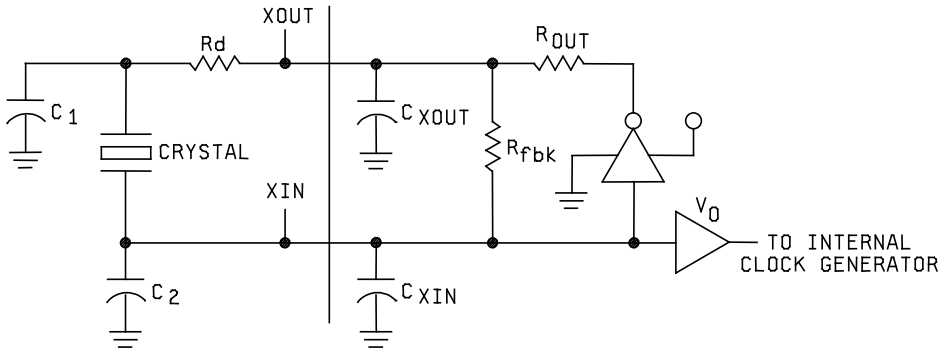


FIGURE 3. Functional block diagram.



TEST CIRCUIT

NOTES: I_{OL} = 4.0 mA (all outputs) for dc levels test.
I_{OL} and I_{OH} are adjusted during ac timing analysis to achieve an ac termination of 50Ω.
$V_{LOAD} = DV_{DD}/2$.
C_T = 40 pF, typical load-circuit capacitance.



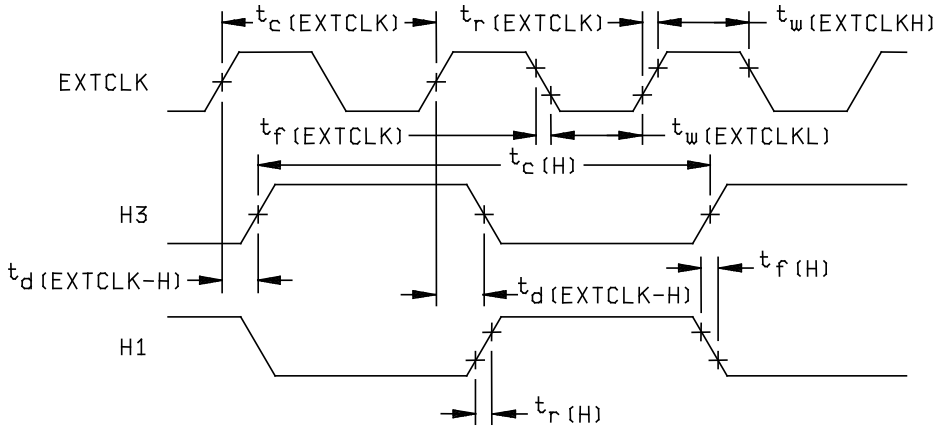
ON-CHIP OSCILLATOR CIRCUIT

Frequency (MHz)	Rd (Ω)	C1 (pF)	C2 (pF)	CL (pF) 1/	RL (Ω) 1/
2	4700	18	18	12	200
5	2200	18	18	12	60
10	470	15	15	12	30
15	0	15	12	12	25
20	0	9	9	10	25

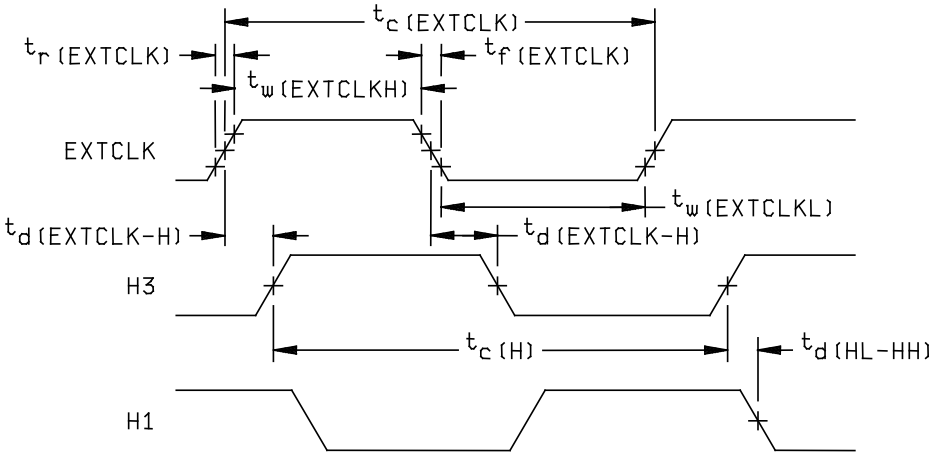
1/ CL and RL are typical internal series load capacitance and resistance of the crystal.

TYPICAL CRYSTAL CIRCUIT LOADING

FIGURE 4. Test circuit and timing waveforms.



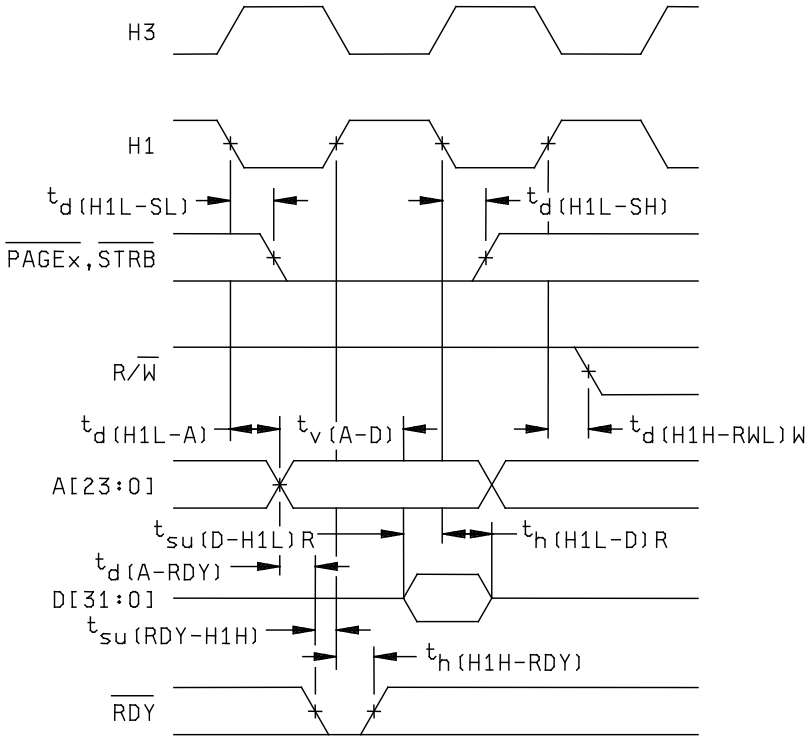
DIVIDE-BY-TWO MODE



DIVIDE-BY-ONE MODE

NOTE: EXTCLK is held low.

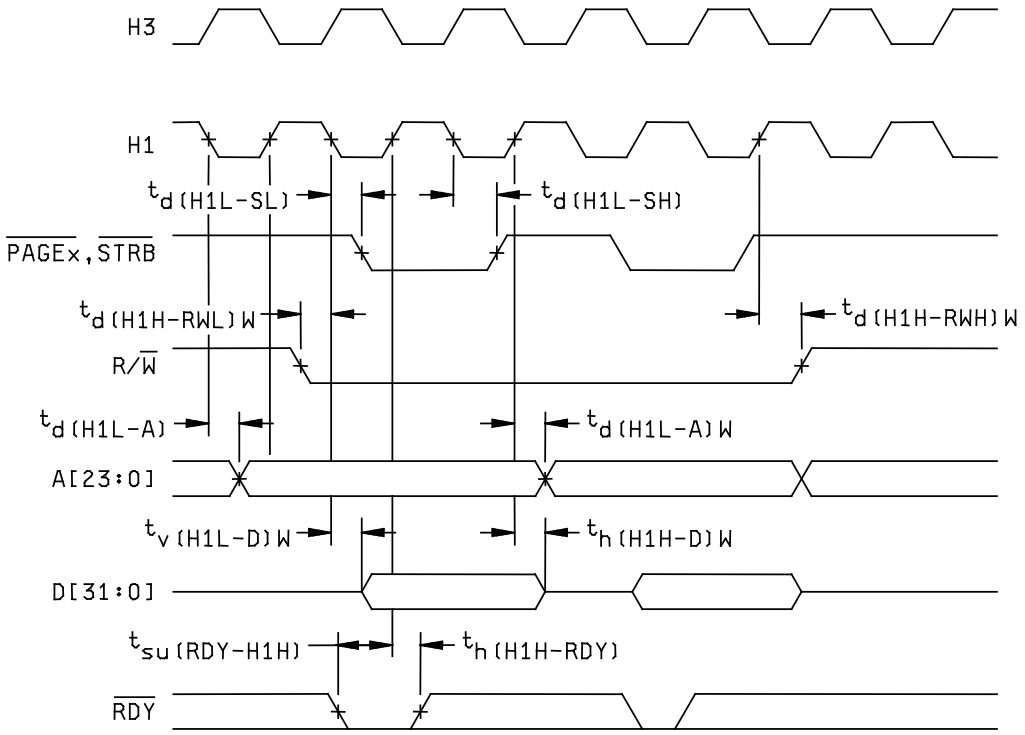
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR MEMORY ($\overline{STRB}$=0 AND $\overline{PAGEx}$=0) READ

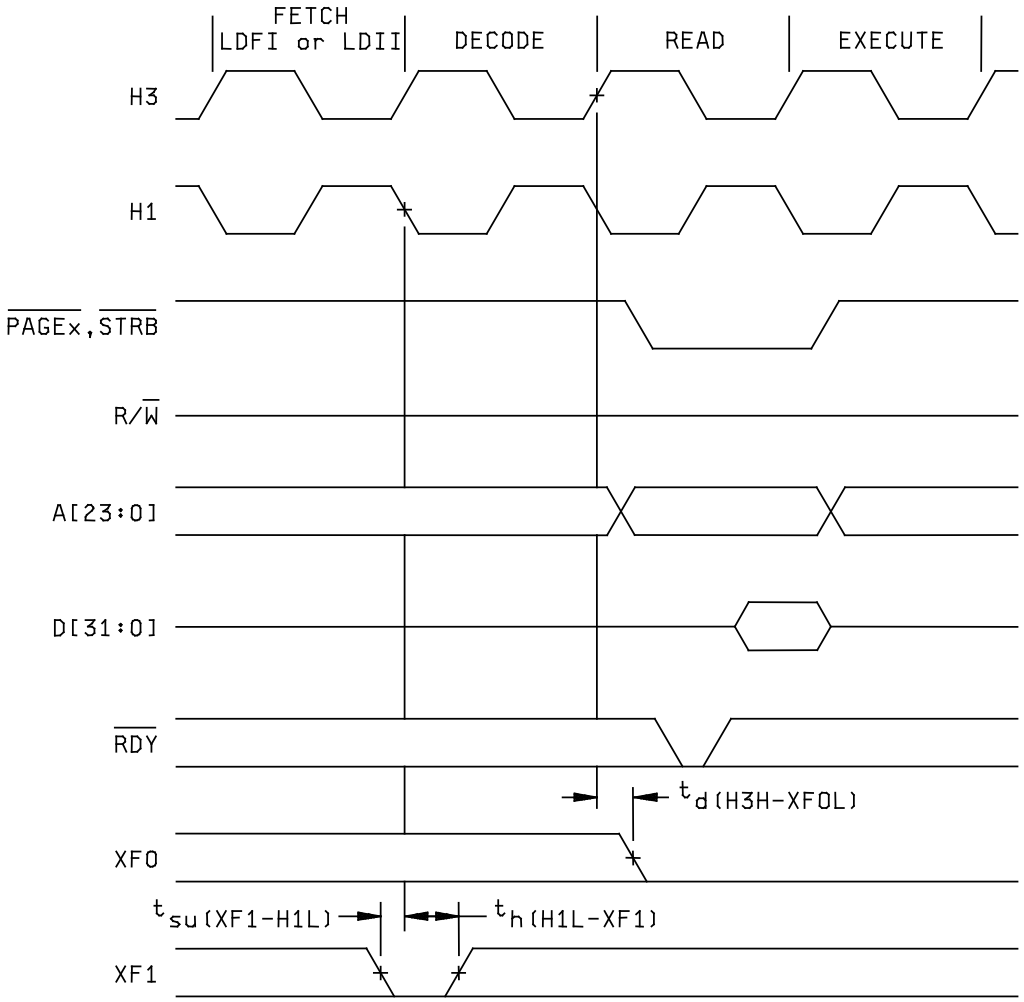
NOTE: $\overline{STRB}$ remains low during back-to-back read operation.

FIGURE 4. Test circuit and timing waveforms - Continued.



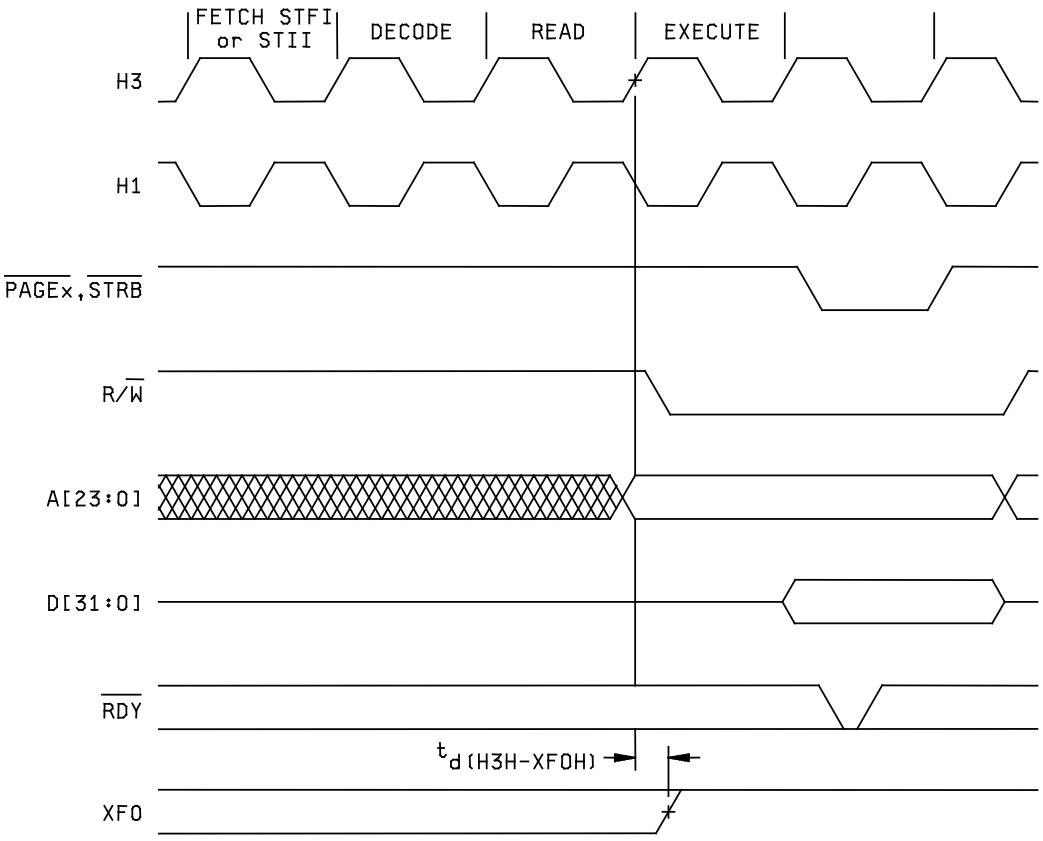
TIMING FOR MEMORY ($\overline{STRB}$=0 AND $\overline{PAGEx}$=0) WRITE

FIGURE 4. Test circuit and timing waveforms - Continued.



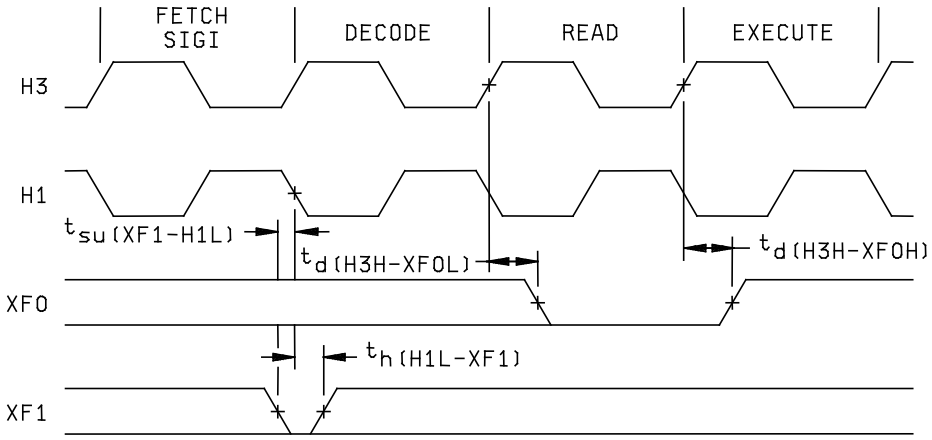
TIMING FOR XFO AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4. Test circuit and timing waveforms - Continued.

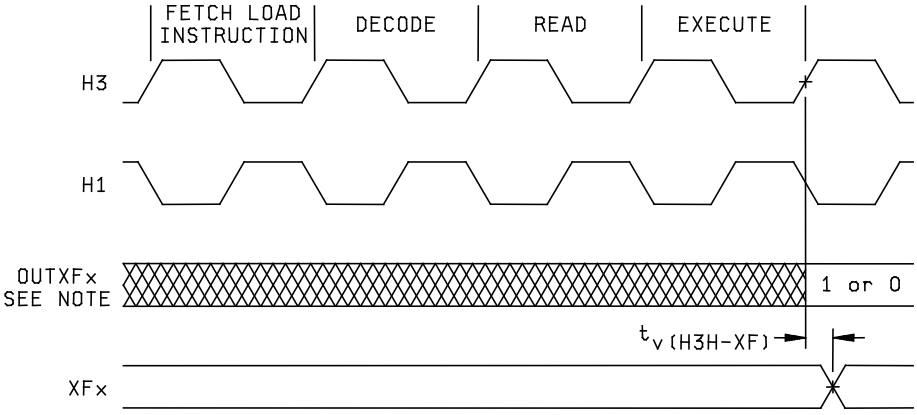


TIMING FOR XFO WHEN EXECUTING AN STFI OR STII

FIGURE 4. Test circuit and timing waveforms - Continued.



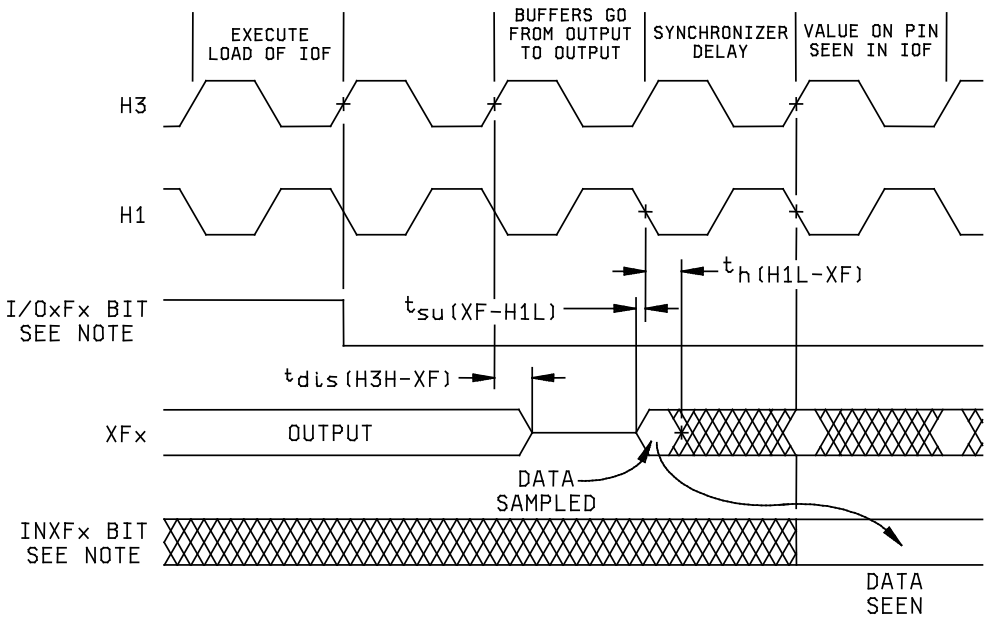
TIMING FOR XFO AND XF1 WHEN EXECUTING SIGI



TIMING FOR LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

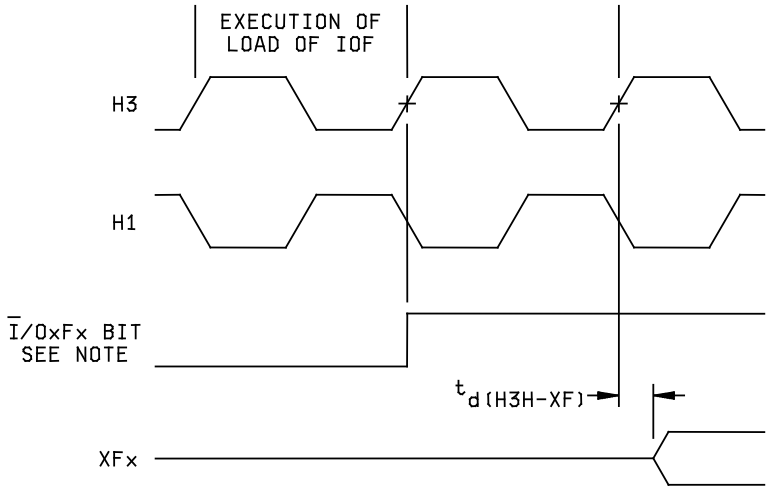
NOTE: OUTXFx represents either bit 2 or 6 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR CHANGING XFx FROM OUTPUT TO INPUT MODE

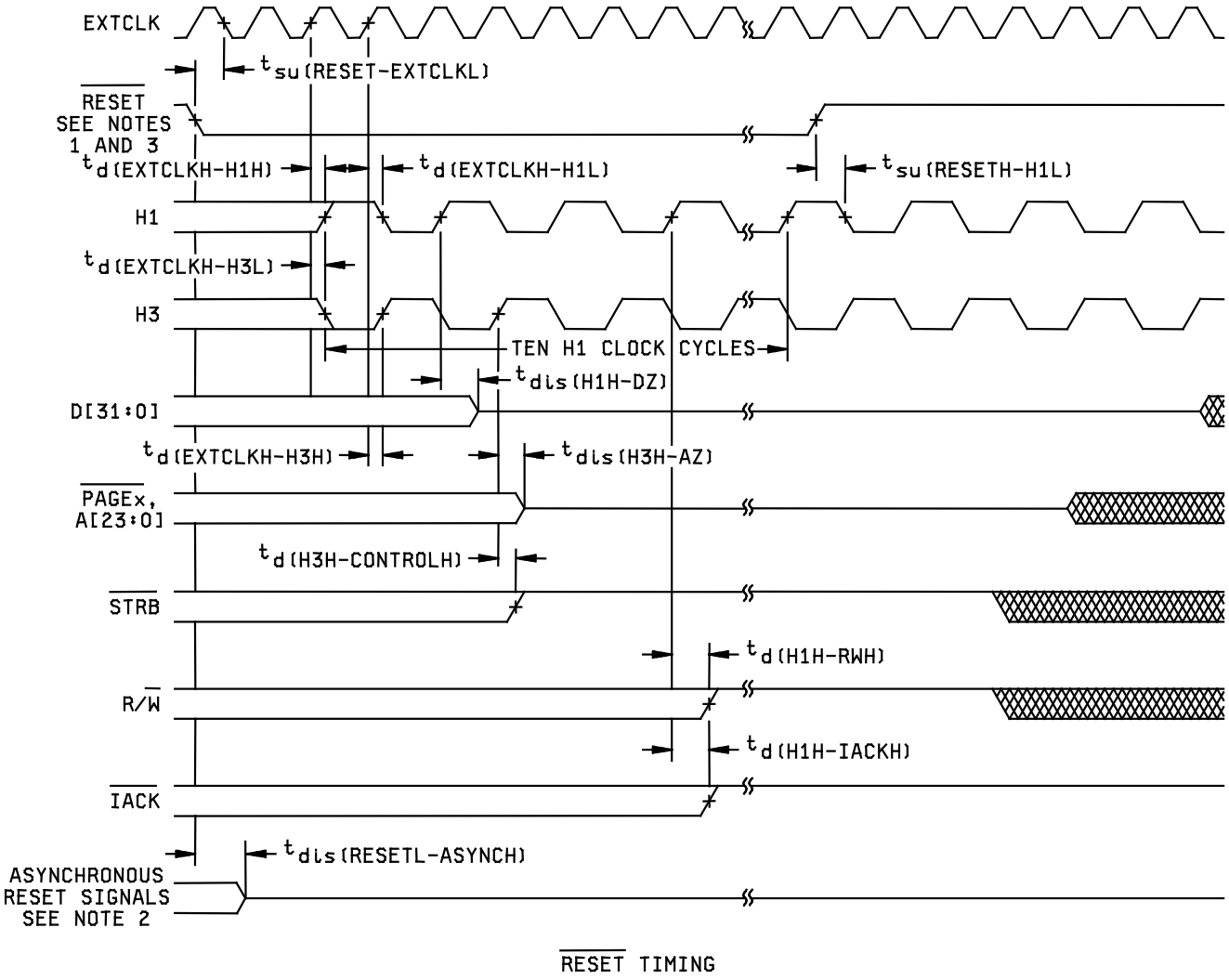
NOTE: $\overline{I}$/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of ther IOF register.



TIMING FOR CHANGING XFx FROM INPUT TO OUTPUT MODE

NOTE: $\overline{I}$/OxFx represents either bit 1 or bit 5 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.

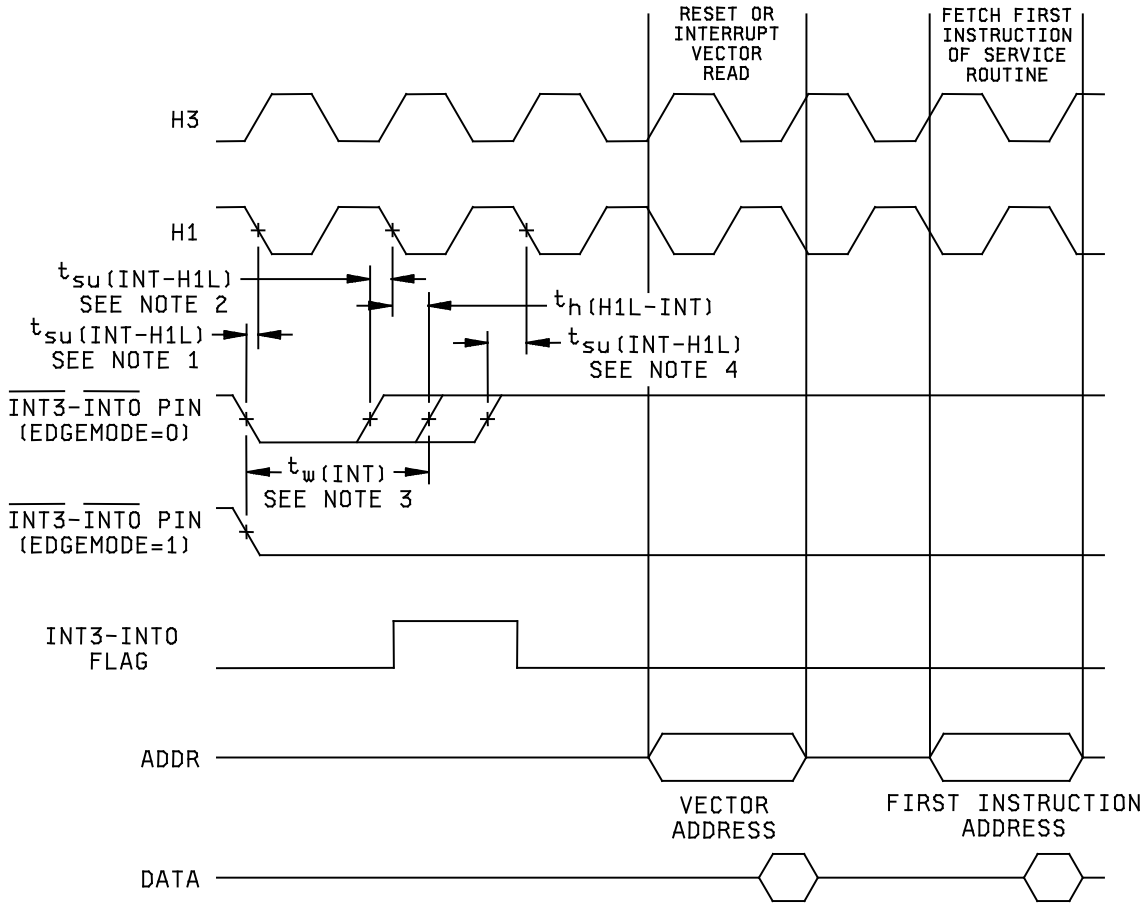


RESET TIMING

NOTES:

1. Clock circuit is configured in 'C31-compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H3.
2. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
3. RESET is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
4. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
5. The address and PAGE3 - PAGE0 outputs are placed in a high-impedance state during reset requiring a nominal 10-22 kΩ pullup. If not, undesirable spurious reads can occur when these outputs are not driven.

FIGURE 4. Test circuit and timing waveforms - Continued.

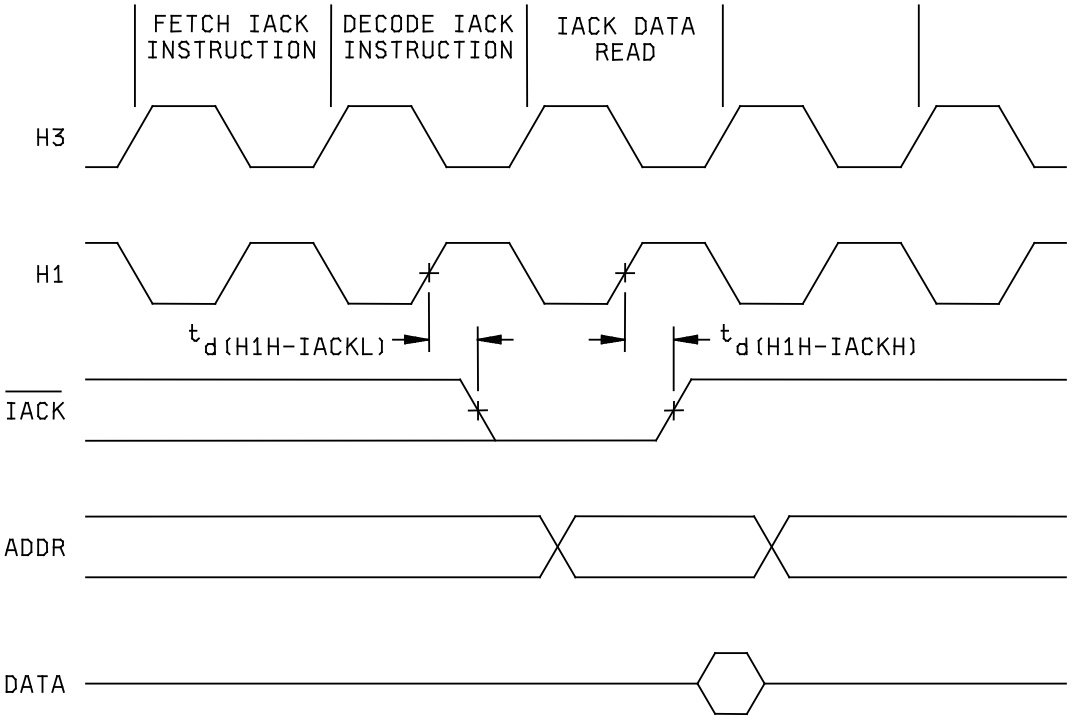


INT3-INT0 RESPONSE TIMING

NOTES:

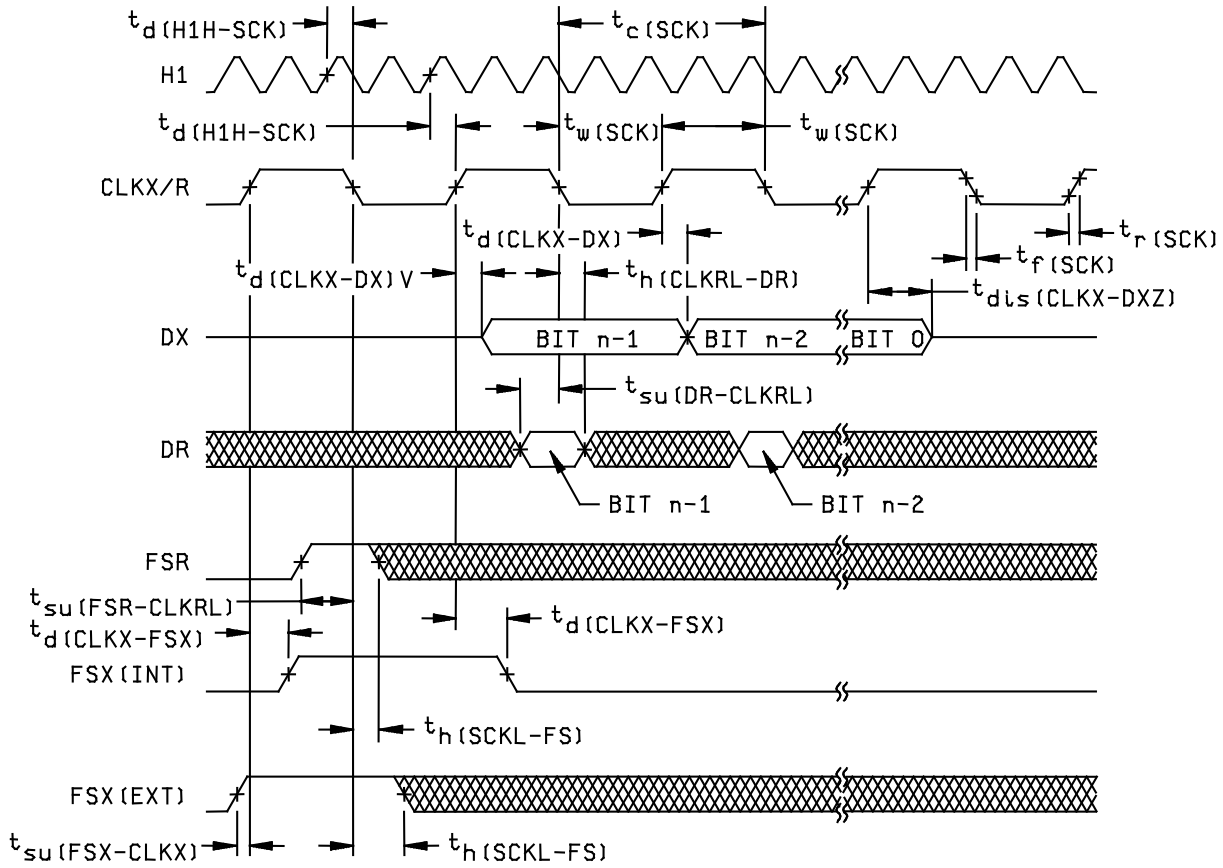
1. Falling edge of H1 just detects INTx falling edge.
2. Falling edge of H1 detects second INTx low, however flag clear takes precedence.
3. Nominal width.
4. Falling edge of H1 misses previous INTx low as INTx rises.

FIGURE 4. Test circuit and timing waveforms - Continued.



INTERRUPT ACKNOWLEDGE ($\overline{IACK}$) TIMING

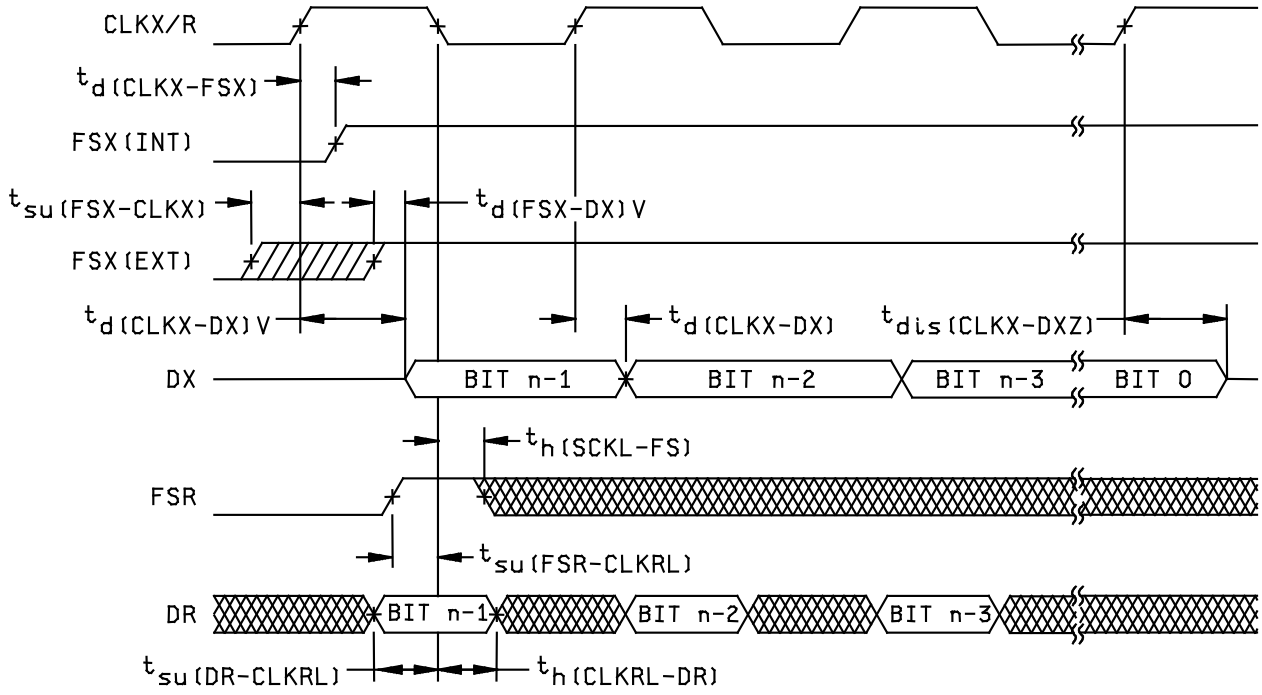
FIGURE 4. Test circuit and timing waveforms - Continued.



FIXED DATA-RATE MODE TIMING

NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

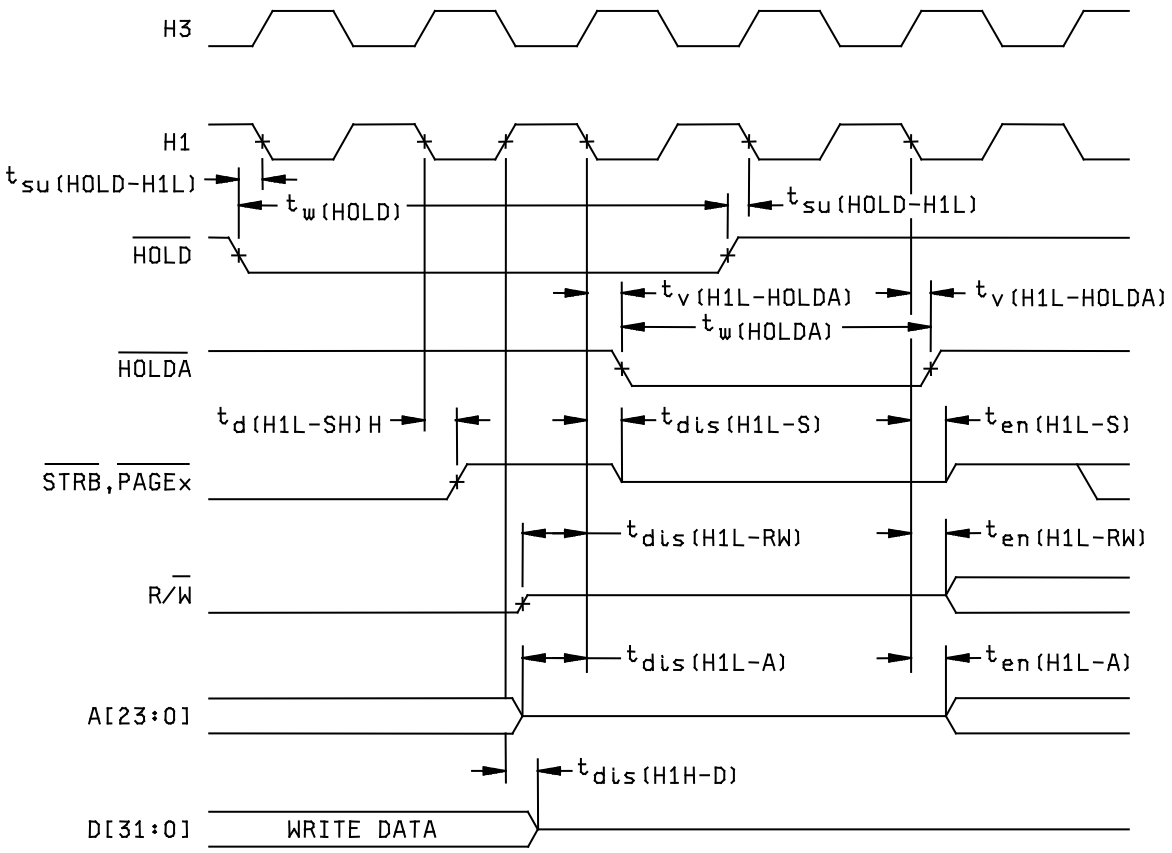
FIGURE 4. Test circuit and timing waveforms - Continued.



VARIABLE DATA-RATE MODE TIMING

NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

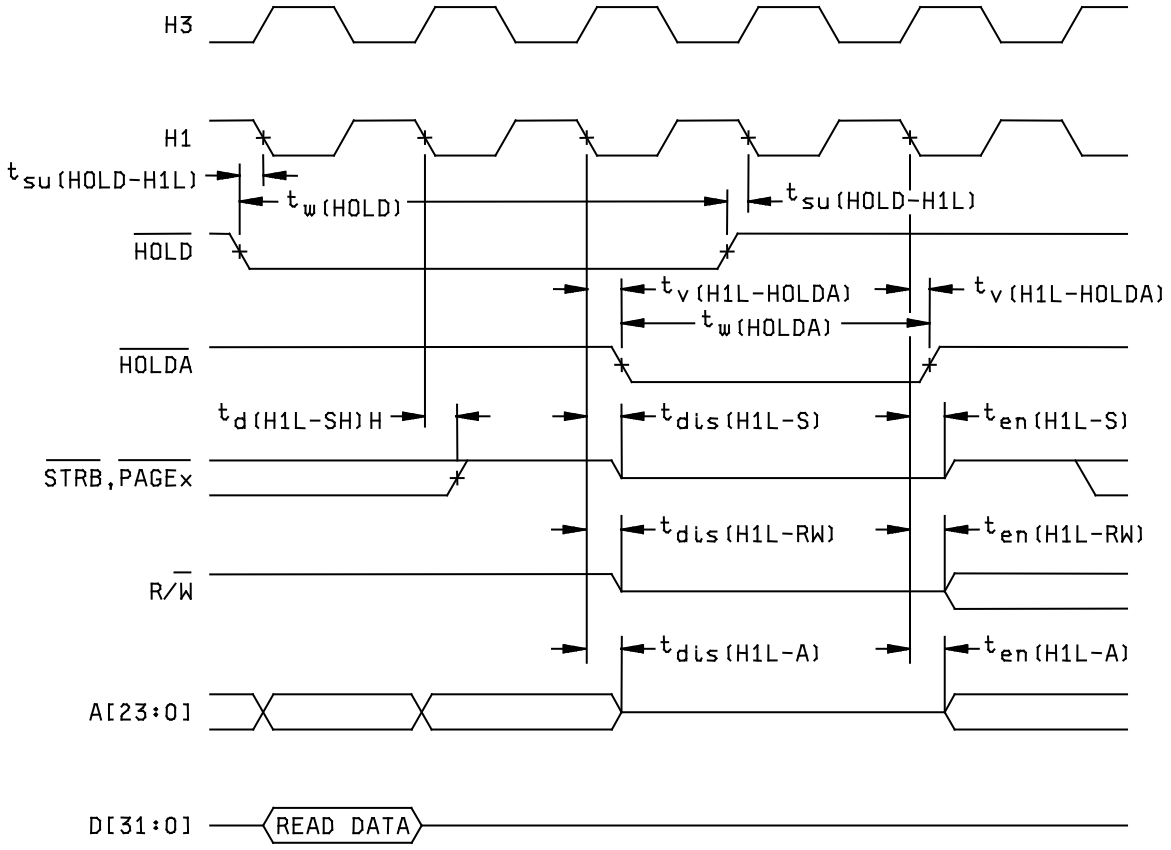
FIGURE 4. Test circuit and timing waveforms – Continued.



TIMING FOR $\overline{HOLD}$/$\overline{HOLDA}$ (AFTER WRITE)

NOTE: $\overline{HOLDA}$ goes low in response to $\overline{HOLD}$ going low and continues to remain low until one H1 cycle after $\overline{HOLD}$ goes back high.

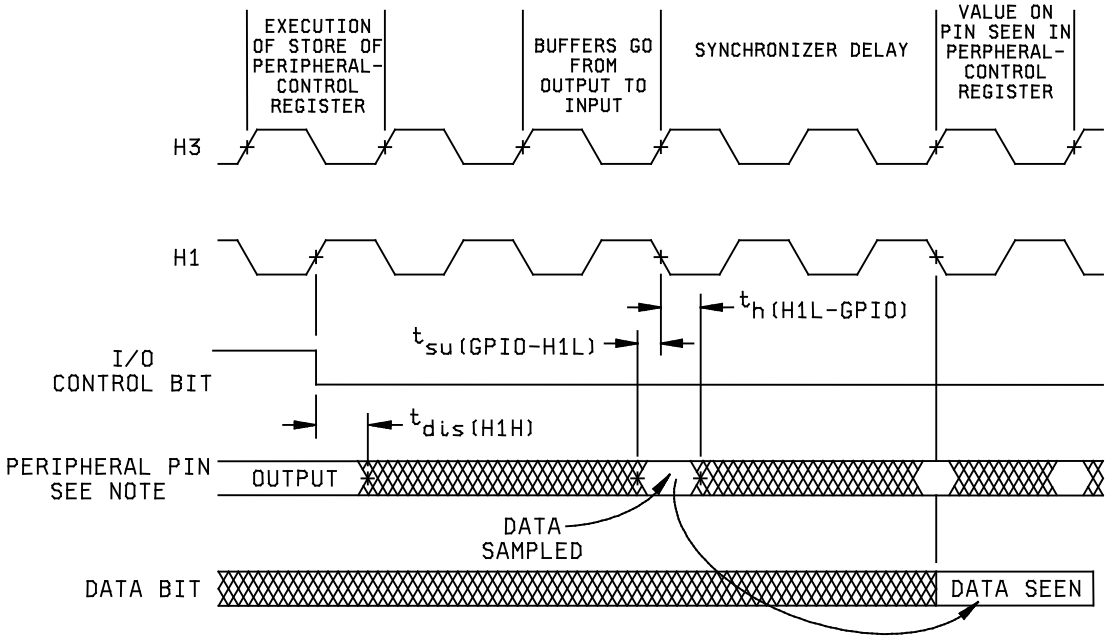
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (AFTER READ)

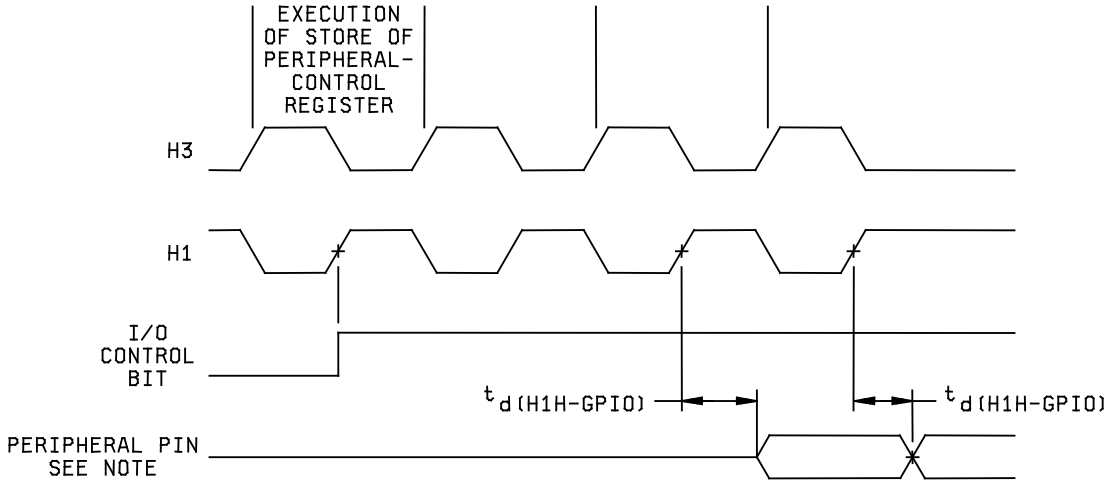
NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

FIGURE 4. Test circuit and timing waveforms - Continued.



CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE OUTPUT TO INPUT MODE TIMING

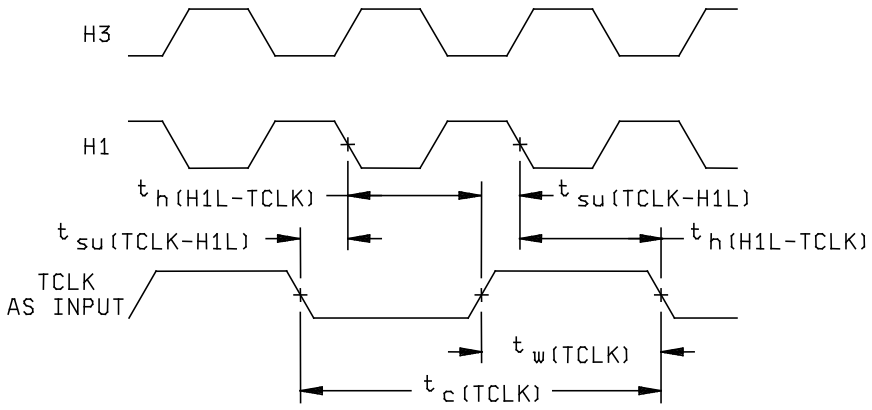
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.



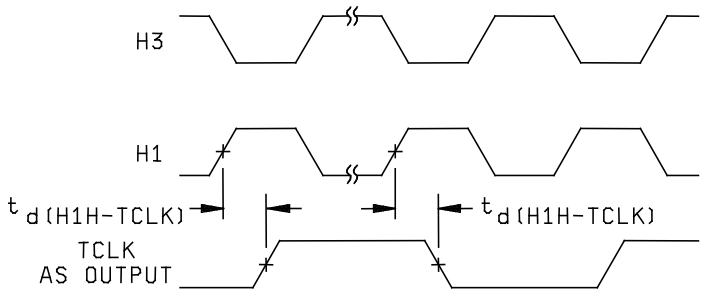
CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE INPUT TO OUTPUT MODE TIMING

NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

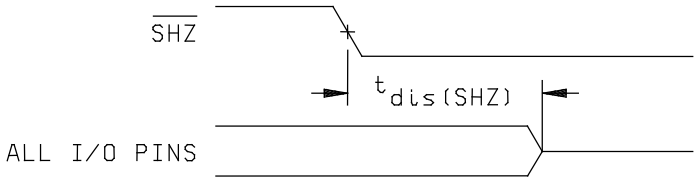
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMER PIN TIMING,INPUT



TIMER PIN TIMING,OUTPUT



TIMING FOR $\overline{SHZ}$

NOTE: Enabling $\overline{SHZ}$ destroys the device register and memory contents. Assert $\overline{SHZ}$ = 1 and reset the device to restore it to a known condition.

FIGURE 4. Test circuit and timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331 and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

TABLE III. Terminal descriptions.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Primary-bus interface			
D31 – D0	I/O/Z	32-bit data port.	S H R
		Data port bus keepers.	S
A23 – A0	O/Z	24-bit address port.	S H R
R/$\overline{W}$	O/Z	Read/Write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over ther parallel interface.	S H R
$\overline{STRB}$	O/Z	Strobe. For all external-accesses.	S H
$\overline{PAGE0}$ - $\overline{PAGE3}$	O/Z	Page strobes. Four decoded page strobes for external access.	S H R
$\overline{RDY}$	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.	
$\overline{HOLD}$	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23 – A0, D31 – D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	
$\overline{HOLDA}$	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic-low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23 – A0, D31 – D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic-high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S
Control signals			
$\overline{RESET}$	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.	
EDGEMODE	I	Edge mode. Enables interrupt edge mode detection.	
$\overline{INT3}$ - $\overline{INT0}$	I	External interrupts.	
$\overline{IACK}$	O/Z	Internal acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate when a section of code is being executed.	S
MCBL/$\overline{MP}$	I	Microcomputer bootloader/microprocessor mode-select.	

See footnotes at end table.

TABLE III. Terminal descriptions - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Control signals – Continued.			
$\overline{SHZ}$	I	Shutdown high impedance. When active, $\overline{SHZ}$ places all pins in the high-impedance state. $\overline{SHZ}$ can be used for board-level testing or to ensure that no dual-drive conditions occur. **Caution:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.	
XF1, XF0	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R
Serial port 0 signals			
CLKR0	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S R
CLKX0	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DR0	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S R
DX0	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSR0	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S R
FSX0	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S R
Timer signals			
TCLK0	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S R
TCLK1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S R
Supply and oscillator signals			
H1	O/Z	External H1 clock.	S
H3	O/Z	External H3 clock.	S
CV_{DD}	I	$+V_{DD}$. Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane. 3/	
DV_{DD}	I	$+V_{DD}$. Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane. 3/	
V_{SS}	I	Ground. All grounds must be connected to a common ground plane.	
$PLLV_{DD}$	I	Internally isolated PLL supply. Connect to CV_{DD} (1.8 V).	
$PLLV_{SS}$	I	Internally isolated PLL ground. Connect to V_{SS}.	

See footnotes at end table.

TABLE III. Terminal descriptions - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Supply and oscillator signals – Continued.			
EXTCLK	I	External clock. Logic level compatible clock input. If the XIN/XOUT oscillator is used, tie this pin to ground.	
XOUT	O	Clock out. Output from the internal-crystal oscillator. If a crystal is not used, XOUT should be left unconnected.	
XIN	I	Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground.	
CLKMD0, CLKMD1	I	Clock mode select pins.	
RSV0, RSV1	I	Reserved. Use individual pullups to DV_{DD}.	
JTAG emulation			
EMU1, EMU0	I/O	Emulation pins 0 and 1. Use individual pullups to DV_{DD}.	
TDI	I	Test data input.	
TDO	O	Test data output.	
TCK	I	Test clock.	
TMS	I	Test mode select.	
$\overline{TRST}$	I	Test reset.	

1/ I = input, O = output, Z = high-impedance state.
2/ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active.
3/ Recommended decoupling. Four 0.1 μF for CV_{DD} and eight 0.1 μF for DV_{DD}.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-08

Approved sources of supply for SMD 5962-00539 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0053901QXA	3/	SMJ320VC33HFGM150
5962-0053901QYA	01295	SMJ320VC33HFGM150
5962-0053901QYC	01295	SMJ320VC33HFGM
5962-0053902QYA	3/	SMJ320VC33HFGM
5962-0053902QYC	3/	SMJ320VC33HFGM

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243