

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change the RHA designator from F to R for device classes M, Q, and V. - ro	01-07-20	R. MONNIN
B	Add information to paragraph 3.5. - ro	04-03-22	R. MONNIN
C	Make a correction to terminal symbol \overline{MR} description as specified under FIGURE 2. - ro	04-09-08	R. MONNIN
D	Make correction to V_{PFO} test description as specified under Table I. - ro	06-02-14	R. MONNIN
E	Make a change to the GND pin as specified under Figure 3. - ro	07-06-22	R. HEBER
F	Make corrections to the V_{CC} and \overline{RESET} pin descriptions as specified under figure 2. - ro	08-08-19	R. HEBER
G	Add figure 4 for a block diagram and figure 5 for two timing waveforms. - ro	09-05-18	J. RODENBECK
H	Make a correction to figure A-1 substrate material from dielectric isolation (DI) to junction isolation (JI). - ro	10-03-09	C. SAFFLE
J	Correct title. Table I, watchdog input (WDI) pulse width test, make correction to condition column by deleting $V_{IH} = 0.8 V$ and substituting $V_{IH} = 0.8 \times V_{CC}$. Add Table IB, paragraphs 2.2, 4.4.4.3h, and 6.7. Add footnote to Table IIB. - ro	10-08-18	C. SAFFLE
K	Under figure 1, case outline X, add the "Q" maximum dimensions 0.045 inch and 1.14 mm. - ro	11-01-25	C. SAFFLE

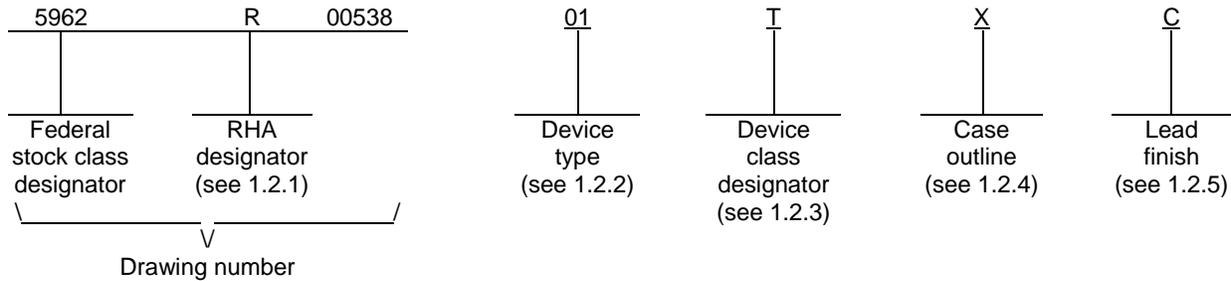
REV																				
SHEET																				
REV	K	K	K	K	K	K	K	K	K	K										
SHEET	15	16	17	18	19	20	21	22	23	24										
REV STATUS OF SHEETS	REV			K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY RAJESH PITHADIA																		
	APPROVED BY RAYMOND MONNIN	MICROCIRCUIT, LINEAR, CMOS, RADIATION HARDENED, POWER-ON, MICROPROCESSOR RESET CIRCUIT, MONOLITHIC SILICON																	
	DRAWING APPROVAL DATE 00-09-27																		
	REVISION LEVEL K		SIZE A	CAGE CODE 67268	5962-00538														
AMSC N/A	SHEET 1 OF 24																		

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	IS-705RH	Radiation hardened, power-on microprocessor reset circuit

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	8	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V _{CC})	0.3 V to 6.0 V
All other inputs	-0.3 V to (V _{CC} + 0.3 V)
Power dissipation (P _D)	2.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T _J)	+175°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ _{JC})	5°C/W
Thermal resistance, junction-to-ambient (θ _{JA})	60°C/W

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.75 V to 5.5 V
Ambient operating temperature range (T _A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):	
Device classes Q, T, and V	1 X 10 ⁵ krad(Si)
Single event latch-up (SEL) to effective LET	≥ 90 MeV/mg/cm ² 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 2/ Guaranteed by design or process but not tested. See manufacturer's SEE test report for more information.

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2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Operating supply voltage	V _{CC}		1,2,3	01	1.2	5.5	V
Supply current	I _{CC}	V _{CC} = 5.5 V	1,2,3	01		500	μA
		M,D,P,L,R 2/	1			500	
Reset section							
Reset threshold voltage	V _{rt}		1,2,3	01	4.50	4.75	V
		M,D,P,L,R 2/	1		4.50	4.75	
Reset threshold voltage hysteresis	V _{RTHYS}		1,2,3	01	20		mV
		M,D,P,L,R 2/	1		20		
Reset pulse width	T _{rs}	V _{CC} = 4.75 V	9,10,11	01	140	280	ms
		M,D,P,L,R 2/	9		140	280	
$\overline{\text{RESET}}$ output voltage	V _{OUT}	V _{CC} = 4.75 V, I _{SOURCE} = 800 μA	1,2,3	01	V _S - 1.5		V
		M,D,P,L,R 2/	1		V _S - 1.5		
		V _{CC} = 4.75 V, I _{SINK} = 3.2 mA	1,2,3			0.4	
		M,D,P,L,R 2/	1			0.4	
		V _{CC} = 1.2 V, I _{OL} = 100 μA	1,2,3			0.3	
		M,D,P,L,R 2/	1			0.3	
Watchdog section							
Watchdog time-out period	t _{WD}	V _{CC} = 5.5 V	9,10,11	01	1.00	2.25	s
		M,D,P,L,R 2/			1.00	2.25	
Watchdog input (WDI) pulse width	t _{WP}	V _{CC} = 4.75 V, V _{IL} = 0.4 V, V _{IH} = 0.8 x V _{CC}	9,10,11	01	50		ns
		M,D,P,L,R 2/			50		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Watchdog section - continued							
Watchdog input (WDI) threshold voltage	V _{IL}	V _{CC} = 4.75 V	1,2,3	01		0.8	V
		M,D,P,L,R 2/	1			0.8	
	V _{IH}	V _{CC} = 5.5 V	1,2,3		3.5		
		M,D,P,L,R 2/	1		3.5		
Watchdog input (WDI) current	I _{WDI}	WDI pin = V _{CC} = 5.5 V	1,2,3	01		100	μA
		M,D,P,L,R 2/	1			100	
		WDI pin = 0 V, V _{CC} = 5.5 V	1,2,3		-100		
	M,D,P,L,R 2/	1	-100				
Watchdog output \overline{WDO} voltage	V \overline{WDO}	V _{CC} = 4.75 V, I _{OH} = 800 μA	1,2,3	01	V _S - 1.5		V
		M,D,P,L,R 2/	1		V _S - 1.5		
		V _{CC} = 4.75 V, I _{OL} = 1.2 mA	1,2,3			0.4	
		M,D,P,L,R 2/	1			0.4	
Manual reset section							
Manual reset (\overline{MR}) pull-up current	I \overline{MR}	\overline{MR} = 0 V, V _{CC} = 5.5 V	1,2,3	01	-500	-100	μA
		M,D,P,L,R 2/	1		-500	-100	
Manual reset (\overline{MR}) pulse width	t \overline{MR}	V _{CC} = 4.75 V	9,10,11	01	150		ns
		M,D,P,L,R 2/	9		150		
Manual reset (\overline{MR}) input threshold voltage	V _{IL}	V _{CC} = 4.75 V	1,2,3	01		0.8	V
		M,D,P,L,R 2/	1			0.8	
	V _{IH}	V _{CC} = 5.5 V	1,2,3		2.0		
		M,D,P,L,R 2/	1		2.0		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Manual reset section – continued.							
Manual reset (\overline{MR}) to reset out delay	t _{MD}	V _{CC} = 4.75 V	9,10,11	01		100	ns
		M,D,P,L,R ^{2/}	9			100	
Threshold detector section							
Threshold detector input (PFI) threshold voltage	V _{PFI}	V _{CC} = 5.0 V	1,2,3	01	1.20	1.30	V
		M,D,P,L,R ^{2/}	1		1.20	1.30	
Threshold detector input (PFI) current	I _{PFI}	V _{CC} = 5.0 V	1,2,3	01	-25.0	+25.0	nA
		M,D,P,L,R ^{2/}	1		-25.0	+25.0	
Threshold detector output (\overline{PFO}) voltage	V _{PFO}	V _{CC} = 4.75 V, I _{OH} = 800 μA	1,2,3	01	V _S – 1.5		V
		M,D,P,L,R ^{2/}	1		V _S – 1.5		
		V _{CC} = 4.75 V, I _{OL} = 3.2 mA	1,2,3			0.4	
		M,D,P,L,R ^{2/}	1			0.4	

^{1/} Unless otherwise specified, V_{CC} = 4.75 V to 5.5 V.

^{2/} Device classes Q, T, and V supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation however, this device is only tested at the R level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

TABLE IB. SEP test limits. ^{1/} ^{2/}

Device type	SEP	Temperature (T _C)	V _{CC}	Effective linear ^{3/} energy transfer (LET)
01	SEL	+125°C	5.5 V	≥ 90 MeV-cm ² /mg

^{1/} For SEP test conditions, see 4.4.4.3 herein.

^{2/} Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

^{3/} Guaranteed by design of process but not tested.

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Case X

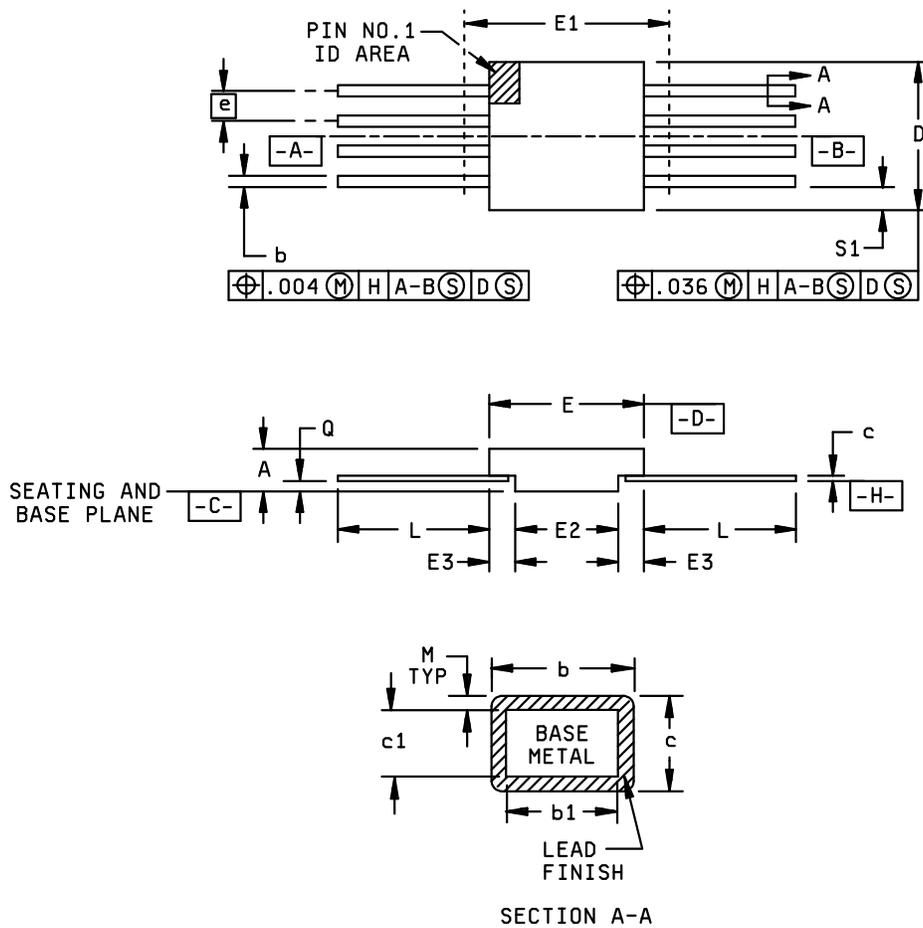


FIGURE 1. Case outline.

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Case X

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.070	0.115	1.18	2.92	
b	0.015	0.022	0.38	0.56	
b1	0.015	0.019	0.38	0.48	
c	0.004	0.009	0.10	0.23	
c1	0.004	0.007	0.10	0.18	
D	0.245	0.265	6.22	6.73	4
E	0.245	0.265	6.22	6.73	
E1	---	0.280	---	7.11	4
E2	0.170	0.180	4.32	4.57	
E3	0.030	---	0.76	---	8
e	0.050 BSC		1.27 BSC		
k	---	---	---	---	3
L	0.250	0.370	6.35	9.40	
Q	0.026	0.045	0.66	1.14	9
S1	0.005	---	0.13	---	7
M	---	0.0015	---	0.04	
N	8		8		

NOTES:

1. The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
6. N is the maximum number or terminal positions.
7. Measure dimension S1 at all four corners.
8. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
9. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outline – Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	\overline{MR}
2	V _{CC}
3	GND
4	PFI
5	\overline{PFO}
6	WDI
7	\overline{RESET}
8	\overline{WDO}

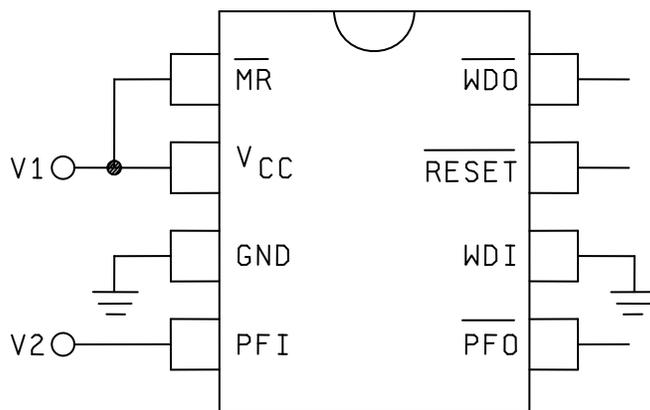
FIGURE 2. Terminal connections.

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Terminal symbol	Description
$\overline{\text{MR}}$	Manual reset input. An active low TTL/CMOS compatible (150 ns minimum pulse width) input that may be used to generate a reset pulse.
V_{CC}	Power supply voltage. Connect the voltage to be monitored to this pin. $\overline{\text{RESET}}$ is guaranteed operable after V_{CC} rises above 1.2 V. See $\overline{\text{RESET}}$ pin for details.
GND	Ground. This pin should be tied to power ground. It establishes the reference for voltage detection.
PFI	Threshold detector input. An input pin for the 1.25 V threshold detector, which may be used to monitor a power fail or low battery condition, or for monitoring other voltage supply levels.
$\overline{\text{PFO}}$	Threshold detector output. A low active output that indicates that the input connected to PFI pin is less than 1.25 V.
WDI	Watchdog input. A three state watchdog input that monitors microprocessor activity. If the microprocessor does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not three stated, $\overline{\text{WDO}}$ goes low. As long as $\overline{\text{RESET}}$ is asserted of the WDI input is three stated, the watchdog timer will stay cleared and will not count. As soon as the reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50 ns can be detected. Floating WDI or connecting WDI to a high impedance three state buffer disables the watchdog feature (WDON = "1").
$\overline{\text{RESET}}$	Reset. On power up, once V_{CC} reaches 1.2 V, $\overline{\text{RESET}}$ is guaranteed logic low. As V_{CC} rises, $\overline{\text{RESET}}$ stays low. When V_{CC} rises above the reset threshold, 4.65 V (typical), an internal timer releases $\overline{\text{RESET}}$ after about 200 ms. $\overline{\text{RESET}}$ pulses low whenever V_{CC} goes below the reset threshold. If this brownout condition occurs in the middle of a previously initiated reset pulse, the pulse will continue for at least 140 ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed low until V_{CC} drops below 1.2 V.
$\overline{\text{WDO}}$	Watchdog output. This output goes low if the microprocessor does not toggle the WDI input within 1.6 seconds and WDI is not three stated. This pin is usually connected to the non-maskable interrupt input of the microprocessor. When V_{CC} drops below 4.65 V, $\overline{\text{WDO}}$ will go low whether or not the watchdog timer has timed out yet. $\overline{\text{RESET}}$ goes low simultaneously, thus preventing an interrupt. If WDI is left unconnected, $\overline{\text{WDO}}$ can be used as low line output. Since floating WDI disables the internal timer, $\overline{\text{WDO}}$ goes low only when V_{CC} drops below 4.65 V, thus functioning as a low line output.

FIGURE 2. Terminal connections – Continued.

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NOTES:

V1 = 5.5 V ± 5 %

V2 = 1.4 V ± 5 %

FIGURE 3. Radiation exposure circuit.

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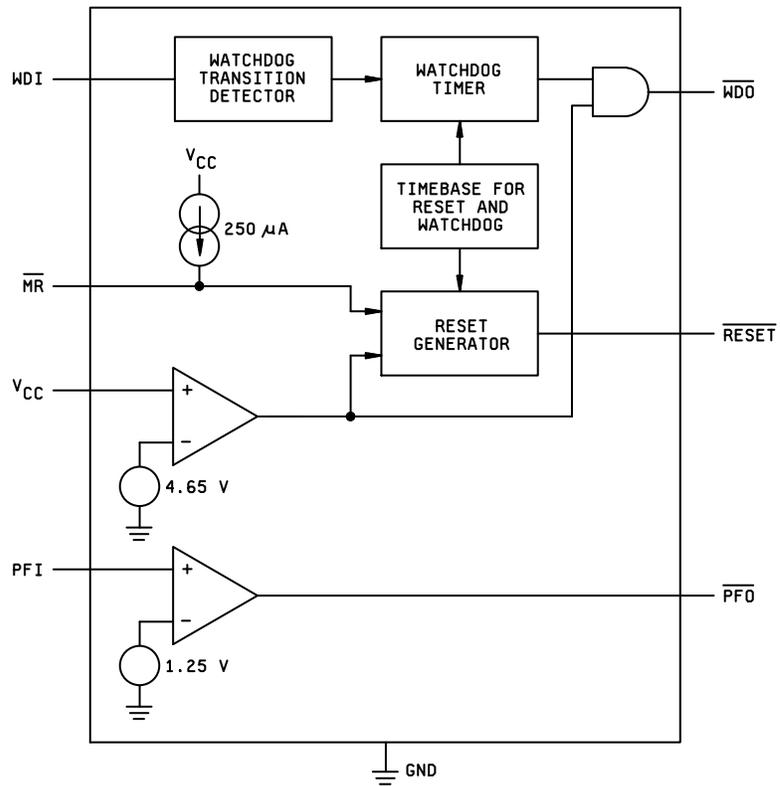


FIGURE 4. Block diagram.

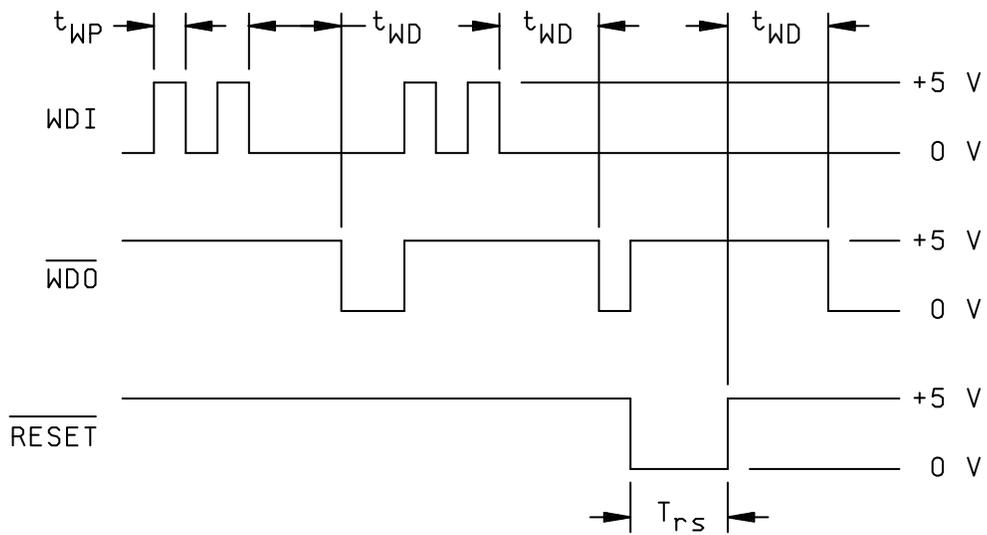
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DLA LAND AND MARITIME
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5962-00538

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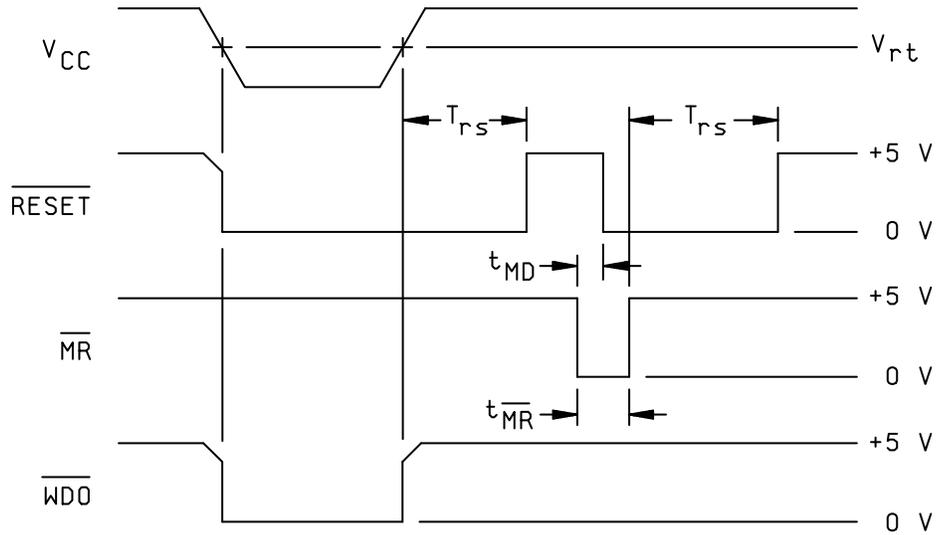
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$\overline{\text{RESET}}$ EXTERNALLY TRIGGERED BY $\overline{\text{MR}}$

FIGURE 5. Timing waveforms.

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\overline{MR} EXTERNALLY DRIVEN LOW

FIGURE 5. Timing waveforms – continued.

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3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q, T and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	---	1,9	1,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,9,10,11 <u>1/</u>	1,2,3, <u>1/</u> 9,10,11	1,2,3, <u>2/ 3/</u> 9,10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	---	1,2,3,9,10,11	1,2,3, <u>3/</u> 9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	---	1,9	1,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	---	1,9	1,9	As specified in QM plan

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1, 9, and deltas.

3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Delta limits
Supply current	I _{CC}	±50 μA

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class T and V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (for example, $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^\circ\text{C}$ and the maximum rated operating temperature $\pm 10^\circ\text{C}$.
- f. Bias conditions shall be defined by the manufacturer for the latchup measurements.
- g. Test four devices with zero failures.
- h. For SEL test limits, see Table IB herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Occurrence of latchup (SEL).

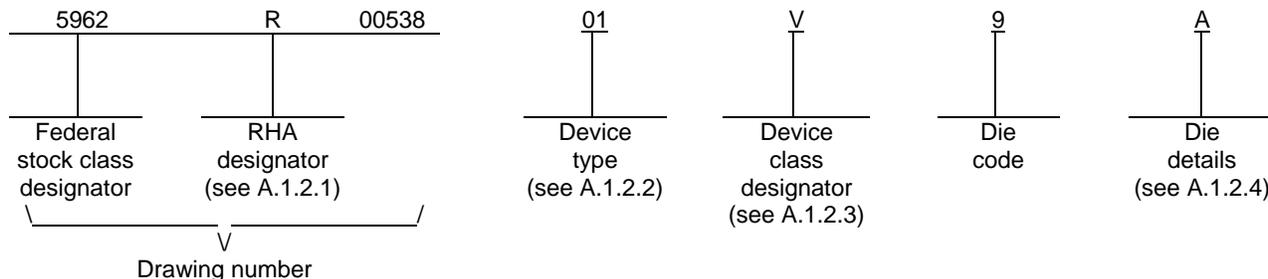
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APPENDIX A
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	IS-705RH	Radiation hardened power-on microprocessor reset circuit

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

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A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

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A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

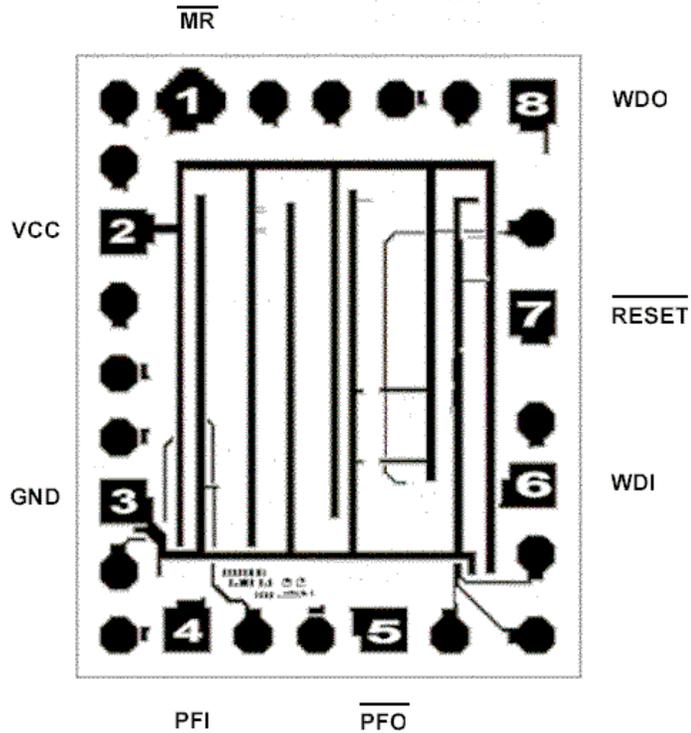
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.

Die size: 59 mils x 72 mils.

Die thickness: 19 mils ± 1 mils.

Interface materials.

Top metallization: Ti Al Cu

Thickness: 16.0 kÅ ± 2 kÅ

Backside metallization: Si

Glassivation.

Type: Nitride (Si₃N₄) over silox (SiO₂)

Nitride thickness: 4 kÅ ± 1 kÅ

Silox thickness: 12 kÅ ± 4 kÅ

Substrate: JI (junction isolation)

Assembly related information.

Substrate potential: Unbiased. (May be left floating or connected to GND).

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-01-25

Approved sources of supply for SMD 5962-00538 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.dscc.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962F0053801QXC	<u>3/</u>	IS9-705RH-8
5962F0053801VXC	<u>3/</u>	IS9-705RH-Q
5962F0053801V9A	<u>3/</u>	IS0-705RH-Q
5962R0053801QXC	34371	IS9-705RH-8
5962R0053801TXC	34371	IS9-705RH-T
5962R0053801VXC	34371	IS9-705RH-Q
5962R0053801V9A	34371	IS0-705RH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

34371

Vendor name and address

Intersil Corporation
 1001 Murphy Ranch Road
 Milpitas, CA 95035-6803

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.