REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correction to TABLE I, I_{DD} parameter. Added Appendix B to allow for the procurement of die. - glg	00-12-11	Raymond Monnin
B	Correction to Appendix B, added paragraph 10.2.4 Die code. Updated boilerplate references. - ksr	02-01-05	Raymond Monnin
C	Add 02 device representing an extended temperature device. Corrected (SEP) effective with no latch-up in paragraph 1.5; was 90.5 MeV-cm2/mg changed to 80 MeV-cm2/mg - ksr	02-10-22	Raymond Monnin
D	Added devices 03 and 04, updated Table I. - ksr	02-12-08	Raymond Monnin
E	Added devices 05 and 06 updated Table I. Added case outline Y. Boilerplate update, part of 5 year review. - ksr	07-03-29	Robert M. Heber
F	Corrected Table I, the post radiation limit for I_{DD2} for devices 05 and 06. - ksr	07-04-11	Robert M. Heber
G	Made corrections to case U dimension table symbol A, D, E1, and E2. - ksr	09-09-24	Charles F. Saffle
H	Update radiation features to section 1.5 and add SEP table IB. Remove all class M references. Correct table I to table IA. Update drawing to reflect current MIL-PRF-38535 requirements. – llb	17-06-01	Charles F. Saffle
J	Update drawing to reflect current MIL-PRF-38535 requirements. Update 1.2.2, 1.3, 1.5, table IA, table IB, figures 4 and 5 for update to R Level RHA and addition of devices 07 and 08. – llb	20-04-08	James R. Eschmeyer
K	Adding Data hold time test condition back to table IA that was omitted in previous revision. Removed duplicate of 4.4.4.1 and resequenced rest of section 4. Update boilerplate to current MIL-PRF-38535 requirements and Accessibility/Section 508 compliance. – llb	22-12-05	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K						
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38						
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
Gary L. Gross

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
00-09-19

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

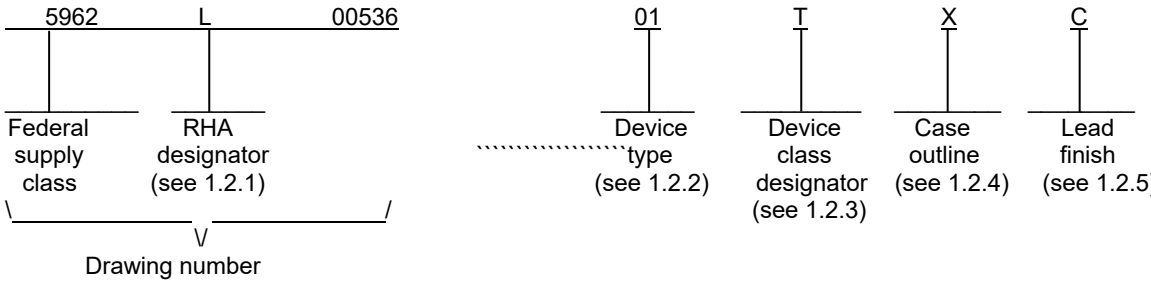
MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K x 8-BIT, RADIATION-HARDENED SRAM, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL K	SIZE A	CAGE CODE **67268**	**5962-00536**
		SHEET	1 OF 33	

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	9Q512	512K X 8-bit Radiation-hardened SRAM (MIL Temp)	25 ns
02	9Q512	512K X 8-bit Radiation-hardened SRAM (Extended Temp)	25 ns
03	9Q512	512K X 8-bit Radiation-hardened SRAM (MIL Temp)	20 ns
04	9Q512	512K X 8-bit Radiation-hardened SRAM (Extended Temp)	20 ns
05	9Q512E	512K X 8-bit Radiation-hardened SRAM (MIL Temp)	20 ns
06	9Q512E	512K X 8-bit Radiation-hardened SRAM (Extended Temp)	20 ns
07	9Q512E	512K X 8-bit Radiation-hardened SRAM (MIL Temp)	20 ns
08	81SRR512K8	512K X 8-bit Radiation-hardened SRAM (Industrial Temp)	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	36	Flat pack
X	See figure 1	36	Flat pack
Y	See figure 1	36	Flat pack

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{DD})	-0.5 V dc to +7.0 V dc
Voltage range on any input pin	-0.5 V dc to +7.0 V dc
Voltage range on any output pin	-0.5 V dc to +7.0 V dc
Input current, dc	± 10 mA
Power dissipation	1.0 W
Case temperature range, (T_C) (Devices 01, 03, 05, and 07)	-55°C to +125°C
Case temperature range, (T_C) (Devices 02, 04, and 06)	-40°C to +125°C
Operating case temperature, (T_C) (Device 08)	-40°C to +105°C
Storage temperature range, (T_{STG})	-65°C to +150°C
Junction temperature, (T_J)	+150°C
Thermal resistance, junction-to-case, (θ_{JC}): Case X and U	+10°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{DD})	+4.5 V dc to +5.5 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to VDD
Case temperature, (T_C) (Devices 01, 03, 05, and 07)	-55°C to +125°C
Case temperature, (T_C) (Devices 02, 04, and 06)	-40°C to +125°C
Operating case temperature, (T_C) (Device 08)	-40°C to +105°C

1.5 Radiation features

Maximum total dose available (dose rate = 50 – 300 Rad(Si)/s)	100K Rad(Si) 4/
Single event phenomenon (SEP):	
For device types 01, 02, 03, and 04:	
No SEL occurs at effective LET (see 4.4.4)	≤ 80 MeV-cm^2/mg 5/
No SEU occurs at onset LET (see 4.4.4)	≤ 1.0 MeV-cm^2/mg 5/
For device types 05, 06, 07, and 08:	
No SEL occurs at effective LET (see 4.4.4)	≤ 110 MeV-cm^2/mg 5/
No SEU occurs at onset LET (see 4.4.4)	≤ 2.8 MeV-cm^2/mg 5/

1.6 Digital logic testing for device classes T, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values in this drawing are with respect to V_{SS}.
4/ Device types 01 – 08 are irradiated at a dose rate = 50 – 300 Rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and radiation end point limits for the noted parameters are guaranteed to a maximum total dose specified herein.
5/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T, and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix B to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q, T, and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T, and V, the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ (Devices 01, 03, 05, 07) $-40°C \le T_C \le +125°C$ (Devices 02,04,06) $-40°C \le T_C \le +105°C$ (Device 08) $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}		1, 2, 3	All	2.0		V
			M, D, P, L, R	1		1/ 2/		
Low-level input voltage	V_{IL}		1, 2, 3	All		0.8	V
			M, D, P, L, R	1			1/ 2/	
High-level output voltage	V_{OH1}	I_{OH} = -4 mA, V_{DD} = 4.5 V	1, 2, 3	All	2.4		V
			M, D, P, L, R	1		1/ 2/		
High-level output voltage	V_{OH2}	I_{OH} = -200 µA, V_{DD} = 4.5 V	1, 2, 3	All	3.2		V
			M, D, P, L, R	1		1/ 2/		
Low-level output voltage	V_{OL1}	I_{OL} = 8.0mA, V_{DD} = 4.5 V	1, 2, 3	All		0.4	V
			M, D, P, L, R	1		1/ 2/		
Low-level output voltage	V_{OL2}	I_{OL} = 200 µA, V_{DD} = 4.5 V	1, 2, 3	All		0.05	V
			M, D, P, L, R	1			1/ 2/	
Input capacitance	C_{IN}	See 4.4.1e, f = 1 MHz at 0 V, T_C = 25°C 3/	V_{IN} = 25 mV	4	1 – 6		10	pF
					07, 08		14	
Bi-directional I/O capacitance	$C_{I/O}$		$V_{I/O}$ = 25 mV	4	1 – 6		12	pF
					07, 08		16	
Input current (leakage)	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$		1, 2, 3	All	-2.0	+2.0	µA
		$V_{DD} = V_{DD}$(max)	M, D, P, L, R	1		1/ 2/	1/ 2/	
Three-state output current (leakage)	I_{OZ}	$0\ V \le V_O \le V_{DD}$, V_{DD} = V_{DD} (max) ~~G~~ = V_{DD} (max)		1, 2, 3	All	-2.0	+2.0	µA
			M, D, P, L, R	1		1/ 2/	1/ 2/	
W2Short-circuit output current 4/ 5/	I_{OS}	$0\ V \le V_O \le V_{DD}$		1, 2, 3	All	-90	+90	mA
			M, D, P, L, R	1		1/ 2/	1/ 2/	
Operating supply current at 1MHz 6/	I_{DD}	Inputs: $V_{IL} = V_{SS}$ +0.8 V, V_{IH} = 2.0 V, I_{OUT} = 0 mA, $V_{DD} = V_{DD}$(max)		1, 2, 3	01 – 04		135	mA
					05 – 08		50	
			M, D, P, L, R	1	All		1/ 2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ (Devices 01, 03, 05, 07) $-40°C \le T_C \le +125°C$ (Devices 02,04,06) $-40°C \le T_C \le +105°C$ (Device 08) $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Operating supply current at: 40MHz (devices 01 – 04) 50 MHz (devices 05 – 08) 6/	I_{DD1}	Inputs: $V_{IL} = V_{SS} + 0.8\ V$ $V_{IH} = 2.0\ V$, $I_{OUT} = 0\ mA$ $V_{DD} = V_{DD}(max)$		1, 2, 3	01 – 04		18	mA
					05 – 08		76	
			M, D, P, L, R	1	All		1/ 2/	
Standby supply current at 0 MHz	I_{DD2}	$\overline{E} = V_{DD} - 0.5\ V$, $V_{DD}(max)$ $V_{IH} = V_{DD} - 0.5\ V$ Inputs: $V_{IL} = V_{SS}$ $I_{OUT} = 0\ mA$		01	01 – 04		6	mA
					05, 06		10	
					07, 08		16	
				2	01 – 04		12	
					05 – 08		45	
			M, D, P, L, R	1	01 -04		1/ 2/	
			M, D, P, L, R	1	05 -08		45	
Functional test		See 4.4.1c, $V_{IH} = V_{DD} - 0.5\ V$		7, 8A, 8B	All			
			M, D, P, L, R	7			1/ 2/	
Read cycle time 7/ 8/	t_{AVAV}	See figures 4 and 5		9, 10, 11	01, 02	25		ns
					03 – 08	20		
			M, D, P, L, R	9	All	1/ 2/		
Address valid to address valid skew time 9/	t_{AVSK}			9, 10, 11	05 – 08		4	ns
			M, D, P, L, R	9			1/ 2/	
Read access time	t_{AVQV}			9, 10, 11	01 – 04		25	ns
					05 – 08		20	
			M, D, P, L, R	9	All		1/ 2/	
Output hold time	t_{AXQX}			9, 10, 11	All	3		ns
			M, D, P, L, R	9		1/ 2/		
$\overline{G}$-controlled output enable time 10/	t_{GLQX}			9, 10, 11	All	0		ns
			M, D, P, L, R	9		1/ 2/		
$\overline{G}$-controlled output enable time (read cycle 3)	t_{GLQV}			9, 10, 11	All		10	ns
			M, D, P, L, R	9			1/ 2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ (Devices 01, 03, 05, 07) $-40°C \le T_C \le +125°C$ (Devices 02,04,06) $-40°C \le T_C \le +105°C$ (Device 08) $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
$\overline{G}$-controlled output three-state time 10/	t_{GHQZ}		9, 10, 11	All		10	ns
		M, D, P, L, R	9			1/ 2/	
$\overline{E}$-controlled output enable time 11/	t_{ETQX}		9, 10, 11	All	3		ns
		M, D, P, L, R	9		1/ 2/		
$\overline{E}$-controlled address setup time for read 9/	t_{AVET2}		9, 10, 11	05 – 08	-4		ns
		M, D, P, L, R	9		1/ 2/		
$\overline{E}$-controlled access time	t_{ETQV}	See figures 4 and 5	9, 10, 11	01 – 04		25	ns
		M, D, P, L, R	9	05 – 08		20	
$\overline{E}$-controlled output three-state time 7/ 10/ 12/	t_{EFQZ}		9, 10, 11	All		10	ns
		M, D, P, L, R	9			1/ 2/	
Write cycle time 13/	t_{AVAV}		9, 10, 11	01, 02	25		ns
				03 – 08	20		
		M, D, P, L, R	9	All	1/ 2/		
Device enable to end of write	t_{ETWH}		9, 10, 11	All	20		ns
		M, D, P, L, R	9		1/ 2/		
Address setup time for write ($\overline{E}$-controlled)	t_{AVET}		9, 10, 11	All	0		ns
		M, D, P, L, R	9		1/ 2/		
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}		9, 10, 11	All	20		ns
		M, D, P, L, R	9		1/ 2/		
Write pulse width	t_{WLWH}		9, 10, 11	All	20		ns
		M, D, P, L, R	9		1/ 2/		
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		9, 10, 11	01 – 04	0		ns
				05 – 08	2		
		M, D, P, L, R	9	All	1/ 2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ (Devices 01, 03, 05, 07) $-40°C \le T_C \le +125°C$ (Devices 02,04,06) $-40°C \le T_C \le +105°C$ (Device 08) $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Address hold time for device enable ($\overline{E}$-controlled)	t_{EFAX}	See figures 4 and 5		9, 10, 11	All	0		ns
			M, D, P, L, R	9		1/ 2/		
$\overline{W}$-controlled three-state time 10/	t_{WLQZ}			9, 10, 11	All		10	ns
			M, D, P, L, R	9			1/ 2/	
$\overline{W}$-controlled output enable time 10/	t_{WHQX}			9, 10, 11	01 – 04	5		ns
					05 – 08	4		
			M, D, P, L, R	9	All	1/ 2/		
Device enable pulse width ($\overline{E}$-controlled)	t_{ETEF}			9, 10, 11	All	20		ns
			M, D, P, L, R	9		1/		
Data setup time	t_{DVWH}			9, 10, 11	All	15		ns
			M, D, P, L, R	9		1/ 2/		
Data hold time	t_{WHDX}			9, 10, 11	All	2		ns
			M, D, P, L, R	9		1/ 2/		
Device enable controlled write pulse width	t_{WLEF}			9, 10, 11	All	20		ns
			M, D, P, L, R	9		1/ 2/		
Data setup time	t_{DVEF}			9, 10, 11	All	15		ns
			M, D, P, L, R	9		1/ 2/		
Data hold time	t_{EFDX}			9, 10, 11	All	2		ns
			M, D, P, L, R	9		1/ 2/		
Address valid to end of write	t_{AVWH}			9, 10, 11	All	20		ns
			M, D, P, L, R	9		1/ 2/		
Write disable time 13/	t_{WHWL}			9, 10, 11	All	5		ns
			M, D, P, L, R	9		1/ 2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

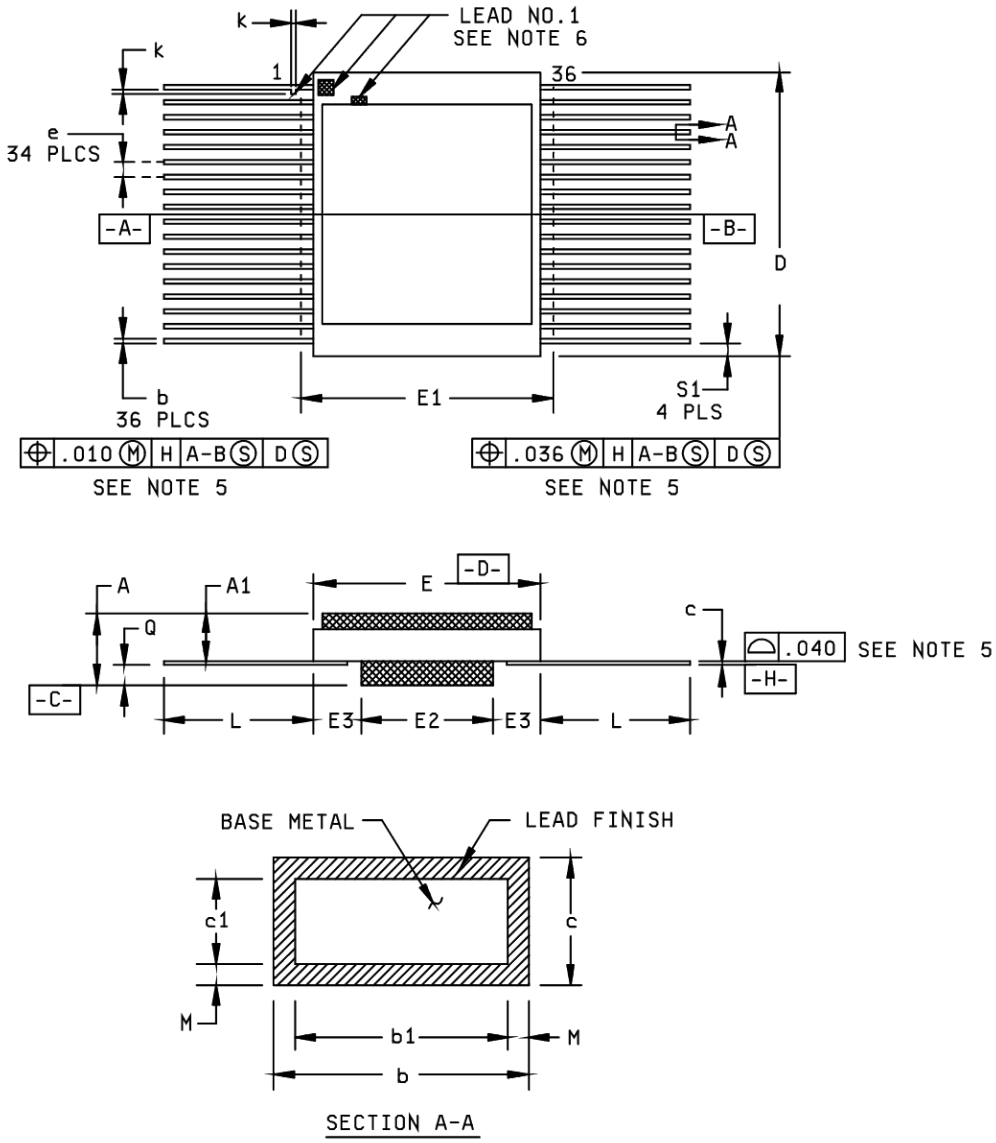
1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the R (100KRad(Si)) TID level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
3/ Measured only for initial qualification and after any design or process changes which may affect this parameter.
4/ Supplied as a design limit but not guaranteed or tested.
5/ Not more than one output may be shorted at a time for maximum duration of one second.
6/ $\overline{G} = V_{IH}$
7/ This is a functional test.
8/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation.
9/ Guaranteed by design.
10/ See figure 5, timing waveforms (High-Z to active level and active to High-Z level waveform).
11/ The ET (enable true) notation refers to the falling edge of $\overline{E}$. SEU immunity does not affect the read parameters.
12/ The EF (enable false) notation refers to the rising edge of $\overline{E}$. SEU immunity does not affect the read parameters.
13/ Functional test performed with outputs disabled ($\overline{G}$ high).

Table IB. SEP test limits 1/ 2/ 3/

Device type	Single event upset V_{DD} = 4.5 V No upsets at onset LET	Single event latch-up Bias V_{DD} =5.5 V No latch-up at effective LET
01 – 04	LET ≤ 1.0 MeV/(mg/cm^2)	LET ≤ 80 MeV/(mg/cm^2)
05 – 08	LET ≤ 2.8 MeV/(mg/cm^2)	LET ≤ 110 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case test temperature T_A = +25°C ± 10°C for SEU and T_A = +125°C ± 10°C for SEL.

Case outline X



Notes:

1. All exposed metallized areas must be gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid and slug are electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumeric. One or both ID methods may be used for pin 1 ID.

FIGURE 1. Case outlines.

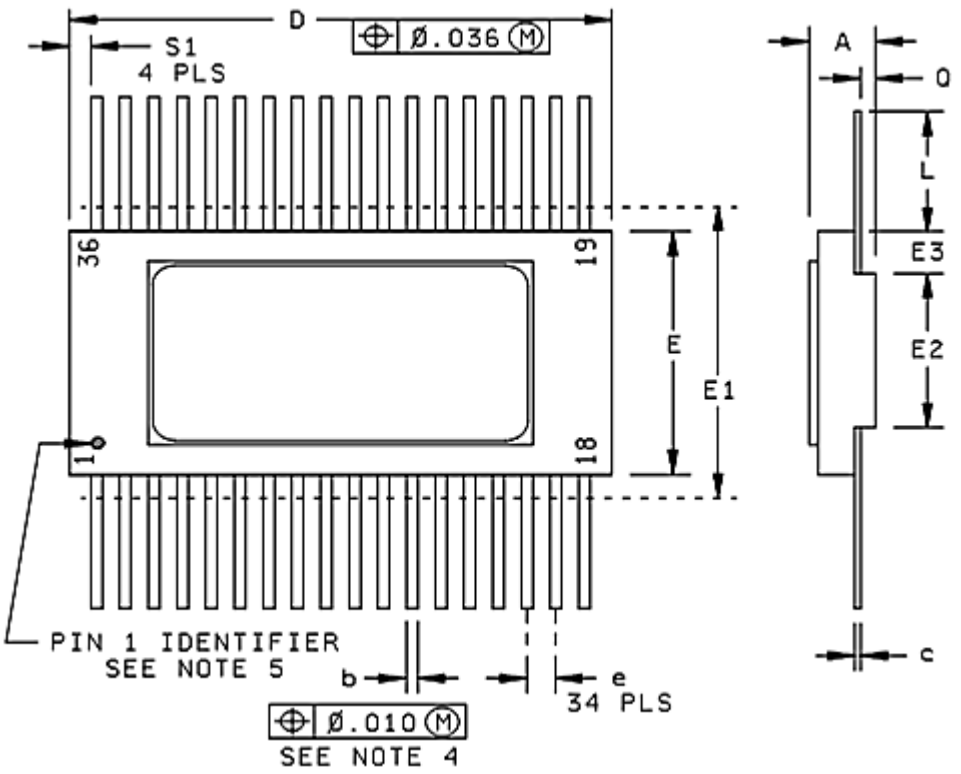
Case outline X – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.35	4.42	.132	.174
A1	2.59	3.40	.102	.134
b	.381	.559	.015	.022
b1	.381	.483	.015	.019
c	.102	.229	.004	.009
c1	.102	.152	.004	.006
D	23.62 max		.930 max	
E	11.99	12.40	.472	.488
E1	12.62 max		.498 max	
E2	9.02 min		.355 min	
E3	.762 min		.030 min	
e	1.27 BSC		.050 BSC	
k	.229	.381	.009	.015
L	7.75	8.25	.305	.325
Q	.661	.787	.026	.031
S1	.127 min		.005 min	
M	.038 max		.0015 max	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outlines – Continued.

Case outline U

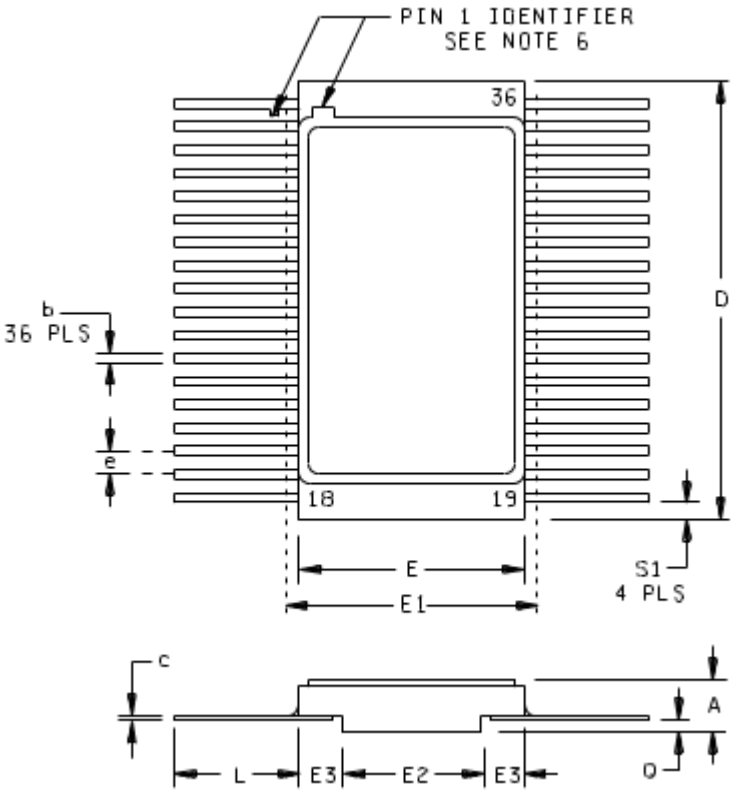


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.82	3.48	.111	.137
b	0.38	0.51	.015	.020
c	0.10	0.18	.004	.007
D	23.11	23.62	.910	.930
E	12.07	12.32	.475	.485
E1		13.08		.515
E2	9.96	10.36	.392	.408
E3	0.76		.030	
e	1.27 BSC		.050 BSC	
L	7.75	8.26	.305	.325
S1	0.13		.005	
Q	0.64	1.14	.025	.045

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metallized areas are gold plated over electroplated nickel.
3. Package lid is electrically connected to V_{SS}.
4. Lead position and coplanarity are not measured.
5. Pin 1 identification area.

FIGURE 1. Case outlines – Continued.

Case Y



Notes:
1. All exposed metallized areas must be gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumeric. One or both ID methods may be used for pin 1 ID.

FIGURE 1. Case outlines – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.64	3.30	.104	.130
b	.381	.483	.015	.019
c	.102	.152	.004	.006
D	23.11	23.62	.910	.930
E	14.53	14.94	.572	.588
E1	15.49 max		.610 max	
E2	11.99	12.40	.472	.488
E3	.762		.030	
e	1.27 BSC		.050 BSC	
L	8.64	9.14	.340	.360
Q	.635		.025	
S1	.127 min		.005 min	

FIGURE 1. Case outlines – Continued.

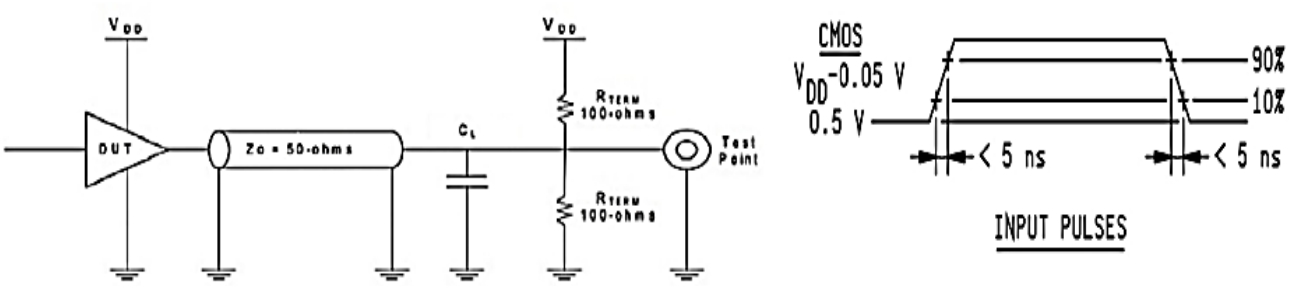
Device types	All
Case outlines	U, X, and Y
Terminal number	Terminal symbol
1	A_0
2	A_1
3	A_2
4	A_3
5	A_4
6	$\overline{E}$
7	DQ_0
8	DQ_1
9	V_{DD}
10	V_{SS}
11	DQ_2
12	DQ_3
13	$\overline{W}$
14	A_5
15	A_6
16	A_7
17	A_8
18	A_9
19	NC
20	A_{10}
21	A_{11}
22	A_{12}
23	A_{13}
24	A_{14}
25	DQ_4
26	DQ_5
27	V_{DD}
28	V_{SS}
29	DQ_6
30	DQ_7
31	$\overline{G}$
32	A_{15}
33	A_{16}
34	A_{17}
35	A_{18}
36	NC

FIGURE 2. Terminal connections.

$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X 1/	X	1	3-state	Standby
X	0	0	Data-in	Write
1	1	0	3-state	Read 2/
0	1	0	Data out	Read

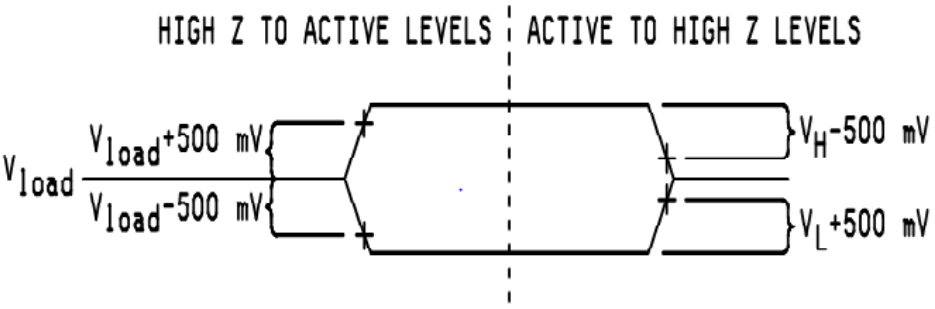
1/ X is defined as a “don’t care” condition.
2/ Device active; outputs disabled.

FIGURE 3. Truth table.

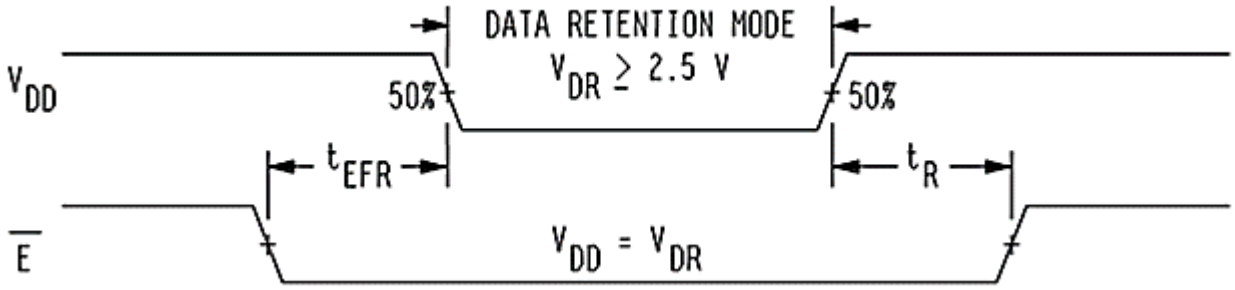


Notes: 1. 50 pF includes scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

FIGURE 4. Output load circuit and input waveforms.



Low V_{DD} data retention waveform devices 01, 02, 03, and 04.



Data retention characteristics (pre/post-irradiation) for devices 01, 02, 03, and 04
(**1** second data retention test)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention	2.5	---	V
I_{DDR} 1/ 2/	Data retention current	---	5.0	mA
t_{EFR} 1/ 3/	Chip deselect to data retention time	0		ns
t_R 1/ 3/	Operation recovery time	t_{AVAV}		ns

1/ $\overline{E}$ = V_{SS}, all other inputs = V_{DR} or V_{SS}.
2/ Data retention current (I_{DDR}) T_C = 25°C.
3/ Not guaranteed or tested.

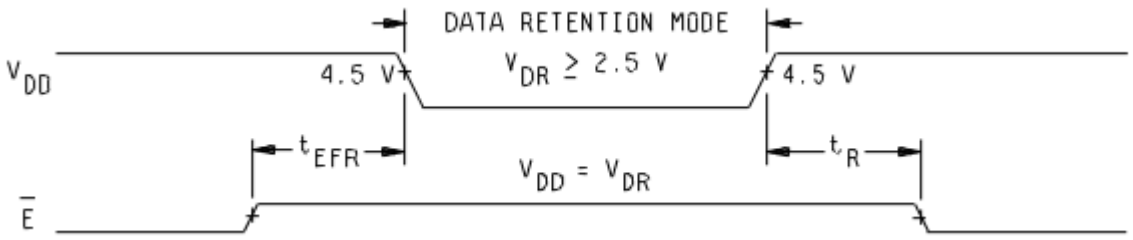
FIGURE 5. Timing waveforms.

Data retention characteristics (pre/post-irradiation) for devices 01, 02, 03, and 04
(**10** second data retention test)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DR} 1/	V_{DD} for data retention	4.5	5.5	V
t_{EFR} 2/ 3/	Chip deselect to data retention time	0		ns
t_R 2/ 3/	Operation recovery time	t_{AVAV}		ns

1/ Performed at V_{DD} (min) and V_{DD} (max).
2/ $\overline{E}$ = V_{SS}, all other inputs = V_{DR} or V_{SS}.
3/ Not guaranteed or tested.

Low V_{DD} data retention waveform devices 05 – 08.



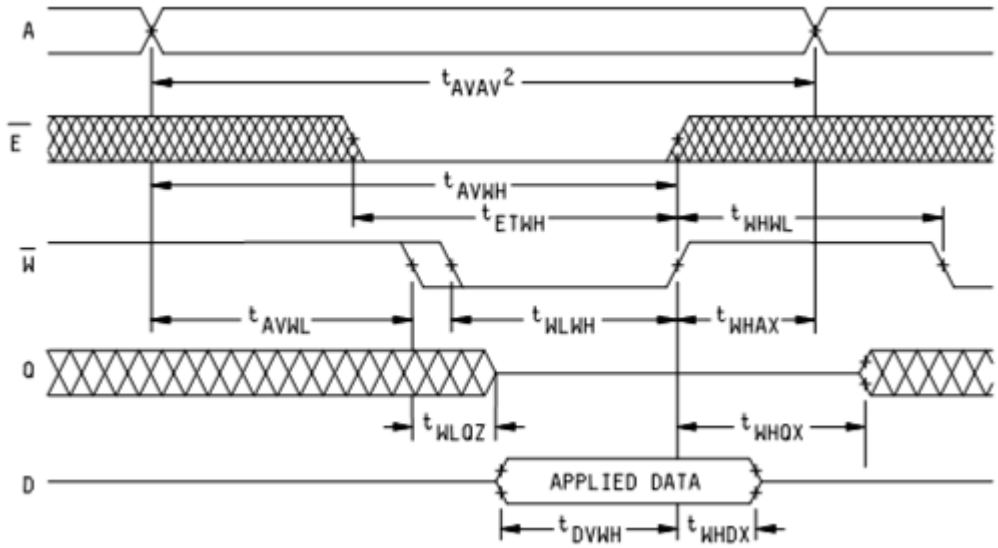
Data retention characteristics (pre-irradiation*) for devices 05 – 08
(**1** second data retention test)

Symbol	Parameter	Temp	Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention	---	2.5	---	V
I_{DDR} 1/	Data retention current (devices 05 and 06)	-40°C	---	10	mA
		-55°C	---	10	
		25°C	---	10	
		125°C	---	45	
I_{DDR} 1/	Data retention current (devices 07 and 08)	-40°C	---	16	mA
		-55°C	---	16	
		25°C	---	16	
		125°C	---	45	
t_{EFR} 1/	Chip select to data retention time	---	0	---	ns
t_R 1/	Operation recovery time	---	t_{AVAV}	---	ns

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 method 1019.
1/ $\overline{E}$ = V_{DD}, all other inputs = V_{DD} or V_{SS}.

FIGURE 5. Timing waveforms – Continued.

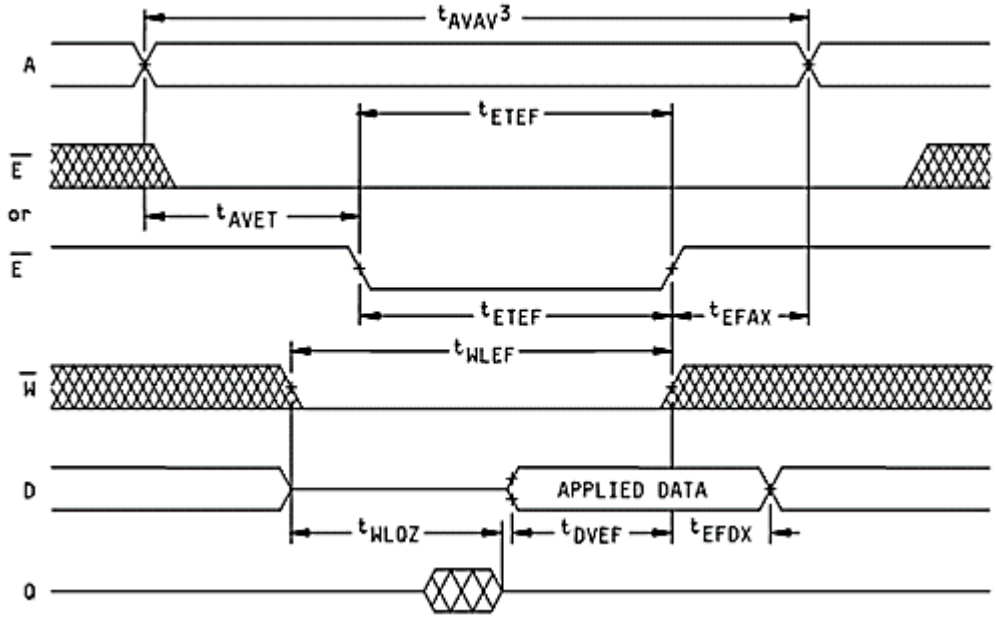
Write cycle 1: write enable-controlled access.



Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.
2. $\overline{G}$ high for t_{AVAV} cycle.

FIGURE 5. Timing waveforms – Continued.

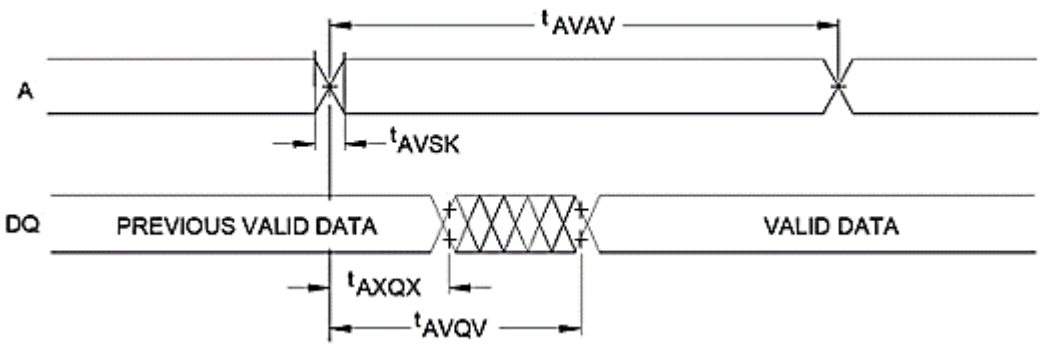
Write cycle 2: chip enable-controlled access.



Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.
2. Either $\overline{E}$ scenario can occur.
3. G high for t_{AVAV} cycle.

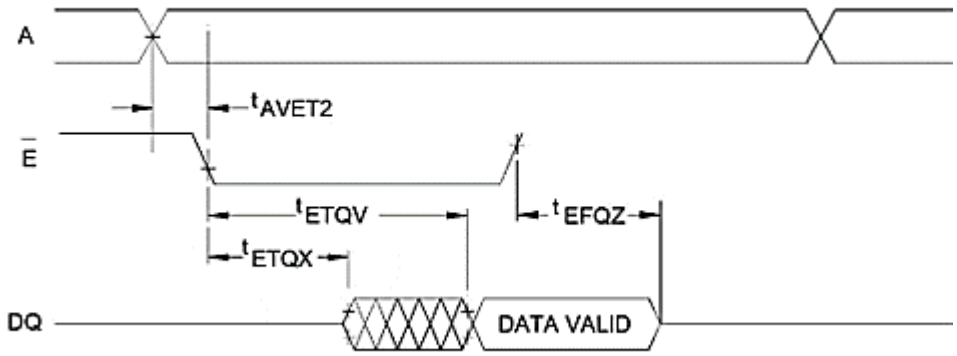
FIGURE 5. Timing waveforms – Continued.

SRAM read cycle 1: address access.



Note: $\overline{E}$ and $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

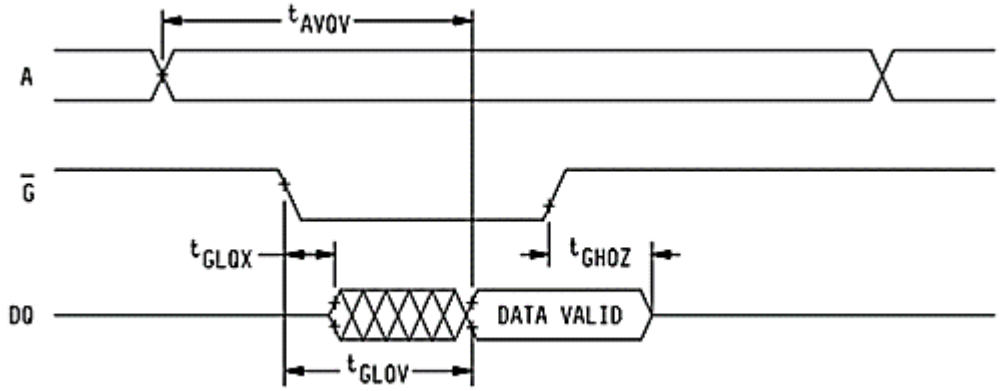
SRAM read cycle 2: chip enable-controlled access.



Note: $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 5. Timing waveforms – Continued.

SRAM read cycle 3: output enable-controlled access.



Note: $\overline{E} \le V_{IL}$(max) and $\overline{W} \ge V_{IH}$(min).

FIGURE 5. Timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T, and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.6 herein).

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes T, Q, and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535)		
		Device class Q	Device class V	Device class T
1	Interim electrical parameters (see 4.2)	- - -	1, 7, 9	As specified in QM plan
2	Static burn-in I and II (method 1015)	Not required	Required	
3	Same as line 1	- - -	1*, 7* Δ	
4	Dynamic burn-in (method 1015)	Required	Required	
5	Same as line 1	- - -	1*, 7* Δ	
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limited shall be required where specified, and the delta values (see Table IIB) shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{DD2}	±10% or 35 μA, whichever is greater 2/

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ If device is tested at or below 35 μA, no deltas are required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA. herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C +5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate upset testing. When specified in the purchase order or contract, dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V and T devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° < angle < 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq$ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring
the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm$10°C.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Occurrence of latch-up (SEL).

APPENDIX A
Appendix A forms a part of SMD 5962-00536
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

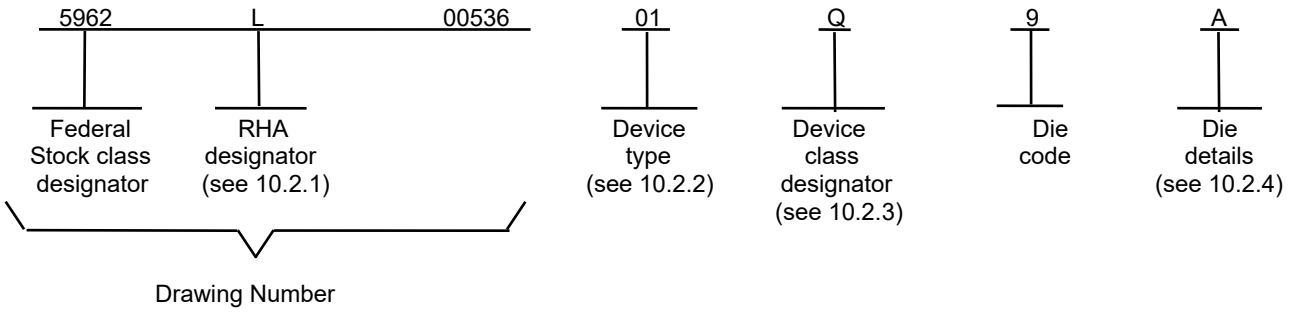
Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

APPENDIX B
APPENDIX B FORMS A PART OF SMD 5962-00536

B.1 SCOPE

B.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

B.1.2 PIN. The PIN shall be as shown in the following example:



B.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

B.1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	9Q512	512K X 8 bit rad-hard SRAM (MIL Temp)
02	9Q512	512K X 8 bit rad-hard SRAM (Extended Temp)
03	9Q512	512K X 8 bit rad-hard SRAM (MIL Temp)
04	9Q512	512K X 8 bit rad-hard SRAM (Extended Temp)
05	9Q512E	512K X 8-bit Radiation-hardened SRAM (MIL Temp)
06	9Q512E	512K X 8-bit Radiation-hardened SRAM (Extended Temp)

B.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

B.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

B.1.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad locations and related electrical functions, interface materials, and other assembly related information, for each product and variant supplied to this appendix.

B.1.2.5.1 Die Physical dimensions.

Die Type	Figure number
01, 02, 03, 04	B-1
05, 06	B-2

B.1.2.5.2 Die Bonding pad locations and Electrical functions.

Die Type	Figure number
01, 02 03, 04	B-1
05, 06	B-2

B.1.2.5.3 Interface Materials.

Die Type	Figure number
01, 02 03, 04	B-1
05, 06	B-2

B.1.2.5.4 Assembly related information.

Die Type	Figure number
01, 02 03, 04	B-1
05, 06	B-2

B.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

B.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

B.2 APPLICABLE DOCUMENTS

B.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

B.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS

B.3.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

B.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

B.3.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in B.1.2.5.1 and on figures B-1 and B-2.

B.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in B.1.2.5.2 and on figures B-1 and B-2.

B.3.2.3 Interface materials. The interface materials for the die shall be as specified in B.1.2.5.3 and on figures B-1 and B-2.

B.3.2.4 Assembly related information. The assembly related information shall be as specified in B.1.2.5.4 and figures B-1 and B-2.

B.3.2.5 Truth table. The truth table shall be as defined within paragraph 3.2.3 of the body of this document.

B.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.6 of the body of this document.

B.3.3 Electrical performance characteristics and post- irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

B.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

B.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in B.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

B.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see B.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

B.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

B.4. VERIFICATION

B.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

B.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a. Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 method 5007.

b. 100% wafer probe (see paragraph B.3.4).

c. 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 method 2010 or the alternate procedures allowed within MIL-STD-883 method 5004.

B.4.3 Conformance inspection.

B.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see B.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.

B.5. DIE CARRIER

B.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical, and electrostatic protection.

B.6. NOTES

B.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

B.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

B.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-HDBK-1331.

B.6.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see B.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

The following metallization diagram supplies the locations and electrical functions of the bonding pads. The internal metallization layout and alphanumeric information contained within this diagram may or may not represent the actual circuit defined by this SMD.

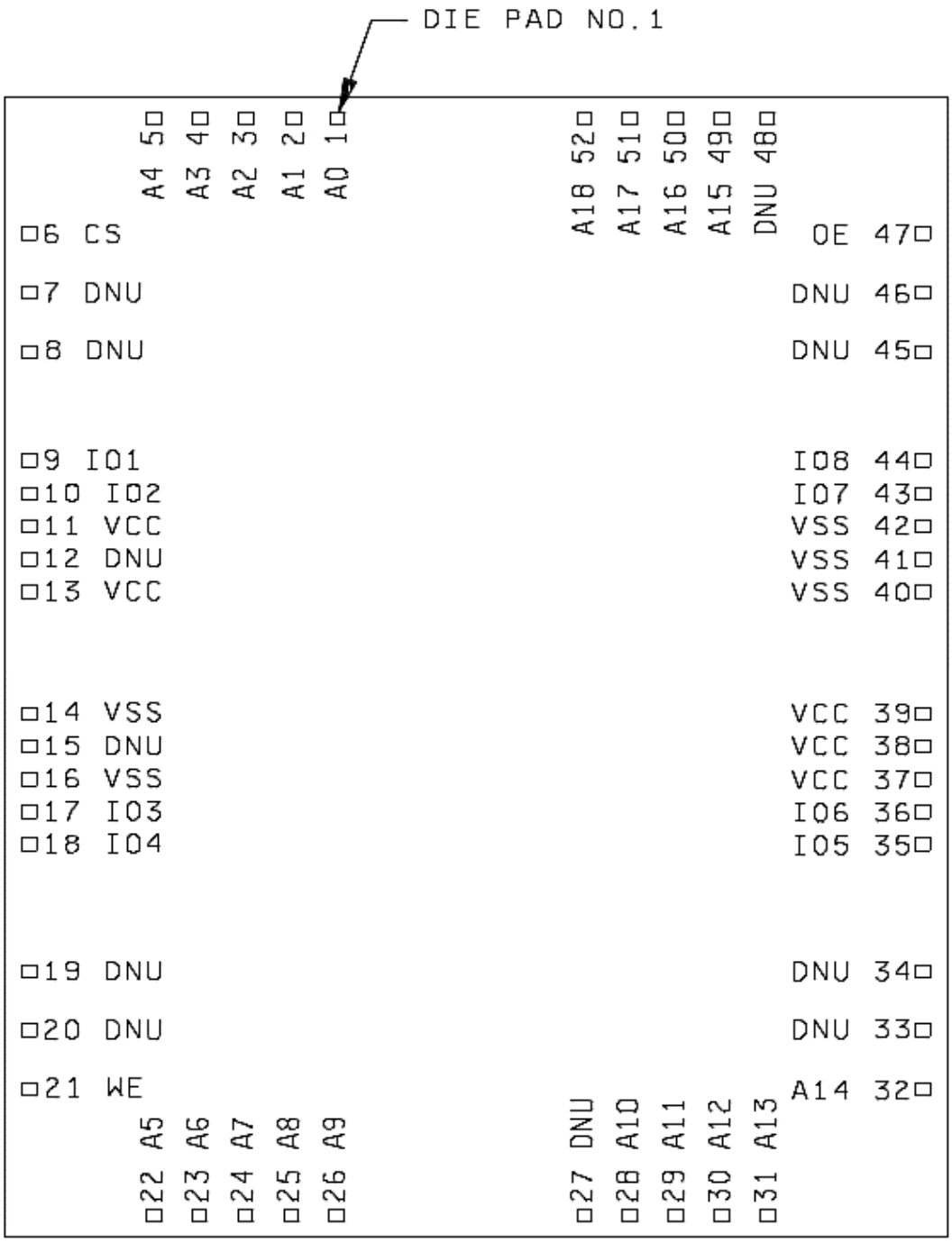


FIGURE B-1. Die bonding pad locations and electrical functions

o DIE PHYSICAL DIMENSIONS

Die Size:	191 x 287 mils.
Die Thickness:	12.6 mils.

o INTERFACE MATERIALS

Top metallization :	Cu	0.66 %
	Al	99.07 %
	Si	0.27 %

Backside Metallization	Silicon

Glassivation	
Type:	Nitride
Thickness	6,000 Å

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Ground/V_{SS}.
Special assembly instructions:	None.

FIGURE B-1. Die bonding pad locations and electrical functions – Continued.

The following metallization diagram supplies the locations and electrical functions of the bonding pads. The internal metallization layout and alphanumeric information contained within this diagram may or may not represent the actual circuit defined by this SMD.

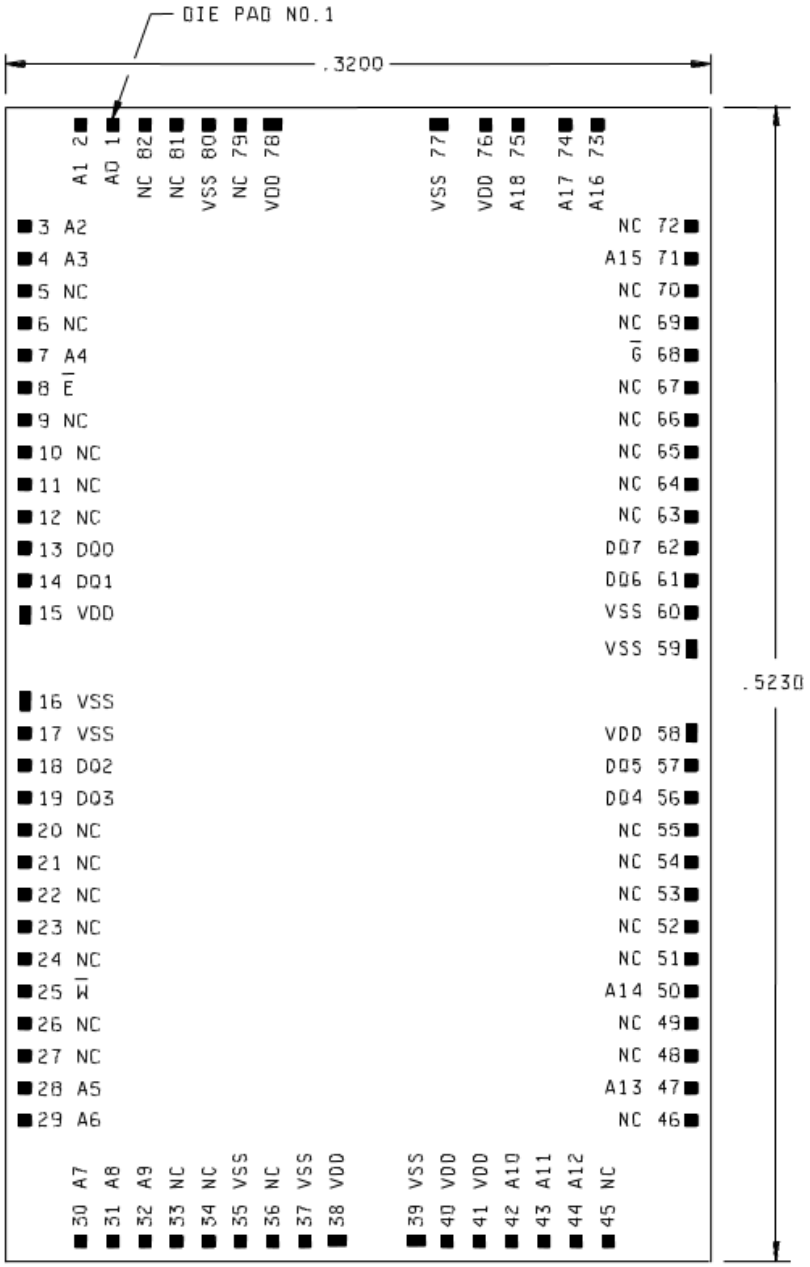


FIGURE B-2. Die bonding pad locations and electrical functions.

o DIE PHYSICAL DIMENSIONS

Die Size:	320 x 523 mils.
Die Thickness:	10.0 ±0.5 mils.

o INTERFACE MATERIALS

Top metallization :	Al	99.5%
	Cu	0.5%

Backside Metallization Silicon

Glassivation

Type:	SiO2 / Si3N4
Thickness	2600 Å < thickness < 10,000 Å

Substrate:
Epitaxial layer on single crystal silicon

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Ground/V_{SS}.
Special assembly instructions:	Do not bond anything to pads designated as NC

FIGURE B-2. Die bonding pad locations and electrical functions – Continued.

Die bonding pad locations (in microns) and electrical functions.

Die Pad	X center	Y center	Signal Name
1	-2852	6454	A0
2	-3252	6454	A1
3	-3874	5612	A2
4	-3874	5212	A3
5	-3874	4820	NC
6	-3874	4420	NC
7	-3874	4012	A4
8	-3874	3612	$\overline{E}$
9	-3874	3212	NC
10	-3874	2812	NC
11	-3874	2420	NC
12	-3874	2020	NC
13	-3874	1612	DQ0
14	-3874	1212	DQ1
15	-3874	819	VDD
16	-3874	-564	VSS
17	-3874	-820	VSS
18	-3874	-1228	DQ2
19	-3874	-1628	DQ3
20	-3874	-2020	NC
21	-3874	-2420	NC
22	-3874	-2828	NC
23	-3874	-3228	NC
24	-3874	-3628	NC
25	-3874	-4028	$\overline{W}$
26	-3874	-4428	NC
27	-3874	-4828	NC
28	-3874	-5228	A5
29	-3874	-5628	A6
30	-3447	-6454	A7
31	-3082	-6454	A8
32	-2717	-6454	A9
33	-2352	-6454	NC
34	-1987	-6454	NC
35	-1630	-6454	VSS
36	-1264	-6454	NC
37	-1010	-6454	VSS
38	-754	-6454	VDD
39	1309	-6454	VSS
40	1675	-6454	VDD
41	1930	-6454	VDD
42	2302	-6454	A10
43	2667	-6454	A11
44	3032	-6454	A12
45	3397	-6454	NC
46	3874	-5612	NC
47	3874	-5212	A13
48	3874	-4820	NC
49	3874	-4420	NC
50	3874	-4012	A14
51	3874	-3612	NC
52	3874	-3212	NC
53	3874	-2812	NC
54	3874	-2420	NC
55	3874	-2020	NC
56	3874	-1612	DQ4
57	3874	-1212	DQ5
58	3874	-819	VDD
59	3874	564	VSS
60	3874	820	VSS
61	3874	1228	DQ6
62	3874	1628	DQ7
63	3874	2020	NC
64	3874	2420	NC
65	3874	2828	NC
66	3874	3228	NC
67	3874	3628	NC
68	3874	4028	$\overline{G}$
69	3874	4420	NC
70	3874	4820	NC
71	3874	5228	A15
72	3874	5628	NC
73	3247	6454	A16
74	2837	6454	A17
75	2147	6454	A18
76	1747	6454	VDD
77	1065	6454	VSS
78	-845	6454	VDD
79	-1252	6454	NC
80	-1644	6454	VSS
81	-2052	6454	NC
82	-2452	6454	NC

FIGURE B-2. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-12-05

Approved sources of supply for SMD 5962-00536 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962D0053601Q9A	3/	UT9Q512_Q DIE
5962D0053601QUA	3/	UT9Q512-UCA
5962D0053601QXA	3/	UT9Q512-ICA
5962D0053601TUA	3/	UT9Q512-UCA
5962D0053601TXA	3/	UT9Q512-ICA
5962D0053608QYA	65342	UT81SRR512K8-5YCA
5962D0053608QYC	65342	UT81SRR512K8-5YCC
5962D0053608VYA	65342	UT81SRR512K8-5VCA
5962D0053608VYC	65342	UT81SRR512K8-5VCC
5962L0053601Q9A	3/	UT9Q512_Q DIE
5962L0053601QUA	3/	UT9Q512-UCA
5962L0053601QUC	3/	UT9Q512-UCC
5962L0053601QXA	3/	UT9Q512-ICA
5962L0053601QXC	3/	UT9Q512-ICC
5962L0053601T9A	3/	UT9Q512_T DIE
5962L0053601TXA	3/	UT9Q512-ICA
5962L0053601TXC	3/	UT9Q512-ICC
5962L0053601TUA	3/	UT9Q512-UCA
5962L0053601TUC	3/	UT9Q512-UCC
5962L0053602Q9A	3/	UT9Q512_Q DIE
5962L0053602QUA	3/	UT9Q512-UWA
5962L0053602QUC	3/	UT9Q512-UWC
5962L0053602QXA	3/	UT9Q512-IWA
5962L0053602QXC	3/	UT9Q512-IWC
5962L0053602T9A	3/	UT9Q512_T DIE
5962L0053602TUA	3/	UT9Q512-UWA
5962L0053602TUC	3/	UT9Q512-UWC
5962L0053602TXA	3/	UT9Q512-IWA
5962L0053602TXC	3/	UT9Q512-IWC
5962L0053603Q9A	3/	UT9Q512_Q DIE
5962L0053603QUA	3/	UT9Q512-UCA
5962L0053603QUC	3/	UT9Q512-UCC
5962L0053603QXA	3/	UT9Q512-ICA
5962L0053603QXC	3/	UT9Q512-ICC
5962L0053603T9A	3/	UT9Q512_T DIE
5962L0053603TUA	3/	UT9Q512-UCA
5962L0053603TUC	3/	UT9Q512-UCC
5962L0053603TXA	3/	UT9Q512-ICA
5962L0053603TXC	3/	UT9Q512-ICC
5962L0053604Q9A	3/	UT9Q512_Q DIE
5962L0053604QUA	3/	UT9Q512-UWA
5962L0053604QUC	3/	UT9Q512-UWC
5962L0053604QXA	3/	UT9Q512-IWA
5962L0053604QXC	3/	UT9Q512-IWC
5962L0053604T9A	3/	UT9Q512_T DIE
5962L0053604TUA	3/	UT9Q512-UWA
5962L0053604TUC	3/	UT9Q512-UWC

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L0053604TXA	3/	UT9Q512-IWA
5962L0053604TXC	3/	UT9Q512-IWC
5962L0053605Q9B	3/	UT9Q512E-Q DIE
5962L0053605QYA	3/	UT9Q512E-20YCA
5962L0053605QYC	3/	UT9Q512E-20YCC
5962L0053605V9B	3/	UT9Q512E-V DIE
5962L0053605VYA	3/	UT9Q512E-20YCA
5962L0053605VYC	3/	UT9Q512E-20YCC
5962L0053606Q9B	3/	UT9Q512E-Q DIE
5962L0053606QYA	3/	UT9Q512E-20YWA
5962L0053606QYC	3/	UT9Q512E-20YWC
5962L0053606V9B	3/	UT9Q512E-V DIE
5962L0053606VYA	3/	UT9Q512E-20YWA
5962L0053606VYC	3/	UT9Q512E-20YWC
5962R0053607QYA	65342	UT9Q512E-20YCA
5962R0053607QYC	65342	UT9Q512E-20YCC
5962R0053607VYA	65342	UT9Q512E-20VCA
5962R0053607VYC	65342	UT9Q512E-20VCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
65342	CAES Colorado Springs, LLC 4350 Centennial Blvd. Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.