REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to t_{T1}, T_{DP}, V_{PAUX}, t_{T2}, T_{DA} tests and switch footnotes 2 and 3 as specified under table I. - ro	00-08-21	R. Monnin
B	Make changes to SEP as specified under 1.5 and I_{CCS}, t_{T1}, t_{T2} tests as specified in table I. – ro	00-09-20	R. Monnin
C	Make correction to PWR pin description as specified in figure 1. - ro	01-12-14	R. Monnin
D	Make changes to UV- in table I, added footnote to 1.5 and table I. - gt	03-06-19	R. Monnin
E	Make changes to the conditions column for the t_{T2} and T_{DA} tests as specified under Table I. Add figure 3. - ro	08-07-30	R. Heber
F	Add device type 02. - drw	13-05-03	Charles F. Saffle
G	Add device type 03. Add paragraph 2.2, 6.7 and Table IB for SEP information. Delete Dose rate latch-up under paragraph 1.5 and paragraph 4.4.4.3. - ro	16-06-21	Charles F. Saffle

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G										
SHEET	15	16	17	18	19	20	21	22	23	24										
REV STATUS				REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rick Officer

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
00-07-26

REVISION LEVEL
G

MICROCIRCUIT, DIGITAL-LINEAR, COMPLEMENTARY SWITCH FET DRIVER, MONOLITHIC SILICON

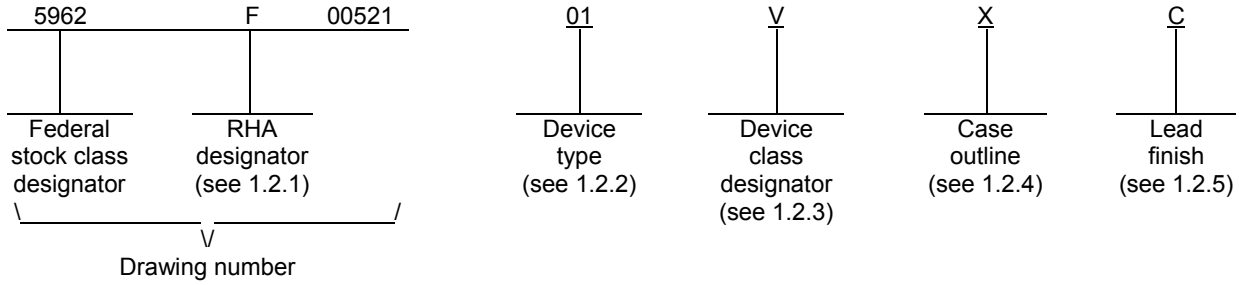
SIZE	CAGE CODE	
A	**67268**	**5962-00521**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	IS-1715ARH	Radiation hardened, complementary switch field effect transistor (FET) driver
02	UC1715-SP	Complementary switch FET drivers
03	IS-1715AEH	Radiation hardened, complementary switch field effect transistor (FET) driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) device types 01 and 03 ..... 10 V dc to 20 V dc
Supply voltage (V_{CC}) device type 02 ..... 20 V dc
DC input voltage range (V_{IN}):
  Device types 01 and 03 ..... 0 V to V_{CC}
  Device type 02 ..... -0.3 V to 20 V
Output current, high (I_{OH}) device type 02:
  Power driver continuous ..... -100 mA
  Power driver peak ..... -1 A
  Auxiliary driver continuous ..... -100 mA
  Auxiliary driver peak ..... -500 mA
Output current, low (I_{OL}) device type 02:
  Power driver continuous ..... 100 mA
  Power driver peak ..... 2 A
  Auxiliary driver continuous ..... 100 mA
  Auxiliary driver peak ..... 1 A
Junction temperature (T_J):
  Device types 01 and 03 ..... +175°C
  Device type 02 ..... +150°C
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +265°C
Thermal resistance, junction-to-case (θ_{JC}):
  Device types 01 and 03 ..... 18°C/W
  Device type 02 ..... 8.25°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
  Device types 01 and 03 ..... 90°C/W
  Device type 02 ..... 72.9°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):
  Device types 01 and 03 ..... 10 V dc to 18 V dc
  Device type 02 ..... 7 V dc to 18 V dc
Ambient operating temperature range (T_A) device types 01 and 03 ..... -55°C to +125°C
Operating temperature range ($T_A = T_J$) device type 02 ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

1.5 Radiation features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device type 01:
Device classes Q, or V ..... 300 krads(Si) 2/
Device class T ..... 100 krads(Si) 2/
Device type 03: ..... 300 krads(Si) 3/
Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):
Device type 03 ..... 50 krads(Si) 3/
Single event phenomena (SEP):
No SEL occurs at effective linear energy transfer (LET) for device type 01 and 03: ..... ≤ 181 MeV·cm^2/mg 4/
No SEB occurs at linear energy transfer (LET) for device type 01 and 03 ..... ≤ 90 MeV·cm^2/mg 4/
Single evet transients observed at LET (for device type 01 and 03)..... 90 MeV·cm^2/mg 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for class Q or V and 100 krads(Si) for class T.
3/ Device types 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).
4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Timing diagram. The timing diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ Device types 01 and 03: $-55°C \le T_A \le +125°C$ V_{CC} = 10 V to 18 V, ENBL ≥ 3 V; Device type 02: $-55°C \le T_A \le +125°C$ ($T_A = T_J$), V_{CC} = 15 V, ENBL ≥ 2 V, $R_T1 = R_T2$ = 100 kΩ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
OVERALL section								
Operating voltage range	V_{CC}			1, 2, 3	01, 03	10	18	V
			M,D,P,L,R,F 2/	1		10	18	
				1, 2, 3	02	7	18	
Input current, nominal	I_{CC}			1, 2, 3	01, 03	1.0	6.0	mA
			M,D,P,L,R,F 2/	1		1.0	6.0	
		ENBL = 3 V		1, 2, 3	02		25	
Input current, sleep mode	I_{CCS}	ENBL = 0.8 V		1, 2, 3	01, 03	300	900	μA
			M,D,P,L,R,F 2/	1		300	900	
				1, 2, 3	02		300	
Under voltage, rising threshold	UV+			1, 2, 3	01, 03	8.5	9.5	V
			M,D,P,L,R,F 2/	1		8.5	9.5	
Under voltage, falling threshold	UV-			1, 2, 3	01, 03	7.7	8.8	V
			M,D,P,L,R,F 2/	1		7.7	8.8	
Under voltage delta	UVD			1, 2, 3	01, 03	0	2.0	V
			M,D,P,L,R,F 2/	1		0	2.0	
Power driver (PWR) section								
Pre turn-on PWR output, low	V_{PPWR}	V_{CC} = 0 V, ENBL ≤ 0.8 V, I_{OUT} = 10 mA		1, 2, 3	All		2.0	V
			M,D,P,L,R,F 2/	1	01, 03		2.0	
PWR pin output low, saturation	V_{PWR}	INPUT = 0.8 V, I_{OUT} = 40 mA		1, 2, 3	All		1.0	V
			M,D,P,L,R,F 2/	1	01, 03		1.0	
		INPUT = 0.8 V, I_{OUT} = 100 mA		1, 2, 3	All		1.5	
			M,D,P,L,R,F 2/	1	01, 03		1.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ Device types 01 and 03: $-55°C \le T_A \le +125°C$ V_{CC} = 10 V to 18 V, ENBL ≥ 3 V; Device type 02: $-55°C \le T_A \le +125°C$ ($T_A = T_J$), V_{CC} = 15 V, ENBL ≥ 2 V, $R_T1 = R_T2$ = 100 kΩ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power driver (PWR) section – continued.							
PWR pin output high, saturation	V_{CC} - V_{PWR}	INPUT = 3.0 V, I_{OUT} = -40 mA	1, 2, 3	01, 03		1.0	V
		M,D,P,L,R,F 2/	1			1.0	
			1, 2, 3	02		3	
		INPUT = 3.0 V, I_{OUT} = -100 mA	1, 2, 3	01, 03		1.5	
		M,D,P,L,R,F 2/	1			1.5	
			1, 2, 3	02		3	
Rise time	T_{RP}	C_L = 2200 pF	9, 10, 11	01, 03	15	50	ns
		M,D,P,L,R,F 2/	9		15	50	
			9, 10, 11	02		60	
Fall time	T_{FP}	C_L = 2200 pF	9, 10, 11	01, 03	15	50	ns
		M,D,P,L,R,F 2/	9		15	50	
			9, 10, 11	02		60	
T1 input pin delay, AUX to PWR	t_{T1}	INPUT rising edge, 3/ 4/ R_{T1} = 10 kΩ	9, 10, 11	All	45	200	ns
		M,D,P,L,R,F 2/	9	01, 03	45	200	
		INPUT rising edge, 3/ 4/ R_{T1} = 100 kΩ	9, 10, 11	All	250	1300	
		M,D,P,L,R,F 2/	9	01, 03	250	1300	
PWR propagation delay	T_{DP}	INPUT falling edge at 5/ 50% points	9, 10, 11	01, 03	50	300	ns
		M,D,P,L,R,F 2/	9		50	300	
			9, 10, 11	02		300	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ Device types 01 and 03: $-55°C \le T_A \le +125°C$ V_{CC} = 10 V to 18 V, ENBL ≥ 3 V; Device type 02: $-55°C \le T_A \le +125°C$ ($T_A = T_J$), V_{CC} = 15 V, ENBL ≥ 2 V, $R_T1 = R_T2$ = 100 kΩ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Auxiliary (AUX) section							
AUX pre turn-on AUX output, low	V_{PAUX}	V_{CC} = 0 V, ENBL ≤ 0.8 V, I_{OUT} = 10 mA	1, 2, 3	All		2.0	V
		M,D,P,L,R,F 2/	1	01, 03		2.0	
AUX pin output low, saturation	V_{AUX}	INPUT = 3.0 V, I_{OUT} = 40 mA	1, 2, 3	All		1.0	V
		M,D,P,L,R,F 2/	1	01, 03		1.0	
		INPUT = 3.0 V, I_{OUT} = 100 mA	1, 2, 3	All		1.5	
		M,D,P,L,R,F 2/	1	01, 03		1.5	
AUX pin output high, saturation	V_{CC} - V_{AUX}	INPUT = 0.8 V, I_{OUT} = -40 mA	1, 2, 3	01, 03		1.0	V
		M,D,P,L,R,F 2/	1			1.0	
			1, 2, 3	02		3	
		INPUT = 0.8 V, I_{OUT} = -100 mA	1, 2, 3	01, 03		1.5	
		M,D,P,L,R,F 2/	1			1.5	
			1, 2, 3	02		3	
Rise time	T_{RP}	C_L = 2200 pF	9, 10, 11	01, 03	15	50	ns
		M,D,P,L,R,F 2/	9		15	50	
			9, 10, 11	02		60	
Fall time	T_{FP}	C_L = 2200 pF	9, 10, 11	01, 03	15	50	ns
		M,D,P,L,R,F 2/	9		15	50	
			9, 10, 11	02		60	
AUX propagation delay	T_{DA}	INPUT rising edge at 5/	9, 10, 11	01, 03	50	185	ns
		50% points M,D,P,L,R,F 2/	9		50	185	
			9, 10, 11	02		185	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ Device types 01 and 03: $-55°C \le T_A \le +125°C$ V_{CC} = 10 V to 18 V, ENBL ≥ 3 V; Device type 02: $-55°C \le T_A \le +125°C$ ($T_A = T_J$), V_{CC} = 15 V, ENBL ≥ 2 V, $R_T1 = R_T2$ = 100 kΩ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Auxiliary (AUX) section – continued							
T2 input pin delay, PWR to AUX	t_{T2}	INPUT falling edge, 3/ 4/	9, 10, 11	01, 03	50	130	ns
		R_{T2} = 10 kΩ M,D,P,L,R,F 2/	9		50	130	
			9, 10, 11	02	45	130	
		INPUT falling edge, 3/ 4/ R_{T2} = 100 kΩ	9, 10, 11	All	200	700	
		M,D,P,L,R,F 2/	9	01, 03	200	700	
ENABLE section							
Input threshold voltage	V_{IT}		1, 2, 3	All		2.8	V
		M,D,P,L,R,F 2/	1	01, 03		2.8	
Input current high	I_{IH}	ENABLE pin = 15 V	1, 2, 3	All	-10	10	μA
		M,D,P,L,R,F 2/	1	01, 03	-10	10	
Input current low	I_{IL}	ENABLE pin = 0 V	1, 2, 3	All	-15	15	μA
		M,D,P,L,R,F 2/	1	01, 03	-15	15	
T1 input section							
Current limit	T_{1CL}	T1 input = 0 V	1,2,3	01, 03	-5.5	-1.6	mA
		M,D,P,L,R,F 2/	1		-5.5	-1.6	
			1, 2, 3	02	-2.0	-0.5	
Nominal voltage at T1 pin	T_{1NV}		1, 2, 3	All	2.7	3.3	V
		M,D,P,L,R,F 2/	1	01, 03	2.7	3.3	
Minimum T1 pin delay	T_{1DM}	T1 pin = 2.5 V 5/	9, 10, 11	01, 03	25	120	ns
		M,D,P,L,R,F 2/	9		25	120	
			9, 10, 11	02		80	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ Device types 01 and 03: $-55°C \le T_A \le +125°C$ V_{CC} = 10 V to 18 V, ENBL ≥ 3 V; Device type 02: $-55°C \le T_A \le +125°C$ ($T_A = T_J$), V_{CC} = 15 V, ENBL ≥ 2 V, $R_T1 = R_T2$ = 100 kΩ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
T2 input section								
Current limit	T_{2CL}	T2 input = 0 V		1, 2, 3	01, 03	-5.5	-2.1	mA
			M,D,P,L,R,F 2/	1		-5.5	-2.1	
				1, 2, 3	02	-2.0	-0.5	
Nominal voltage at T2 pin	T_{2NV}			1, 2,3	All	2.7	3.3	V
			M,D,P,L,R,F 2/	1	01, 03	2.7	3.3	
Minimum T2 pin delay	T_{2DM}	T2 pin = 2.5 V 4/		9, 10, 11	01, 03	20	80	ns
			M,D,P,L,R,F 2/	9		20	80	
				9, 10, 11	02		80	
INPUT section								
Input threshold voltage	V_{IT}			1, 2, 3	All		2.8	V
			M,D,P,L,R,F 2/	1	01, 03		2.8	
Input current high	I_{IH}	INPUT = 15 V		1,2,3	All	-10	10	μA
			M,D,P,L,R,F 2/	1	01, 03	-10	10	
Input current low	I_{IL}	INPUT = 0 V		1,2,3	All	-20	20	μA
			M,D,P,L,R,F 2/	1	01, 03	-20	20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

1/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation for device class Q or V and levels M, D, P, L, and R of irradiation for device class T. However, device type 01 is only tested at the "F" level for device class Q or V and the "R" level for device class T in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).
RHA device type 03 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and irradiation of M, D, P, and L levels for condition D. However, device type 03 is only tested at the "F" level in accordance with MIL-STD-883, method 1019, condition A, and tested at the "L" level in condition D (see 1.5 herein).
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

3/ T1 and T2 delay is defined as the time between the 50% transition point of AUX (PWR) and the 50% transition point of PWR (AUX) with no capacitive load on either output.

4/ For device type 02, the parameter is guaranteed to the limit specified by characterization, but not production tested.

5/ Propagation delays are measured from the 50% point of the input signal to the 50% point of the output signal's transition with no load on outputs.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET)
01 and 03	No SEL	125°C	Effective LET ≤ 181 MeV-cm^2/mg
	No SEB	125°C	LET ≤ 90 MeV-cm^2/mg
	SET observed	25°C	LET= 90 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Device types 01 and 03 have been tested for SEE at Texas A&M University heavy ion facility with heavy ion beam gold (Au), fluence= 1X10^7 ions/cm^2 and flux =1 x 10^5 ions/cm^2/s. No single event burnout (SEB) and single-event latchup (SEL) was observed corresponding effective LET of 181 MeV·cm^2/mg for SEL and LET of 90 MeV·cm^2/mg for SEB. For more information on SEP test results, customers are requested to contact the manufacturer.

Device types	01 and 03	02
Case outline	X	F
Terminal number	Terminal symbol	
1	NC	NC
2	V_{CC}	V_{CC}
3	PWR	PWR
4	GND	GND
5	GND	GND
6	AUX	AUX
7	NC	NC
8	NC	NC
9	NC	NC
10	V_{CC}	NC
11	T2	T2
12	GND	NC
13	GND	NC
14	INPUT	INPUT
15	T1	T1
16	ENABLE	ENABLE

NC = No connect

FIGURE 1. Terminal connections.

Symbol	Description
NC	No connection
V_{CC}	Chip positive supply (10 V – 20 V device types 01 and 03), (7 V – 20 V device type 02)
PWR	Output. PWR switches immediately (neglecting propagation delay) at INPUT's falling edge but is delayed after the rising edge by the value of the resistance on T1. PWR is capable of sinking and sourcing (3.0 A device type 01), (2.0 A device type 02) of peak gate drive current. During sleep mode, PWR is active low.
GND	Chip negative supply.
AUX	Output. AUX switches immediately (neglecting propagation delay) at INPUT's rising edge but is delayed after the falling edge before switching by the value of the resistance on T2. AUX is capable is sinking and sourcing (3.0 A device types 01 and 03), (sinking 1.0 A, sourcing 0.5 A device type 02) of peak gate drive current. During sleep mode, AUX is active low.
V_{CC}	Chip supply (device types 01 and 03, 10 V – 20 V), (device type 02, 7 V – 20 V)
T2	Input. A resistor to ground programs the time delay between PWR switch turn-off and AUX turn-on.
INPUT	Input. INPUT switches at TTL logic levels but the allowable range is from 0 V to V_{CC} allowing direct connection to most common IN PWR controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.
T1	Input. A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.
ENABLE	Input. The ENABLE input switches at TTL logic levels, but the allowable range is from 0 to V_{CC}. The ENABLE input will place the device into sleep mode when it is a logic low. The current into V_{CC} during the sleep mode is typically 500 μA.

FIGURE 1. Terminal connections – continued.

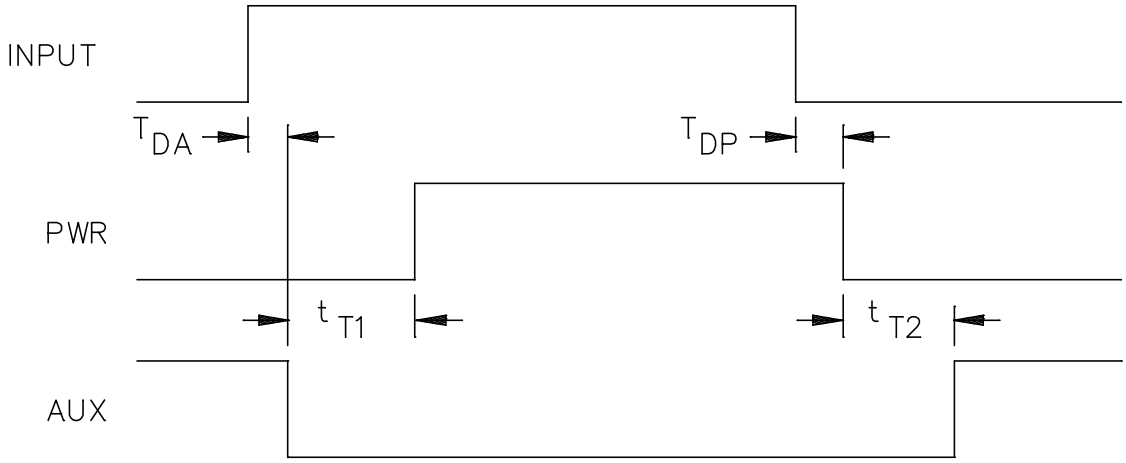


FIGURE 3. Timing diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.2 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1, 9	1, 9	As specified in QM plan
Final electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11 1/	1, 2, 3, 9, 10, 11 2/, 3/	As specified in QM plan
Group A test requirements (see 4.4)	1, 2, 3 ,9, 10, 11	1, 2, 3, 9, 10, 11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11 3/	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1 ,9	1, 9	As specified in QM plan

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 9, and deltas.
3/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Device types	Delta limits
Input current, nominal	I_{CC}	01, 03	±100 μA
		02	±750 μA
Input current, low	I_{IL}	All	±1.0 μA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01 and 03. In addition, for device type 03, a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract SEP testing shall be required on class T and V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b Occurrence of latchup (SEL).

c Occurrence of single event burn-out (SEB).

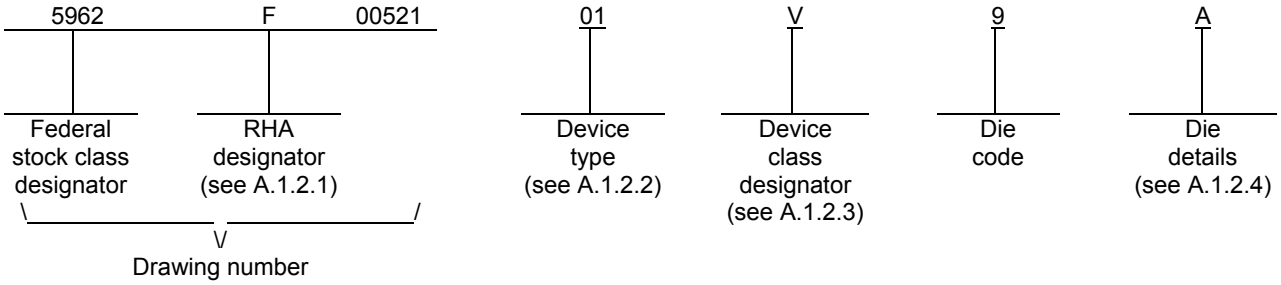
d Observance of single event transient (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-00521

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	IS-1715ARH	Radiation hardened complementary switch field effect transistor (FET) driver
03	IS-1715AEH	Radiation hardened complementary switch field effect transistor (FET) driver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, 4.4.4.3, 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

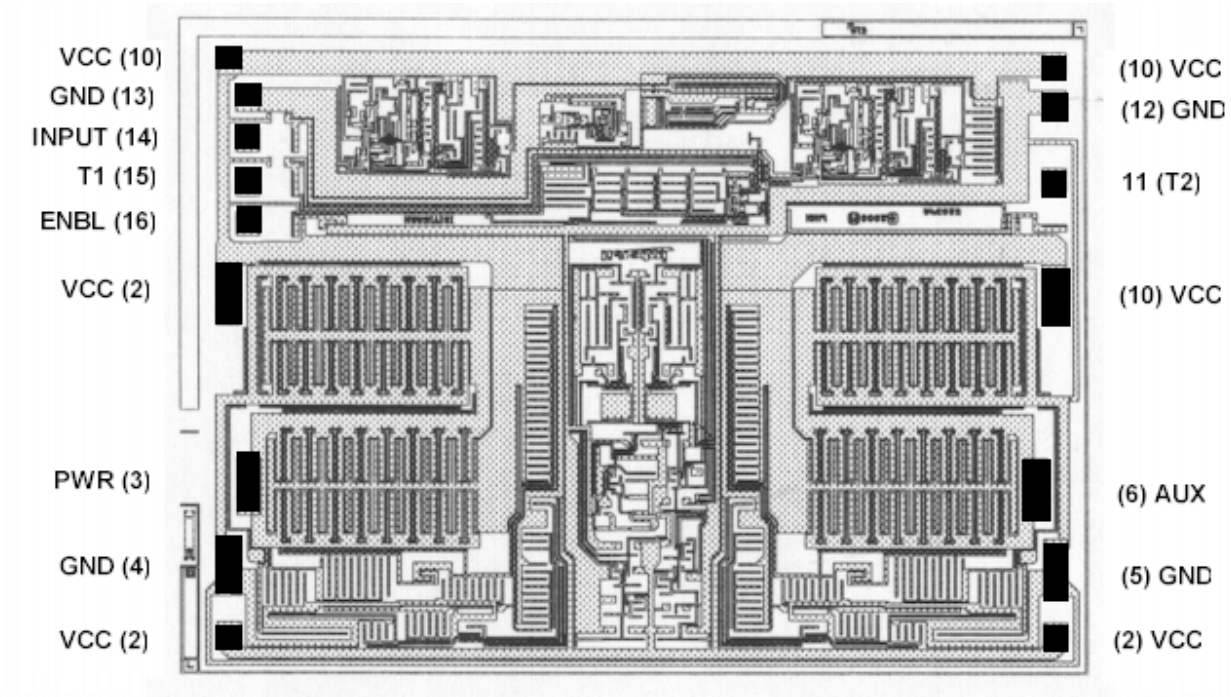
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 129 mils x 174 mils
Die thickness: 19 mils ±1 mil

Interface materials.
Top metallization: AL, Si, Cu 16.9 kÅ ±2 kÅ
Backside metallization: NONE (Silicon)

Glassivation.
Type: Phosphorus silicon glass (PSG)
Thickness: 8.0 kÅ ±1.0 kÅ

Substrate: DI (dielectric isolation)

Assembly related information.
Substrate potential: Unbiased (DI)
Special assembly instructions: (1.) All double size pads are double bonded.
(2.) All pin 2 and pin 10 V_{CC} pads are bonded to V_{CC} for power and noise considerations. (These are lead-frame connected in packaged devices.)

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-06-21

Approved sources of supply for SMD 5962-00521 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0052101QXC	34371	IS9-1715ARH-8
5962R0052101TXC	34371	IS9-1715ARH-T
5962F0052101VXC	34371	IS9-1715ARH-Q
5962F0052101V9A	34371	IS0-1715ARH-Q
5962-0052102VFA	01295	UC1715W-SP
5962F0052103VXC	34371	IS9-1715AEH-Q
5962F0052103V9A	34371	IS0-1715AEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243