

REVISIONS

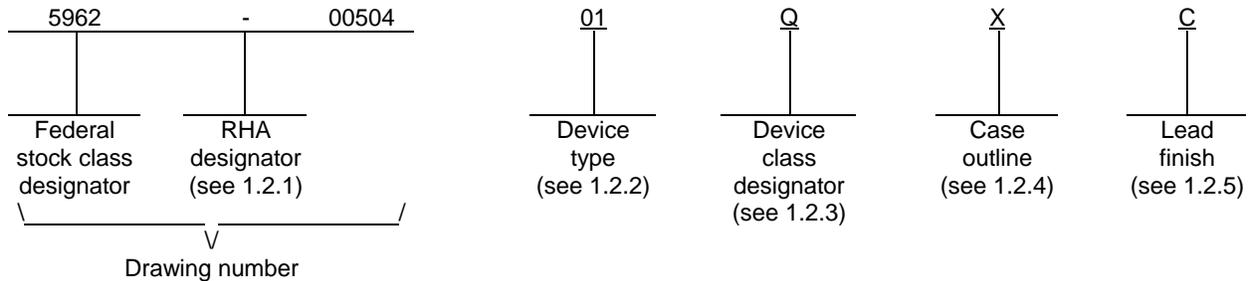
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redraw. For case outline X, change A3 dimension. - drw	08-11-19	Robert M. Heber

REV																				
SHEET																				
REV	A	A	A																	
SHEET	15	16	17																	
REV STATUS OF SHEETS	REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A	PREPARED BY Dan Wonnell					<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p>														
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Raymond Monnin																			
	APPROVED BY Raymond Monnin					<p align="center">MICROCIRCUIT, DIGITAL-LINEAR, ANALOG-TO- DIGITAL CONVERTER, 8-BIT, 1 GSPS, MONOLITHIC SILICON</p>														
	DRAWING APPROVAL DATE 01-11-15																			
	REVISION LEVEL A					SIZE A	CAGE CODE 67268	5962-00504												
														SHEET 1 OF 17						

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	8388B	A/D converter, 8-bit, wide bandwidth, 1 giga samples per second sampling rate

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	68	Quad flat pack with gull-wing leads, enhanced θ_{JC}
Y	See figure 1	68	Quad flat pack with gull-wing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/, 2/, 3/

Positive supply voltage (V_{CC})	GND to 6 V dc
Digital negative supply voltage (DV_{EE})	GND to -5.7 V dc
Digital positive supply voltage (V_{PLUSD})	GND -0.3 V to 2.8 V dc
Negative supply voltage (V_{EE})	GND to -6 V dc
Maximum difference between negative supply voltages (DV_{EE} to V_{EE})	0.3 V dc
Analog input voltages (V_{IN} or V_{INB})	-1 V to 1 V dc
Maximum difference between analog inputs ($V_{IN} - V_{INB}$)	-2 V to 2 V dc
Digital input voltage (V_D):	
GORB	-0.3 V to $V_{CC} + 0.3$ V dc
DRRB	$V_{EE} - 0.3$ V to 0.9 V dc
Digital output voltage (V_O)	$V_{PLUSD} - 3$ V to $V_{PLUSD} - 0.5$ V dc
Clock input voltage (V_{CLK} or V_{CLKB})	-3 V to 1.5 V dc
Maximum difference between clock inputs ($V_{CLK} - V_{CLKB}$)	-2 V to 2 V dc
Junction temperature (T_J)	+135°C
Storage temperature (T_{STG})	-65°C to +150°C
Lead temperature (T_{LEAD})	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	1.56°C/W
Case outline Y	4.75°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC})	4.75 V to 5.25 V dc; 5 V dc typical
Positive digital supply voltage (V_{PLUSD}):	
ECL output compatibility	GND
LVDS output compatibility	+1.4 V to +2.6 V dc; +2.4 V dc typical
Negative supply voltage range (V_{EE} , V_{DVEE})	-5.25 V to -4.75 V dc; -5 V dc typical
Differential analog input voltage (full scale, 50Ω differential or single-ended):	
V_{IN} , V_{INB}	±113 mV to ±137 mV dc; ±125 mV dc typical
$V_{IN} - V_{INB}$	450 mV _{PP} to 550 mV _{PP} ; 500 mV _{PP} typical
Clock input power level (50Ω single-ended clock input):	
P_{CLK} , P_{CLKB}	3 dBm to 10 dBm max.; 4 dBm typical
Operating temperature range	-55°C < T_C , T_J ≤ +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Absolute maximum ratings are limited values, to be applied individually, while other parameters are within specified operating conditions.
- 3/ The use of thermal heatsink is mandatory.

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DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55 (-0/+5)°C < T _C ; T _J < +125 (-5/+0)°C V _{EE} = DV _{EE} = -5 V, V _{CC} = +5 V, V _{IN} - V _{INB} = 500 mVpp full scale differential input, digital outputs 75 or 50 Ω differentially terminated. unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Full scale input voltage range	V _{IN}	Differential mode	1, 2, 3	01	-125	125	mV
		Single-ended input option			-250	250	
	V _{INB}	0 V common mode voltage			-125	125	
Analog input capacitance	C _{IN}		4 <u>1/</u>	01		3.5	pF
Input bias current	I _{IN}		1 <u>1/</u>	01		20	μA
Input resistance	R _{IN}		1 <u>1/</u>	01	0.5		MΩ
Full power input bandwidth	FPBW		4 <u>1/</u>	01	1.3		GHz
Small single input bandwidth	SSBW		4 <u>1/</u>	01	1.5		GHz
Logic "0" input voltage	V _{IL}		1, 2, 3	01		-1.5	V
Logic "1" input voltage	V _{IH}		1, 2, 3	01	-1.1		V
Logic "0" input current	I _{IL}		1, 2, 3	01		50	μA
Logic "1" input current	I _{IH}		1, 2, 3	01		50	μA
Clock input power level	P _{CLK}		4 <u>1/</u>	01	-2	10	dBm
Clock input capacitance	C _{CLK}		4 <u>1/</u>			3.5	pF
Differential output voltage swings <u>2/</u> , <u>3/</u>	V _{DIFF}	75Ω open transmission lines, V _{PLUSD} = 0 V	1, 2, 3	01	1.50		V
		75Ω differentially terminated V _{PLUSD} = 0 V			0.70		
		50Ω differentially terminated V _{PLUSD} = 0 V			0.54		
Logic "0" output voltage <u>2/</u> , <u>3/</u>	V _{OL}	75Ω open transmission lines, V _{PLUSD} = 0 V	1	01		-1.54	V
		75Ω differentially terminated V _{PLUSD} = 0 V				-1.34	
		50Ω differentially terminated V _{PLUSD} = 0 V				-1.32	
Logic "1" output voltage <u>2/</u> , <u>3/</u>	V _{OH}	75Ω open transmission lines, V _{PLUSD} = 0 V	1	01	-0.88		V
		75Ω differentially terminated V _{PLUSD} = 0 V				-1.07	
		50Ω differentially terminated V _{PLUSD} = 0 V				-1.16	
Output level drift <u>2/</u> , <u>3/</u>	V _{OD}		1, 2, 3	01		1.6	mV/°C

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55 (-0/+5)°C < T _C ; T _J < +125 (-5/+0)°C V _{EE} = DV _{EE} = -5 V, V _{CC} = +5 V, V _{IN} - V _{INB} = 500 mVpp full scale differential input, digital outputs 75 or 50 Ω differentially terminated. unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential non linearity	DNL	<u>2/</u> , <u>4/</u>	1	01	-0.5	0.6	LSB
			2, 3		-0.6	0.7	
Integral non linearity	INL	<u>2/</u> , <u>4/</u>	1	01	-1.0	1.0	LSB
			2, 3		-1.2	1.2	
Gain error	A _E	<u>2/</u>	1	01	-10	10	%FS
			2, 3		-11	11	
Input offset voltage	V _{INOFF}	<u>2/</u>	1	01	-26	26	mV
			2, 3		-30	30	
Gain error drift	TC _A	<u>2/</u>	1 <u>1/</u>	01	100	150	ppm/°C
Offset error drift	TC _{OFF}	<u>2/</u>	1 <u>1/</u>	01	40	60	ppm/°C
Positive supply voltage, analog	V _{CC}		1, 2, 3	01	4.75	5.25	V
Positive supply voltage, digital	V _{PLUSD}		1, 2, 3	01	1.4	2.6	V
Positive supply current, analog	I _{CC}		1, 2, 3	01		445	mA
Positive supply current, digital	I _{PLUSD}		1, 2, 3	01		145	mA
Negative supply voltage	V _{EE}		1, 2, 3	01	-5.25	-4.75	V
Negative supply current, analog	AI _{EE}		1, 2, 3	01		200	mA
Negative supply current, digital	DI _{EE}		1, 2, 3	01		180	mA
Power dissipation	P _D		1, 2, 3	01		4.3	W
Power supply rejection ratio	PSRR		1 <u>1/</u>	01		40	mV/V
Bit error rate	BER	<u>5/</u>	9 <u>1/</u>	01		1E-12	error/ sample
ADC settling time	t _S	V _{IN} - V _{INB} = 400 mV _{PP}	9 <u>1/</u>	01	0.5	1	ns
Overvoltage recovery time	t _{OR}		9 <u>1/</u>	01	0.5	1	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55 (-0/+5)°C < T _C ; T _J < +125 (-5/+0)°C V _{EE} = DV _{EE} = -5 V, V _{CC} = +5 V, V _{IN} - V _{INB} = 500 mVpp full scale differential input, digital outputs 75 or 50 Ω differentially terminated. unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Signal to noise and distortion ratio <u>2/</u>	SINAD	F _S = 1 GSPS, F _{IN} = 20 MHz	4, 5, 6 <u>1/</u>	01	42		dB
		F _S = 1 GSPS, F _{IN} = 500 MHz			41		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-1 dBFS)			38		
Effective number of bits <u>2/</u>	ENOB	F _S = 1 GSPS, F _{IN} = 20 MHz	4, 5, 6 <u>1/</u>	01	7		dB
		F _S = 1 GSPS, F _{IN} = 500 MHz			6.6		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-1 dBFS)			6.2		
Signal to noise ratio <u>2/</u>	SNR	F _S = 1 GSPS, F _{IN} = 20 MHz	4, 5, 6 <u>1/</u>	01	42		dB
		F _S = 1 GSPS, F _{IN} = 500 MHz			41		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-1 dBFS)			41		
Total harmonic distortion <u>2/</u>	THD	F _S = 1 GSPS, F _{IN} = 20 MHz	4, 5, 6 <u>1/</u>	01	50		dB
		F _S = 1 GSPS, F _{IN} = 500 MHz			46		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-1 dBFS)			42		
Spurious free dynamic range <u>2/</u>	SFDR	F _S = 1 GSPS, F _{IN} = 20 MHz	4, 5, 6 <u>1/</u>	01	-52		dBc
		F _S = 1 GSPS, F _{IN} = 500 MHz			-47		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-1 dBFS)			-42		
		F _S = 1 GSPS, F _{IN} = 1000 MHz (-3 dBFS)			-45		
Two-tone intermodulation distortion <u>2/</u>	IMD	F _{IN1} = 489 MHz@F _S = 1 GSPS F _{IN2} = 490 MHz@F _S = 1 GSPS	4, 5, 6 <u>1/</u>	01	-47		dBc
Maximum clock frequency	F _S	See figure 4, <u>6/</u>	4, 5, 6 <u>1/</u>	01	1	1.4	GSPS
Minimum clock frequency	F _S	See figure 4, <u>7/</u>	4, 5, 6 <u>1/</u>	01	10	50	MSPS
Maximum clock pulse width (high)	t _{C1}	See figure 4	4, 5, 6 <u>1/</u>	01	0.28	50	ns
Maximum clock pulse width (low)	t _{C2}	See figure 4	4, 5, 6 <u>1/</u>	01	0.35	50	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55 (-0/+5)°C < T _C ; T _J < +125 (-5/+0)°C V _{EE} = DV _{EE} = -5 V, V _{CC} = +5 V, V _{IN} - V _{INB} = 500 mVpp full scale differential input, digital outputs 75 or 50 Ω differentially terminated. unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Aperture delay	t _A	See figure 4	9, 10, 11 <u>1/</u>	01	100	400	ps
Aperture uncertainty (rms)	Jitter	See figure 4 <u>8/</u>	9, 10, 11 <u>1/</u>	01		0.6	ps
Data output delay	t _{OD}	See figure 4 <u>9/</u> , <u>10/</u> , <u>11/</u>	9, 10, 11 <u>1/</u>	01	1150	1660	ps
Output rise/fall time for DATAs (20% - 80%)	t _R /t _F	See figure 4 <u>10/</u>	9, 10, 11 <u>1/</u>	01	250	550	ps
Output rise/fall time for Data ready (20% - 80%)	t _R /t _F	See figure 4 <u>10/</u>	9, 10, 11 <u>1/</u>	01	250	550	ps
Data ready output delay	t _{DR}	See figure 4 <u>9/</u> , <u>10/</u> , <u>11/</u>	9, 10, 11 <u>1/</u>	01	1110	1620	ps
Data ready reset delay	t _{RDR}	See figure 4	9, 10, 11 <u>1/</u>	01		1000	ps
Data to data ready. Clock low pulse width	t _{OD} -t _{DR}	See figure 4 <u>12/</u> , <u>13/</u>	9, 10, 11 <u>1/</u>	01	0	80	ps
Data to data ready. Output delay (50% clock duty cycle)	t _{D1}	@ 1 GSPS	9, 10, 11 <u>1/</u>	01	420	500	ps
Data pipeline delay	t _{PD}	See figure 4	9, 10, 11 <u>1/</u>	01	4	4	clock cycles

1/ These subgroups shall be measured only for the initial test and after process or design changes which may affect the parameter. A minimum sample of 5 devices with zero failures shall be required.

2/ Single ended or differential input mode, 50% clock duty cycle (CLK, CLKB), Binary output data format.

3/ Differential output buffers are internally loaded by 75Ω resistors. Buffer bias current = 11 mA.

4/ Histogram testing based on sampling of a 10 MHz sinewave at 50 MSPS.

5/ Output error amplitude < +/- LSB around worst code.

6/ Min value guaranties performances. Max value guaranties functionality.

7/ Min value guaranties functionality. Max value guaranties performances.

8/ Maximum jitter value obtained for single-ended clock input on the die (chip on board): 200 fs.

9/ Specified loading conditions for digital outputs:

- 50 ohms or 75 ohms controlled impedance traces properly 50/75 ohms terminated, or unterminated 75 ohms controlled impedance traces.
- Controlled impedance traces far end loaded by 1 standard ECLinPS register. (e.g. 10E452)(Typical input parasitic capacitance of 1.5 pF including package and ESD protections.)

10/ Termination load parasitic capacitance derating values:

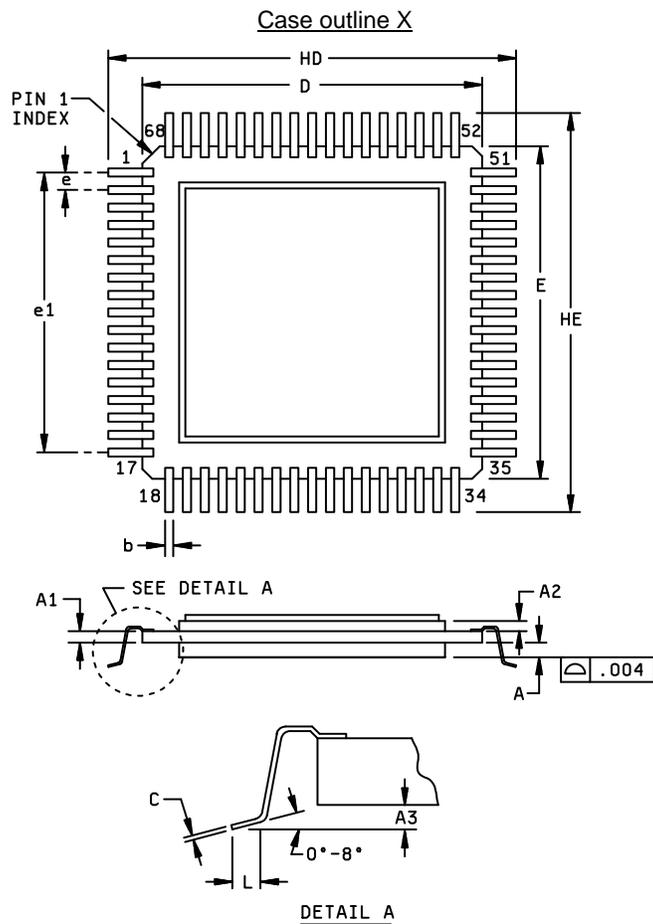
- 50 ohms or 75 ohms controlled impedance traces properly 50/75 ohms terminated: 60 ps/pF or 75 ps per additional ECLinPS load.
- Unterminated (source terminated) 75 ohms controlled impedance lines: 100 ps/pF or 150 ps per additional ECLinPS termination load.

11/ Apply proper 50/75 impedance traces propagation time derating values: 6 ps/mm (155 ps/inch) for the evaluation board.

12/ At 1GSPS, 50/50 clock duty cycle, t_{C2} = 500 ps (t_{C1}). t_{DR} - t_{OD} = -100 ps (typ.) does not depend on the sampling rate.

13/ Values for t_{OD} and t_{DR} track each other over temperature, (1 percent variation for t_{OD} - t_{DR} per 100 degrees Celsius temperature variation). Therefore t_{OD} - t_{DR} variation over temperature is negligible. Moreover, the internal (onchip) and package skews between each data t_{ODS} and t_{DR} effect can be considered as negligible. Consequently, minimum values for t_{OD} and t_{DR} are never more than 100 ps apart. The same is true for the t_{OD} and t_{DR} maximum values.

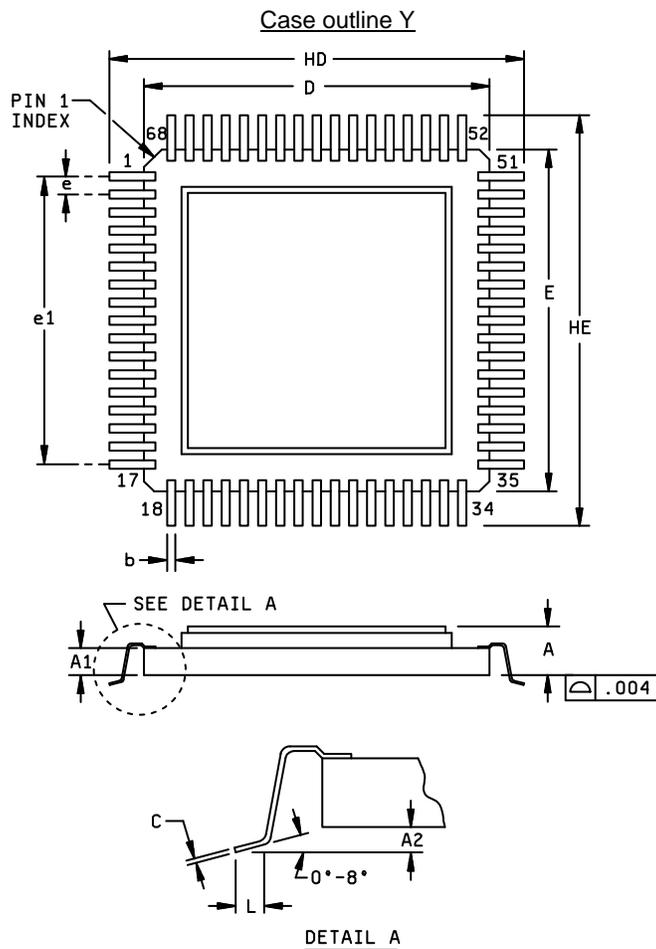
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Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		0.0385		0.978
A1		0.0310		0.787
A2	0.017	0.023	0.43	0.59
A3	0.002	0.012	0.05	0.31
b	0.021	0.025	0.53	0.63
C	0.005	0.010	0.13	0.25
D/E	0.944	0.956	23.978	24.282
HD/HE	1.133	1.147	28.78	29.13
e	0.050 BSC		1.27 BSC	
e1	0.800 BSC		20.32 BSC	
L	0.027	0.037	0.70	0.95

FIGURE 1. Case outlines.

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Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		0.135		3.43
A1	0.067	0.083	1.7	2.1
A2	0.018	0.035	0.46	0.88
b	0.021	0.025	0.53	0.63
C	0.005	0.010	0.13	0.25
D/E	0.944	0.956	23.978	24.282
HD/HE	1.133	1.147	28.78	29.13
e	.050 BSC		1.27 BSC	
e1	.800 BSC		20.32 BSC	
L	0.027	0.037	0.70	0.95

Note: The U.S. Government preferred system of measurement is the metric S.I. system. However, since this item was originally designed using inch-pound units of measurements, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

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Device Type	01
Case outline	X and Y
Terminal number	Terminal symbol
1	V _{PLUSD}
2	V _{PLUSD}
3	D ₅
4	D _{5B}
5	GND
6	D ₄
7	D _{4B}
8	DV _{EE}
9	DV _{EE}
10	DV _{EE}
11	DR
12	DRB
13	GND
14	D ₃
15	D _{3B}
16	V _{PLUSD}
17	V _{PLUSD}
18	V _{PLUSD}
19	D ₂
20	D _{2B}
21	D ₁
22	D _{1B}
23	D ₀
24	D _{0B}
25	GORB
26	V _{CC}
27	GND
28	GND
29	V _{CC}
30	V _{EE}
31	V _{EE}
32	V _{CC}
33	V _{CC}
34	GND

Device Type	01
Case outline	X and Y
Terminal number	Terminal symbol
35	GND
36	GND
37	CLK
38	CLK
39	CLKB
40	CLKB
41	GND
42	GND
43	GND
44	V _{EE}
45	V _{EE}
46	V _{CC}
47	V _{CC}
48	V _{EE}
49	DIOD/DRRB
50	GND
51	GND
52	GND
53	GND
54	V _{IN}
55	V _{IN}
56	V _{INB}
57	V _{INB}
58	GND
59	GND
60	Gain
61	V _{CC}
62	OR
63	ORB
64	D ₇
65	D _{7B}
66	D ₆
67	D _{6B}
68	V _{PLUSD}

FIGURE 2. Terminal connections.

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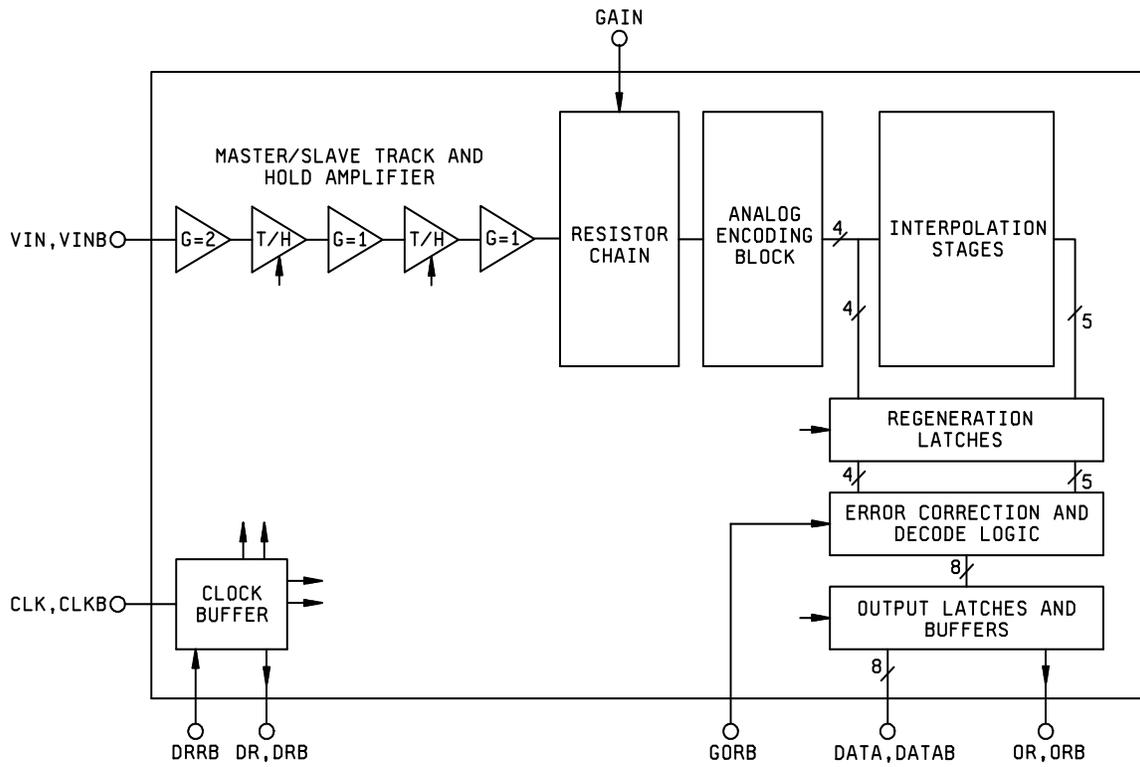
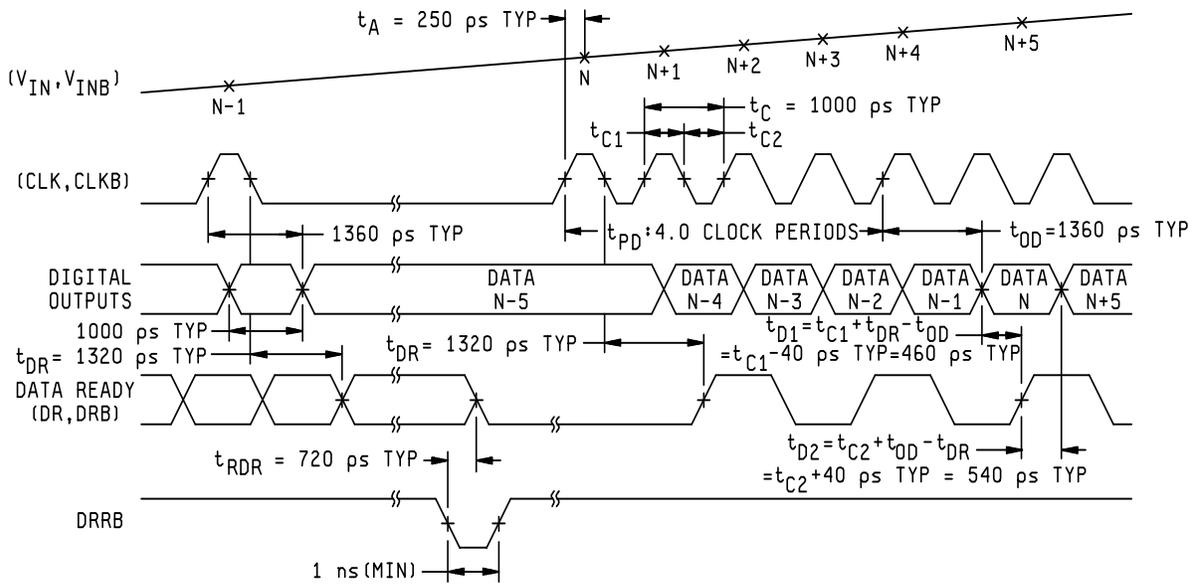
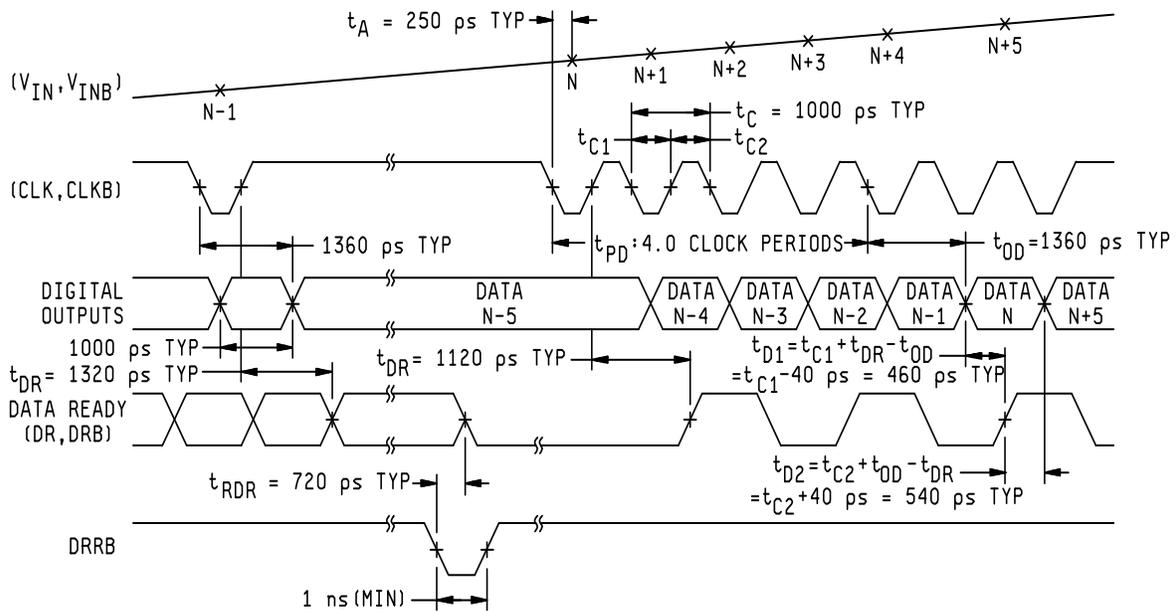


FIGURE 3. Block diagram.

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1 GSPS clock rate, data ready reset, clock held at LOW level.



1 GSPS clock rate, data ready reset, clock held at HIGH level.

FIGURE 4. Timing waveforms.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 57 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9	1, 9
Final electrical parameters (see 4.2)	<u>1/</u> , <u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11	<u>1/</u> , <u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11	<u>1/</u> , <u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	<u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11	<u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11	<u>2/</u> 1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ Subgroups 4, 5, 6, 9, 10, 11 shall be measured only for the initial test and after process or design changes which may affect the parameter. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and table III herein.

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TABLE III. Symbol definitions.

Symbol	Signal name	Function
GND	Ground	Ground pins. To be connected to external ground plane.
V _{PLUSD}	Digital positive power supply	Digital positive supply. (0 V for ECL compatibility, +2.4 V for LVDS compatibility). (See note)
V _{CC}	Positive power supply	+5 V positive supply.
V _{EE}	Analog negative power supply	-5 V analog negative supply.
DV _{EE}	Digital negative power supply	-5 V digital negative supply.
V _{IN}	Differential analog input	In phase (+) analog input signal of the sample and hold differential preamplifier.
V _{INB}	Differential analog input	Inverted phase (-) of analog input signal (V _{IN}).
CLK	Differential clock input	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	Differential clock input	Inverted phase (-) of ECL clock input signal (V _{IN}).
D ₀ , D ₁ , D ₂ , D ₃ , D ₄ , D ₅ , D ₆ , D ₇	Differential output data port	In phase (+) digital outputs. B ₀ is the LSB. B ₇ is the MSB.
D _{0B} , D _{1B} , D _{2B} , D _{3B} , D _{4B} , D _{5B} , D _{6B} , D _{7B}	Differential output data port	Inverted phase (-) digital outputs. B _{0B} is the inverted LSB. B _{7B} is the inverted MSB.
OR	Out of range output	In phase (+) out of range bit. Out of range is high on the leading edge of code 0 and 256.
ORB	Out of range output	Inverted phase (-) of out of range bit (OR).
DR	Differential data ready output	In phase (+) output of data ready signal.
DRB	Differential data ready output	Inverted phase (-) output of data ready signal (DR).
GORB	Gray or binary digital output select	Gray or binary select output format control pin. Binary output format if GORB is floating or V _{CC} . Gray output format if GORB is connected at ground (0 V).
GAIN	ADC gain adjust	ADC gain adjust pin.
DIOD/DRRB	Die junction temp. measurement /asynchronous data ready reset	This pin has a double function (can be left open or grounded if not used): DIOD: die junction temperature monitoring pin. DRRB: asynchronous data ready reset function.

NOTE: The common mode level of the output buffers is 1.2 V below the positive digital supply. For ECL compatibility the positive digital supply must be set at 0 V (ground). For LVDS compatibility (output common mode at +1.2 V) the positive digital supply must be set at 2.4 V. If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-11-19

Approved sources of supply for SMD 5962-00504 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0050401QXC	F8385	TS8388BMFSB/Q
5962-0050401QYC	F8385	TS8388BMFB/Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

F8385

Vendor name
and address

E2V Semiconductors
Avenue De Rochepleine
BP 123
Saint Egreve CEDEX 38521, France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.