The documentation and process conversion measures necessary to comply with this revision shall be completed by 15 October 2014.

INCH–POUND
MIL–STD–750–4
w/CHANGE 1
15 August 2014
SUPERSEDING
MIL–STD–750-4
3 January 2012
(see 6.4)

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

DIODE ELECTRICAL TEST METHODS FOR SEMICONDUCTOR DEVICES

PART 4: TEST METHODS 4000 THROUGH 4999

AMSC N/A

FSC 5961

FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This entire standard has been revised. This revision has resulted in many changes to the format, but the most significant one is the splitting the document into parts. See MIL–STD–750 for the change summary.

3. Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218–3990, or emailed semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

SUMMARY OF CHANGE 1 MODIFICATIONS

1. Test method 4011 was revised to rename the specified methods as conditions.

2. Test method 4066 was revised to include a new ESD current impulse test condition.

Test method	Paragraph	Modification
4011	3.1	Changed
4011	3.2	Changed
4011	3.3	Changed
4011	4.a	New
4066	2	Changed
4066	6.2	Changed
4066	7.1	Changed
4066	8	New
4066	8.1	New
4066	8.2	New

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4301	Junction capacitance
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4326	Series resistance
4331	Switching time

1. SCOPE

1.1 Purpose. Part 4 of this test method standard establishes uniform test methods for the basic electrical testing of semiconductor diodes to determine resistance to deleterious effects of natural elements and conditions surrounding military operations. For the purpose of this standard, the term "devices" includes such items as transistors, diodes, voltage regulators, rectifiers, tunnel diodes, and other related parts. This part of a multipart test method standard is intended to apply only to semiconductor devices.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The electrical test methods included in this part are numbered 4000 to 4999 inclusive.

1.2.2 Test method revisions. Test method revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 4011.4 designates the fourth revision of test method 4011.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 and the individual test methods of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 and the individual test methods of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750 – Test Methods For Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASME INTERNATIONAL (ASME)

ASME Y14.38 – Abbreviations and Acronyms for Use on Drawings and Related Documents.

(Copies of these documents are available online at http://www.asme.org or from ASME International, Three Park Avenue, New York, NY 10016–5990.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JESD320 – Conditions for Measurement of Diode Static Parameters.

(Copies of this document are available online at http://www.jedec.org or from JEDEC, 3103 North 10th Street, Suite 240-S Arlington, VA 22201–2107.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related applicable specification sheet, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purposes of this part of the test method standard, the abbreviations, symbols, and definitions specified in MIL–PRF–19500, ASME Y14.38, and herein shall apply.

3.2 Acronyms used in this standard. Acronyms used in this part of the test method standard are defined as follows:

a. ATE – Automatic test equipment.

b. CFM – Cubic feet per minute.

c. CHLD – Cumulative Helium Leak Detector.

d. DUT – Device under test.

e. ESD – Electrostatic discharge.

f. ESDS – Electrostatic discharge sensitivity.

g. FET – Field-effect transistor.

h. FIST – Forward instability shock test.

i. FWHM – Full-width half-max.

j. GaAs – Gallium Arsenide.

k. GND – Ground.

l. HCFC – Hydrochlorofluorocarbons.

m. HTRB – High temperature reverse bias.

n. Hz – Hertz.

o. IF – Intermediate frequency.

p. IGBT – Insulated gate bipolar transistor.

q. LCC – Leadless chip carrier.

r. MELF – Metal electrode leadless face.

s. mH – Microhenries.

t. MOS – Metal oxide semiconductor

u. MOSFET – Metal oxide semiconductor field-effect transistor.

v. NIST – National Institute of Standards and Technology.

w. ns – Nanosecond.

x.	PIND	–	Particle impact noise detection.
y.	pF	–	Picofarad.
z.	P-N		p-n junction
aa.	ppmv	–	Parts per million volume
bb.	RF	–	Radio frequency.
cc.	RH	–	Relative humidity.
dd.	SEM	–	Scanning electron microscope.
ee.	SOA	–	Safe operating area.
ff.	SSOP	–	Steady-state operating power.
gg.	STU	–	Sensitivity test unit.
hh.	SWR	–	Standing wave ratio.
ii.	TLD	–	Thermoluminescence dosimetry.
jj.	TDE		Time dependent effects.
kk.	TSP	–	Temperature sensitive parameter.
ll.	UHF	–	Ultra high frequency.

4. GENERAL REQUIREMENTS

4.1 General. Unless otherwise specified in the individual test method, the general requirements of MIL–STD–750 shall apply.

4.2 Test conditions for electrical measurements. Unless otherwise required for a specified test method, semiconductor devices should not be subjected to any condition that will cause any maximum rating of the device to be exceeded. The precautions should include limits on maximum instantaneous currents and applied voltages. High series resistances (constant current supplies) and low capacitances are usually required. If low cutoff or reverse current devices are to be measured; for example, nanoampere units, care should be taken to ensure that parasitic circuit currents, or external leakage currents are small compared with the cutoff or reverse current of the device to be measured.

4.2.1 Steady-state dc measurements (test method series 4000). Unless otherwise specified, all steady-state dc parameters are defined using steady-state dc conditions.

4.2.2 Pulse measurements (test method series 4000). When device static or dynamic parameters are measured under pulsed conditions, in order to avoid measurement errors introduced by device heating during the measurement period, the following items should be covered in the performance specification sheet:

a. The statement "pulsed test" shall be placed by the test specified.

b. Unless otherwise specified, the pulse time (t_p) shall be ≤10 milliseconds and the duty cycle shall be a maximum of 2 percent; within this limit the pulse must be long enough to be compatible with test equipment capability and the accuracy required, and short enough to avoid heating.

4.2.3 Electrical characteristics tests for microwave diodes (test method series 4100). When device static or dynamic parameters are measured under pulsed conditions, in order to avoid measurement errors introduced by device heating during the measurement period, the following items should be covered in the performance specification sheet:

a. Measurement of conversion loss, output noise ratio, and other microwave parameters shall be conducted with the device fitted in the holder. All fixed adjustments of the holder shall be made at a laboratory designated by the Government. In the test equipment, the impedance presented to the mixer by the local oscillator (and the signal generator, if used) shall be the characteristic impedance of the transmission line between the local oscillator and mixer (the maximum VSWR, looking toward the local oscillator, shall be 1.05 at the signal and image frequencies).

b. For qualification inspection of reversible UHF and microwave devices, the radio frequency measurements, excluding the post environmental test end points and high temperature life (nonoperating) end points, shall be made, first, with the adapter on one end of the device, and then repeated with the adapter at the opposite end of the device; for the environmental and life tests, fifty percent of each sample shall be tested with the adapter on one end of the device and the remaining half of the sample shall be tested with the adapter on the opposite end of the device. End point measurements shall be made without moving the adapter. This procedure shall be repeated on at least one lot every 6 months.

c. For quality conformance inspection of reversible UHF and microwave devices, the electrical measurements, including the post environmental test end points, may be made with the adapter on either end of the device.

4.2.4 Test circuits. The test circuits shown in the test methods of this test method standard are given as examples which may be used for the measurements. They are not necessarily the only test circuits which can be used; however the manufacturer shall demonstrate to the Government that other test circuits which they may desire to use will give results within the desired accuracy of measurement. Circuits are shown for PNP transistors in one circuit configuration only. They may readily be adapted for NPN devices and for other circuit configurations.

4.3 Non–destructive tests. Unless otherwise demonstrated, the test methods listed in table I shall be classified as nondestructive.

TABLE I. Non-destructive tests.

Test method number	Test
4066	Surge current
4081	Thermal resistance of lead mounted diode (forward voltage, switching method)

NOTE: When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions or approved accelerated screening when it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and in the case where it is allowed adequate sample testing, shall be performed to provide the proper reliability safeguards.

4.4 Destructive tests. No test methods within this test method standard have been classified as destructive.

4.5 Laboratory suitability. Prior to processing any semiconductor devices intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written Laboratory Suitability status for each test method to be employed. Processing of any devices by any facility without Laboratory Suitability status for the test methods used shall render the processed devices nonconforming.

* 4.6 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification or specification sheet by specifying the test method number, and the details required in the summary of the applicable test method shall be listed. To avoid the necessity for changing specifications that refer to this test methods of this standard, the revision number should not be used when referencing test methods. (For example: Use 4011 versus 4011.4.)

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this test method standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This test method standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this test method standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this test method standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing.

Destructive tests
Electrical characteristics tests
Laboratory Suitability
Non–destructive tests

6.4 Supersession data. The main body and five parts (–1 through –5) of this revision of MIL–STD–750 replace superseded MIL–STD–750E.

6.5 Changes from previous issue. The margins of this standard are marked with asterisks where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

METHOD 4000

CONDITION FOR MEASUREMENT OF DIODE STATIC PARAMETERS

1. Purpose. The purpose of this test method is for measuring a temperature-sensitive static parameter under conditions such that the product of the applied voltage and current at the test point produces a power dissipation level that will cause significant heating of the junction, the measured result may be subject to errors due to thermal or transient effects. In order to avoid such errors, the measurement should be made under defined conditions.

2. Steady-state dc measurements. When making measurements under conditions of steady-state dc, a condition of thermal equilibrium may be considered to have been achieved if halving the time between the application of power and the taking of the reading causes no error in the indicated results within the required accuracy of measurement. For these purposes very long pulses or step functions may be considered as steady-state dc. When appropriate, the mounting conditions (T_L or T_C) or the thermal resistance (reference point to ambient $R_{\theta CA}$ or $R_{\theta LA}$) shall be specified.

3. Pulse measurements. When a measurement is made under pulse conditions, the point of measurement after the start of the pulse shall be chosen such that it is long enough to charge interconnecting test cable capacitance, avoid electrical transient effects, and short enough to avoid heating effects. This can be ensured if halving the minimum selected time, or doubling the maximum selected time, will not produce errors beyond the defined accuracy of the measurement. The pulse measurement may be intended to correlate to a steady-state dc measurement, provided that a correlation has been established.

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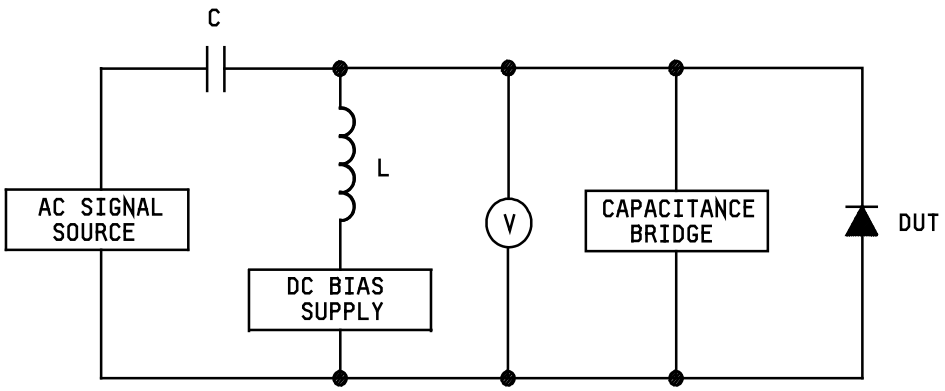
METHOD 4001.1

CAPACITANCE

1. Purpose. The purpose of this test method is to measure the capacitance across the semiconductor device terminals under specified dc bias and ac signal voltages.

2. Test circuit. See figure 4001–1.



NOTE: Both dc bias and ac signal sources may be incorporated in the capacitance bridge. The dc bias source should be properly isolated, preferably with an inductance L in series and have negligible capacitance compared to the DUT. The reactance of C must be negligible compared to the reactance of the DUT, at the frequency of measurement. Impedance of voltmeter should be at least 10 times that of the DUT.

FIGURE 4001–1. Test circuit for capacitance.

3. Procedure. The dc voltage source shall be adjusted to the specified bias voltage. The ac small signal voltage shall be adjusted to the specified frequency for the capacitance measurement. The bridge shall be nulled and adjusted for zero capacitance reading just prior to insertion of the DUT to eliminate error from external circuitry.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. DC bias voltage.

b. Test frequency.

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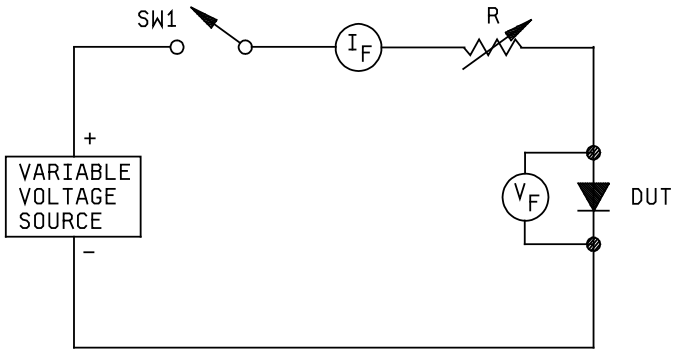
METHOD 4011.5

FORWARD VOLTAGE

1. Purpose. The purpose of this test method is to measure the voltage across the device when a specified current flows through the device in the forward direction.

2. Test circuit. See figure 4011–1.



NOTE: When specified, switch SW1 shall consist of either an electronic switch or a pulse generator to provide pulses of short-duty cycle to minimize device heating. When pulse techniques are used, suitable peak-reading methods shall be used to measure the parameters of pulse amplitude, frequency, duty cycle, and pulse width. When dc techniques are used, device thermal equilibrium shall be achieved before the measurement is made.

FIGURE 4011–1. Test circuit for forward voltage.

3. Procedure.

* 3.1 Condition A (DC method). The specified test current (I_F) shall be adjusted by varying either the variable voltage source or the resistor (R). The value of I_F shall be measured using an ammeter. The forward voltage (V_F) shall be measured using a dc voltmeter. The voltmeter connections shall be made at specified points on the device and always within the current connection points.

* 3.2 Condition B (pulse method). An oscilloscope shall be used to measure the pulse characteristics. The pulse generator or electronic switch shall be adjusted to achieve the specified amplitude, frequency, and pulse width values. Device current (I_F) may be determined by measuring the voltage drop across a known value of resistor (R) where:

$$I_F = \frac{V\ peak\ X\ duty\ cycle}{R}$$

After adjusting pulse level to correct value for required I_F, measure forward voltage V_F.

* 3.3 Condition C (curve tracer method). A Tektronix Model 576 or equivalent curve tracer shall be used. The device shall be tested by applying a positive voltage to the anode and limiting the current to within the manufacturer's ratings for I_F. The forward voltage may be determined by observing the curve tracer waveform at the specified I_F.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

* a. Test condition letter.

b. Test current (I_F).

c. Forward voltage (V_F).

d. Duty cycle and pulse width, when pulse techniques are used.

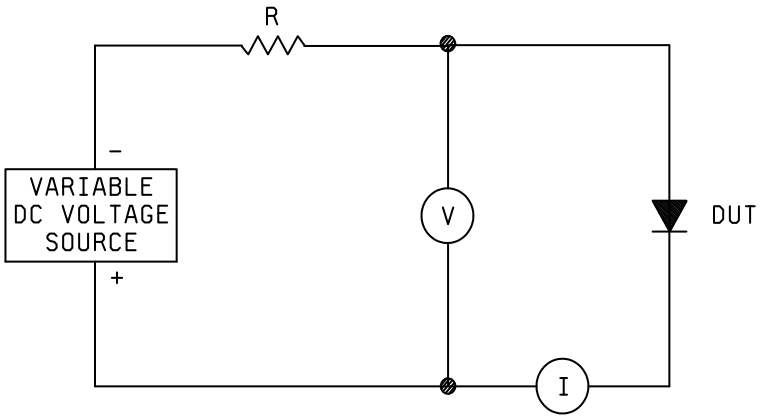
METHOD 4016.4

REVERSE CURRENT LEAKAGE

1. Purpose. The purpose of this test method is to measure the reverse current leakage through a device at a specified reverse voltage using a dc method or an ac method, as applicable.

2. DC method.

2.1 Test circuit. See figure 4016–1.



NOTE: To assure accurate measurement of reverse leakage current, the voltage drop across the ammeter shall be subtracted from the measured value of reverse voltage. Resistor (R) shall be chosen to limit the current flow in the event the device goes into reverse breakdown.

FIGURE 4016–1. Test circuit for reverse current leakage (dc method).

2.2 Procedure.

2.2.1 Reverse current. The dc voltage shall be adjusted to the specified value by voltmeter (V) and the reverse current (I_R) shall be measured by current meter (I).

3. AC method.

3.1 Test circuit. See figure 4016–2.

*NOTE: The resistor R is a selectable value within the curve tracer.

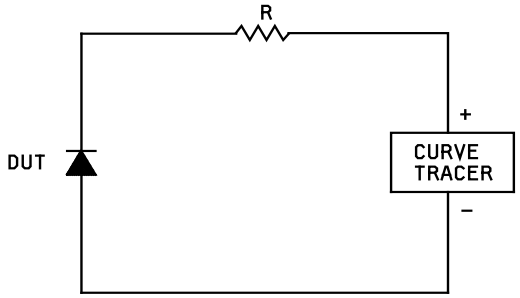


FIGURE 4016–2. Test circuit for reverse current leakage (ac method).

3.2 Procedure.

3.2.1 Reverse current. A Tektronix 576-curve tracer or equivalent shall be used to apply voltage in the reverse direction only. The curve tracer supply shall be adjusted to obtain the specified peak reverse voltage across the device. Current and voltage shall be measured on the curve tracer.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:.

a. DC or ac method.

b. Test voltage (dc method) or peak reverse voltage (ac method).

c. Thermal resistance of minimum heat dissipater on which device is mounted in °C/W (where applicable).

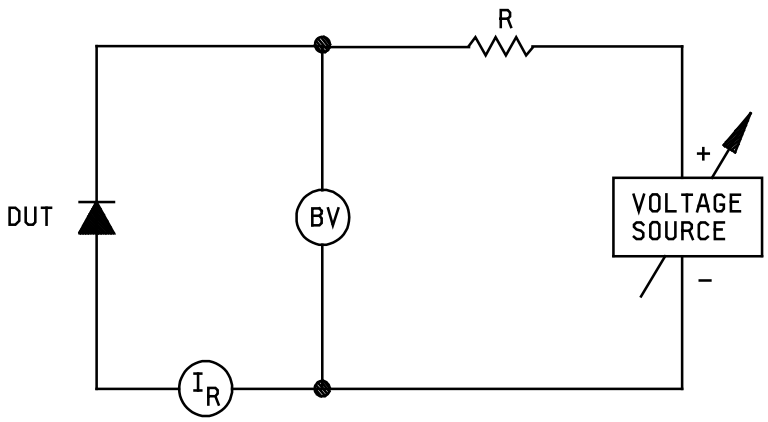
d. Thermal equilibrium or pulse condition such as specified in JEDEC JESD320. (If pulse test is not specified, thermal equilibrium dc test method correlation will be applicable. This may include pulse measurement intended to correlate to steady-state dc measurement as described in JEDEC JESD320.)

METHOD 4021.2

BREAKDOWN VOLTAGE (DIODES)

1. Purpose. The purpose of this test method is to determine if the breakdown voltage of the semiconductor device is greater than the specified minimum limit.

2. Test circuit. The resistance R is a current-limiting resistance and is chosen to avoid excessive current flowing through the device. (See figure 4021–1).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4021–1. Test circuit for breakdown voltage (diodes).

3. Procedure. The reverse current shall be adjusted from zero until either the minimum limit for breakdown voltage or the specified test current is reached. The device is acceptable if the specified minimum limit for BV is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The test current (see 3) shall be specified in the applicable performance specification sheet or acquisition document:

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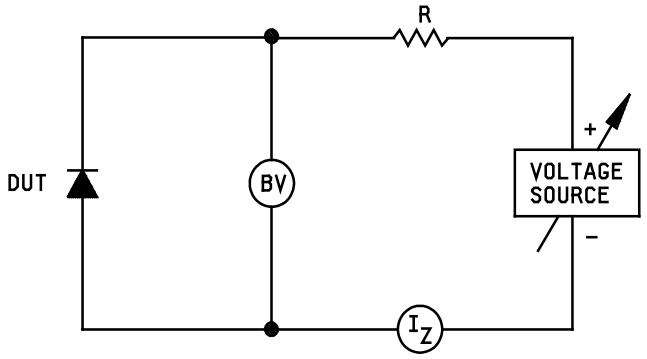
METHOD 4022

BREAKDOWN VOLTAGE
(VOLTAGE REGULATORS AND VOLTAGE-REFERENCE DIODES)

1. Purpose. This test method is designed to measure the breakdown voltage of voltage regulator and voltage-reference semiconductor devices under the specified conditions.

2. Test circuit. See figure 4022–1.



NOTE: The voltmeter being used to measure the terminal voltage should present an open circuit to the terminals across which the voltage is being measured.

FIGURE 4022–1. Test circuit for breakdown voltage (voltage regulators and voltage-reference diodes).

3. Procedure. The reverse current shall be adjusted from zero until the specified test current is reached. The specified test current shall remain applied for the specified time to approach thermal equilibrium with the device mounted as specified in the individual specification sheet. The breakdown voltage shall then be read from the voltmeter.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test current (see 3).

b. Time after application of test current when breakdown voltage shall be read.

c. Method of mounting.

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METHOD 4023.2

SCOPE DISPLAY

1. Purpose. The purpose of this test method is to define criteria for inspection of the dynamic reverse characteristics of rectifiers, switching, and zener diodes when viewed on a curve tracer. This inspection criteria may not be applicable to specific rectifier designs where the semiconductor device is not intended to be driven into avalanche breakdown, or where the applicable specification sheet has not provided for this inspection.

2. Scope. This test applies to all devices requiring stable or sharp and stable breakdown characteristics. Figures 4023–1 through 4023–12 are shown in the first quadrant. The depictions on figures 4023–2 through 4023–12 have been compiled to describe commonly observed faults. The inspections shall be classified as follows:

a. Condition A – stable (only) types. The curve traces on figures 4023–3, 4023–8, 4023–10, and 4023–11 shall apply for condition A.

b. Condition B – sharp and stable types. The curve traces on figures 4023–2 through 4023–12 shall apply for condition B. The ideal sharp and stable trace is one which exhibits a single horizontal line up to the point of breakdown, then transitions vertically to form a 90 degree angle while maintaining the single line (see figure 4023–1). Deviations from this ideal, which are not specifically allowed in this method or applicable specification sheet shall be cause for rejection of the DUT. Tolerances from acceptable devices have been assigned when applicable.

NOTE: Since low voltage zeners do not inherently have, and some other devices may not have a sharp breakdown, specific exceptions in requirements are also provided herein. For ideal reverse trace see figure 4023–1. For soft knee see figure 4023–2. For drift see figure 4023–3.

3. Procedures

a. The curve tracer presentation shall be configured so that the horizontal axis shall be calibrated in volts per division and the vertical axis shall be calibrated in amperes per division (or fractions thereof). The vertical and horizontal axis of the curve tracer presentation will be graduated into eight or ten divisions, each representing a precalibrated increment of current or voltage.

b. A series load resistor shall be used to limit the device reverse current and prevent device damage. This typical resistance should be approximately one quarter or more of the device resistance at the breakdown specification, when the curve trace set-up permits.

Example: A device to be observed at I_{BR} of 100 μA which is specified to be 400 volts minimum, would have a series resistance chosen according to the following:

$R \geq 0.25\ (400 / 0.0001)$, therefore:
$R \geq 1\ M\Omega$

The curve tracer peak voltage (V_{CT}) may also require limitation, particularly if the series load resistance described cannot be achieved. See figure 4023–1 and 3.e. for typical load line relationships to assure safe reverse current monitoring.

Unless otherwise specified, the breakdown current shall be the current used for the breakdown voltage test.

c. The trace should occur in the first and third quadrant of the display and be slowly adjusted from zero volts to attain the specified current with the maximum amount of resolution for determination of trace characteristics.

d. The DUT shall be held under breakdown conditions for at least two second to ensure freedom from intermittent instability for breakdown drift.

e. The vertical and horizontal sensitivity shall be adjusted on the curve tracer to provide a rendition of the complete trace to the specified current. Horizontal and vertical sensitivity shall be adjusted to provide a trace occupying no less than 50 percent of the available screen.

f. The curve trace voltage shall not be simply set at a predetermined value and snapped on instantaneously. This may be done only if the product to be tested is known to have a sufficiently narrow breakdown voltage (V_{BR}) range with a predetermined series (load line) resistor setting (see b.) and described below, to assure that the device will not be overpowered. This is typically the case for zener diodes prescreened on V_Z (or V_{BR}). The peak open circuit supply voltage of the curve tracer (V_{CT}) may then be adjusted such that the V_{CT} setting can provide no more current (I_{BR} or I_Z) than that required for avalanche breakdown, taking into account the series load resistance R on figure 4023–1. Unless otherwise specified, these relationships may be calculated by:

$$I_{BR} = \frac{V_{CT} - V_{BR}}{R}, \text{ and } V_{CT} = I_{BR}R + V_{BR}$$

The resistance R may be determined by:

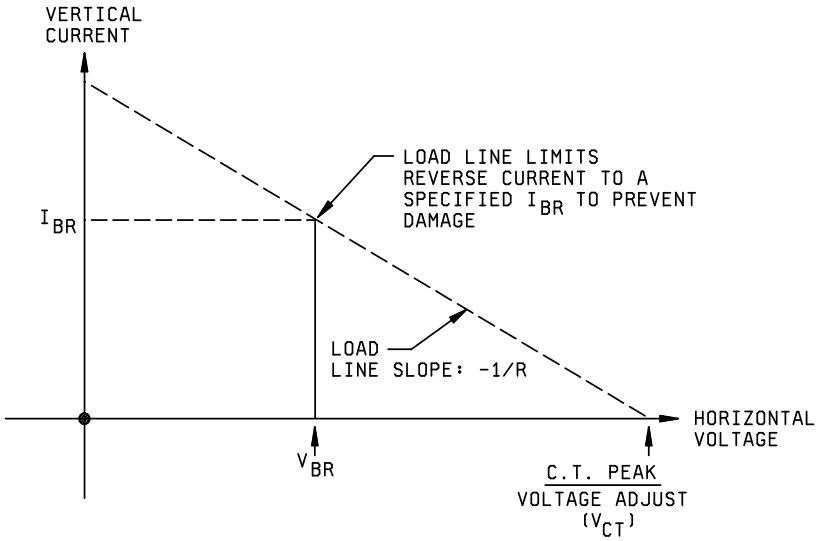
$$R = \frac{V_{CT} - V_{BR}}{I_{BR}}$$

The V_{BR} (or V_Z) utilized in this equation should be the minimum expected so as to always maximize the R value selected.

g. Allowance for deviation from the desired characteristics described in this method or applicable specification sheet shall be granted by the qualifying activity. If a particular rejectable trace described is expected in a manufacturer's normal process, it shall be identified and explained during device conformance/ qualification. Devices exhibiting the exceptional trace characteristic shall be present in the conformance/qualification lot to establish reliability.

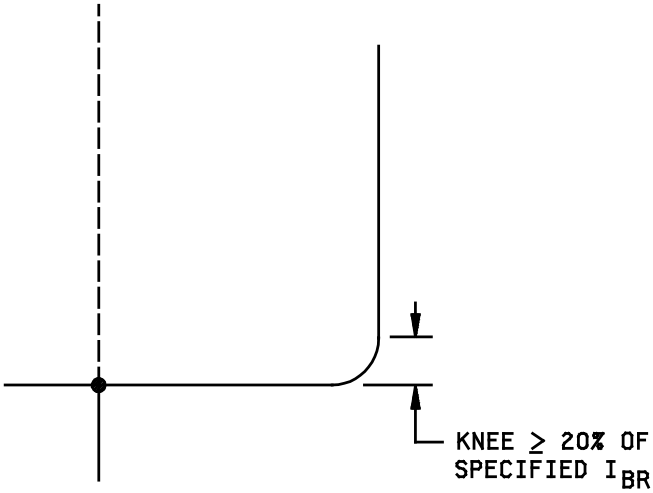
h. Any device that is stable and passes the applicable illustrated scope conditions shall be passed. Any device that exceeds the conditions in the applicable illustrate scope conditions will be failed. Any device that passes but is continuing to move, drift or otherwise change shall be observed for another 2 seconds. This cycle of 2 second intervals will continue until the part stabilizes and passes by still meeting the pass criteria or fails by exceeding the pass criteria. Any device that is still drifting after a total of 10 seconds shall be failed as being chronically unstable.

4. Summary. The following shall be specified in the applicable performance specification sheet or acquisition document: Test condition to be used.



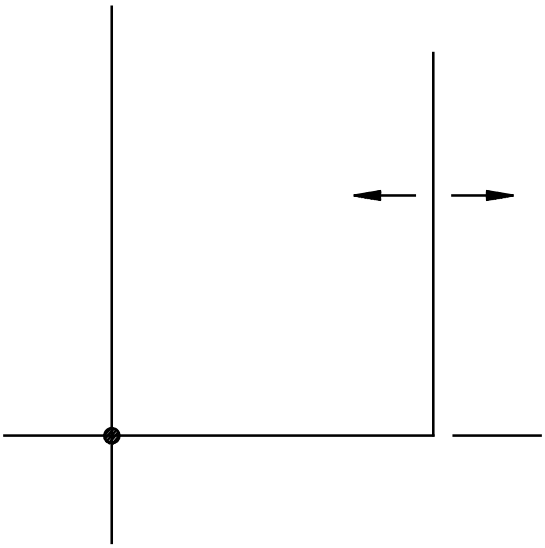
This ideal trace exhibits none of the characteristics described on the figures below. Also, illustrated are the basic curve tracer adjustments and relation for a safe maximum operating current (I_{BR}) with the series load resistor (R) versus peak open circuit voltage (V_{CT}) and device breakdown voltage (V_{BR}).

FIGURE 4023–1. Ideal reverse trace.



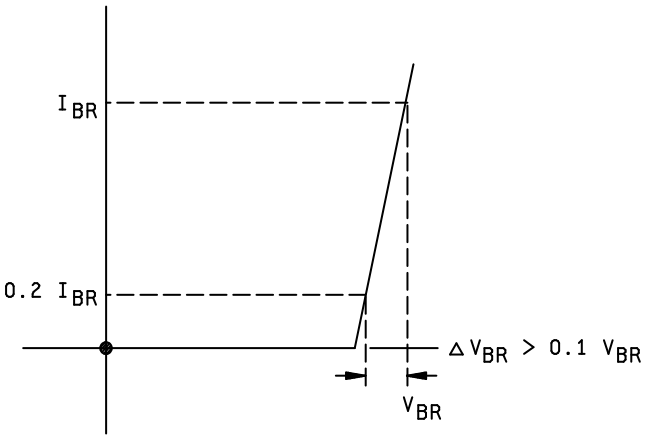
The knee area is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not require more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified Ik_{BR}. Not applicable to signal diodes, low voltage zeners, fast, ultrafast, and Schottky rectifiers or low voltage zeners ≤ 10 volts.

FIGURE 4023–2. Soft knee.



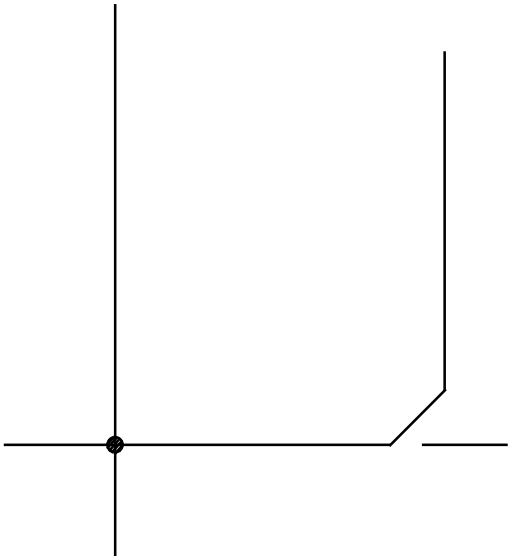
The vertical component of the trace should remain stable in the horizontal axis. An undesirable drift is defined as greater than a 10 percent increase or 2 percent decrease in actual breakdown voltage up to 1,500 volts. If over 1,500 volts, the allowable drift should be separately specified.

FIGURE 4023–3. Drift.



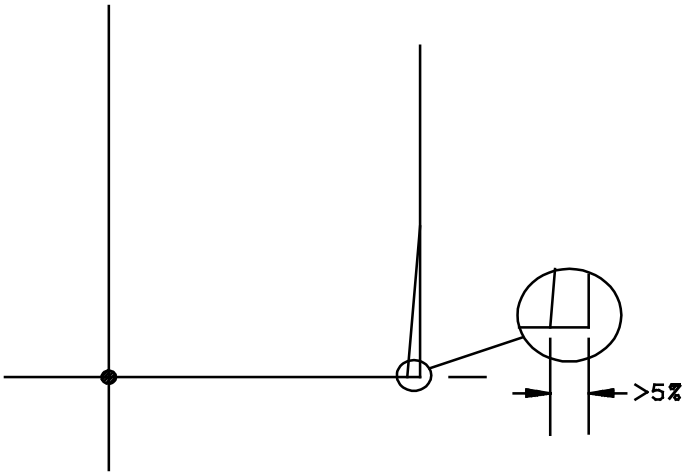
The slope shall be less than 10 percent of V_{BR} when viewed between 20 percent to 100 percent of the specified I_{BR} or I_Z. Low voltage zeners below 5.5 volts are in exception to this requirement also, or other devices, as may be specified.

FIGURE 4023–4. Slope.



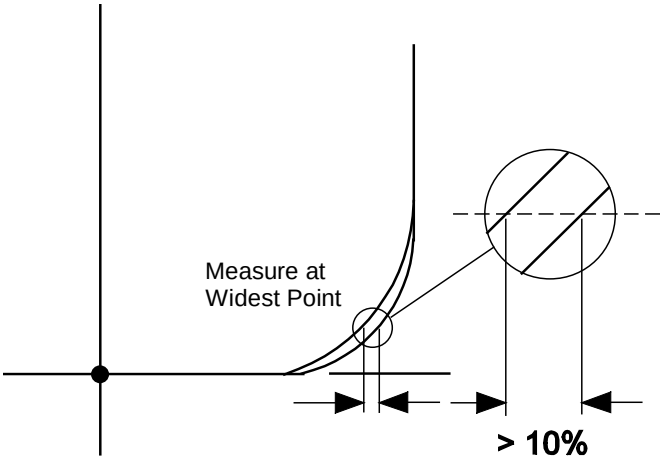
The double break is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not occupy more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified I_{BR} or I_{ZT}. This requirement is not applicable to ultrafast or Schottky rectifiers, and low voltage zeners ≤ 10 volts.

FIGURE 4023–5. Double break (reject criteria for sharp knee devices).



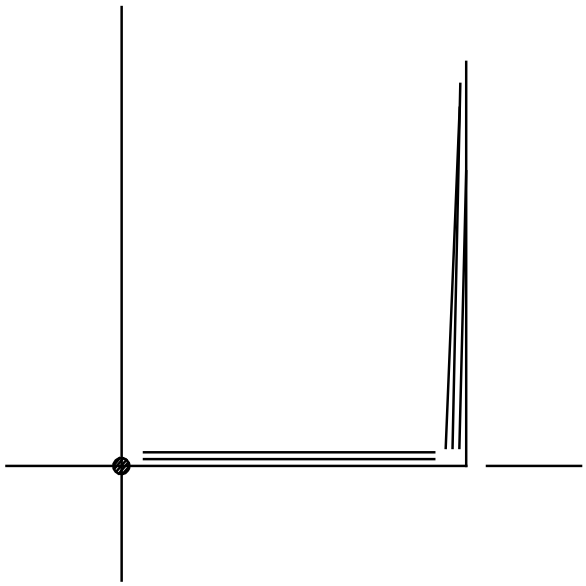
For standard rectifiers and zeners, the region at the knee may display a secondary trace no more than 5 percent of the total voltage of the DUT (see detail).

FIGURE 4023–6. Double trace.



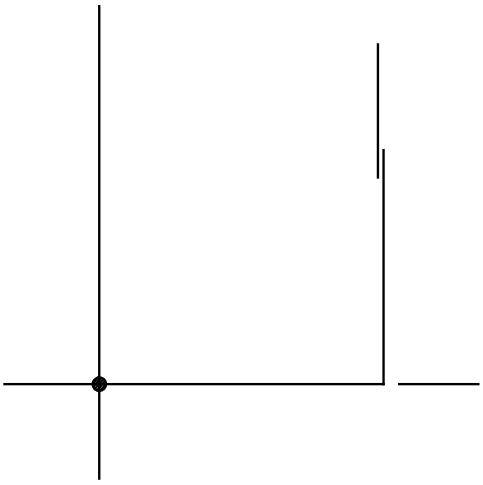
For soft knee diodes including signal diodes, low voltage zeners, and altered junction fast, superfast and ultrafast rectifiers, the region at the knee may display a secondary trace no more than 10 percent of the total voltage of the DUT (see detail).

FIGURE 4023–7. Double trace, soft knee.



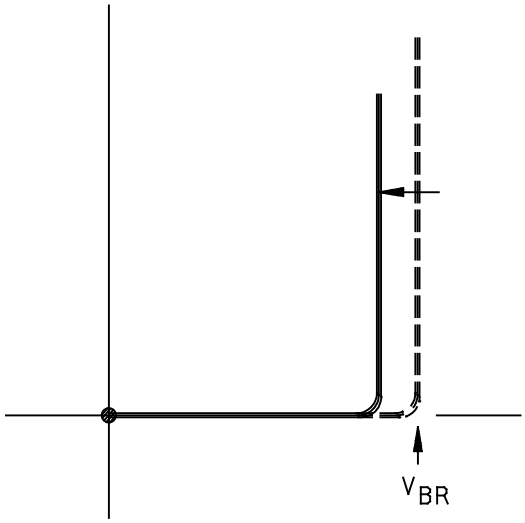
Any jittery movement of the trace in any direction, not caused by power line voltage fluctuations, shall not occur.

FIGURE 4023–8. Unstable (jitter).



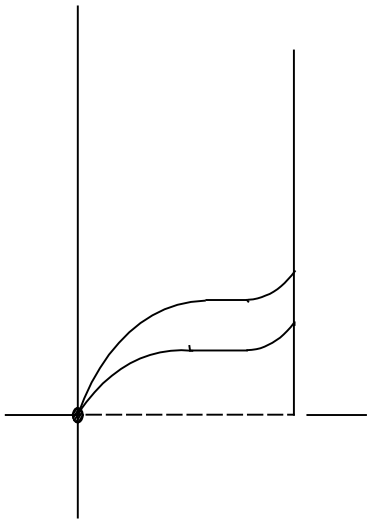
The vertical component shall not depart from a single vertical line, except as allowed on figures 4023–6 and 4023–7.

FIGURE 4023–9. Discontinuity.



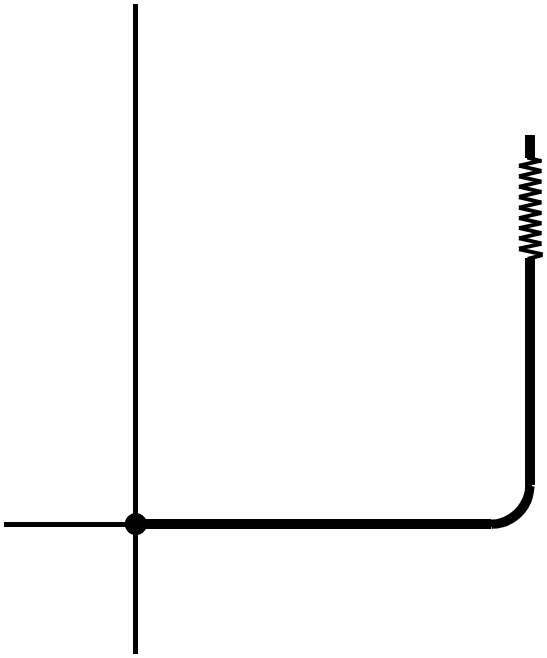
The vertical component shall not decrease its value abruptly by 2 percent or more of V_{BR}.

FIGURE 4023–10. Snap back – collapsing V_{BR}.



Leakage current (vertical) shall not degrade from an initial value.

FIGURE 4023–11. Floater.



Instability (arcing) appearing at or near the specified I_{BR} region on the vertical trace (such as may be coincident with visible sparking activity within the device die region) shall not be present. Noise at or near the knee is permissible, such as typically observed on avalanche-zener devices.

FIGURE 4023–12. Arcing.

METHOD 4026.4

FORWARD RECOVERY VOLTAGE AND TIME

1. Purpose. The purpose of this test method is intended to measure the forward voltage and recovery time of the semiconductor device. A device reveals an excessive transient forward voltage when it is switched rapidly into the forward conductance region. The amplitude and time duration of this voltage peak can be measured by observing the voltage waveform across the device when a flat-top pulse of the specified amplitude, rise time, pulse width, and frequency are applied to the device.

2. Test circuit. See figure 4026–1.

a. The forward transient test circuit shown on figure 4026–1 is used in conjunction with a pulse generator and an output sensing device. Care should be taken to minimize lead length where lead inductance might cause ringing in the test circuit.

b. The value of resistor R_p shall be chosen to optimize the impedance match between pulse generator and test circuit, thereby minimizing the ringing in the test circuit.

3. Procedure. The test shall be performed using the following:

3.1 Conditions:

a. Pulse input A:

(1) I_F amplitude: As specified.

(2) Rise time = 10 ns or as specified.

(3) Pulse width $t_1 \geq 10X$ specified response time.

(4) Generator resistance $R_S \geq 20\ R_F$ ($R_F = V_F/I_F$ at specified I_F).

(5) Pulse frequency shall be such that a reduction in frequency shall result in no change in forward recovery characteristics.

b. Response detector input impedance, $Z \geq 100\ R_F$.

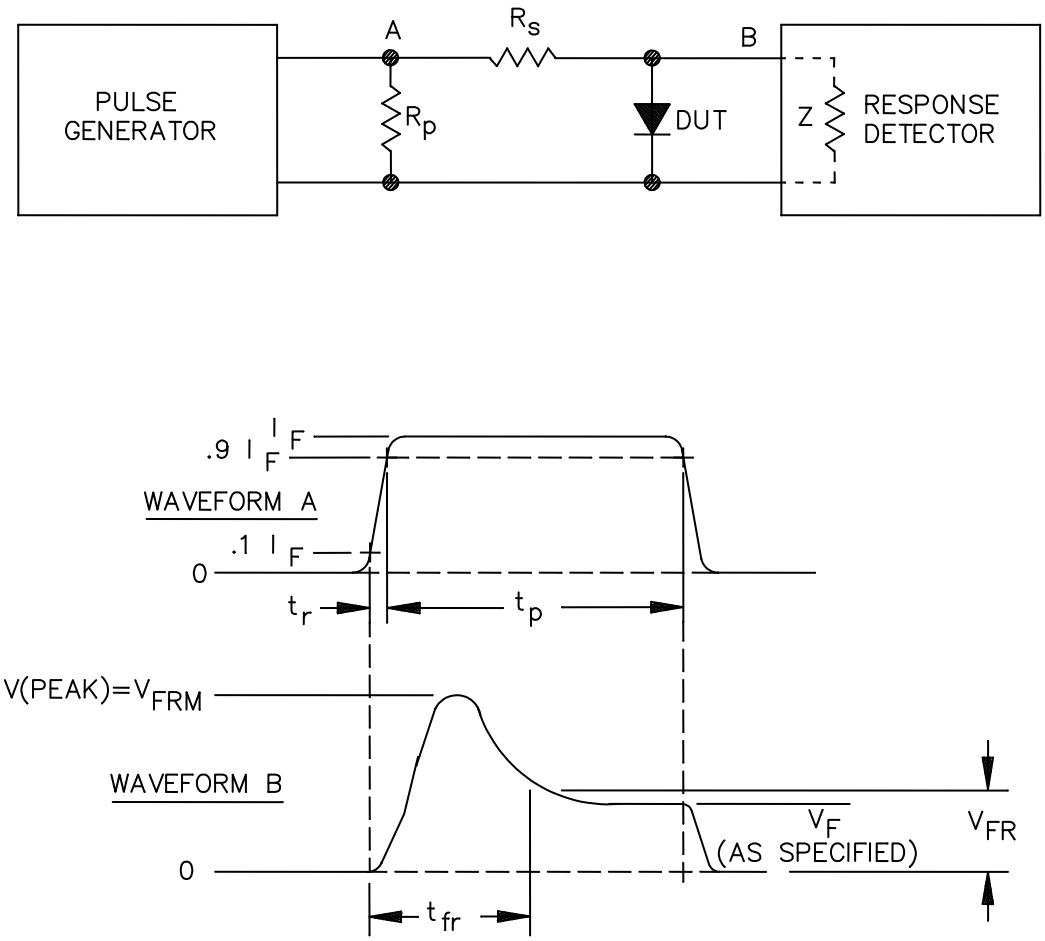


FIGURE 4026–1. Test circuit for forward recovery voltage and time.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. I_F of input waveform A (see 3.1).

b. Rise time if other than 10 nanoseconds (see 3.1).

c. Forward recovery voltage V_{FR} chosen to terminate the forward recovery time measurement (see figure 4026–1).

d. The following measurements should be made: Forward recovery time (t_{fr}) (measured from the time of 0.1 seconds I_F to the time that forward voltage recovers to a specified V_{FR}) (see figure 4026–1).

e. The peak forward voltage $V_{(PEAK)}$ (see figure 4026–1). This symbol is interchangeable with V_{FRM}.

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METHOD 4031.5

REVERSE RECOVERY CHARACTERISTICS

1. Purpose. The purpose of this test method is to measure the reverse recovery time and other specified recovery characteristics related to signal, switching, and rectifier diodes by observing the reverse transient current versus time when switching from a specified forward current to a reverse biased state in a specified manner.

2. General guide for selecting appropriate condition. Four conditions are given to include recommended practice for the range of diodes considered. A general guide for selecting the appropriate condition letter is:

a. Signal diodes with reverse recovery time less than 6 ns.

b. Low to medium current rectifiers with maximum specified recovery times of 25 to 3,000 ns.

c. High current rectifiers with maximum specified recovery times of 350 ns or greater.

d. Ultra-fast rectifiers, particularly on new specification sheets.

Further, detailed guidance is given under each condition below.

3. Test condition A. This condition is particularly relevant to low current, signal diodes faster than 6 ns and tested at 10 mA. However, it is practicable for measurements up to 20 ns and 100 mA.

3.1 Circuit notes for condition A.

a. Rise time of the reverse voltage pulse across a noninductive calibration resistor in place of the DUT shall be less than 20 percent of the recovery time of the DUT, for greatest accuracy.

b. Oscilloscope rise time shall be less than 20 percent of device recovery time, for greatest accuracy.

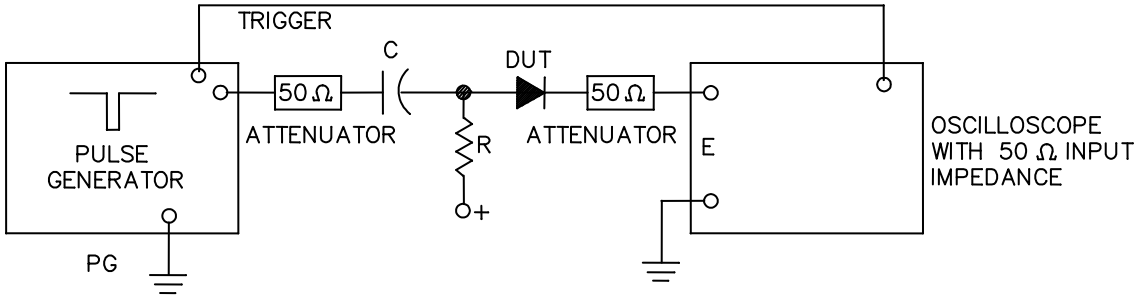
c. Proper coaxial networks and terminations shall be employed to ensure against error-producing pulse reflections.

d. $R > 10\ R_L$.

e. Unless otherwise specified, $R_L = Z_{PG} + Z_{SCOPE} = 100\ \Omega$.

f. $C > 10\ PW \div R_L$.

g. PW > 2 x maximum specified t_{rr} (see figure 4031–1.)



NOTE: The test circuit shall comply with the test conditions.
PW = Pulse width of reverse voltage pulse (see figure 4031–2).
R_L = Load resistance.
C = Coupling capacitance.

FIGURE 4031–1. Test circuit for condition A.

3.2 Procedure for condition A. The specified forward current shall be adjusted by resistor R and the + supply. Voltage E, developed across the 50 ohm oscilloscope input impedance shall be measured. Specified forward current shall be calculated by the expression $I_F = E/50$. The time duration of I_F shall be at least 10 times the device recovery time. The oscilloscope trace deflection above zero reference shall be adjusted by the oscilloscope vertical sensitivity to produce an amplitude of 2 cm minimum vertical deflection. Adjustment of the reverse transient current (I_{RM}) shall be made by varying the pulse generator output, observing the voltage E across the 50 ohm oscilloscope input impedance, and calculating I_{RM} by the expression $I = E/50$. When reverse bias voltage V_R is specified, and I_{RM} is not, the DUT shall be replaced with a shorting bar and I_{RM} shall be calculated by the expression $V_R/50$ (see figure 4031–2.)

3.3 Summary for condition A.

a. The following conditions shall be specified in the applicable specification sheet.

(1) Forward current, I_F.

(2) Reverse current I_{RM} (preferred), or reverse voltage (optional alternative).

(3) Load resistance, if other than 100 Ω (this is the sum of Z_{PG} and Z_{SCOPE}).

(4) Ambient temperature in °C.

(5) Generator impedance, if other than 50 Ω.

(6) Recovery current measuring point, $i_{R(REC)}$, if different from 10 percent of I_{RM}.

b. The following measurement shall be made:

(1) t_{rr} (see figure 4031–2).

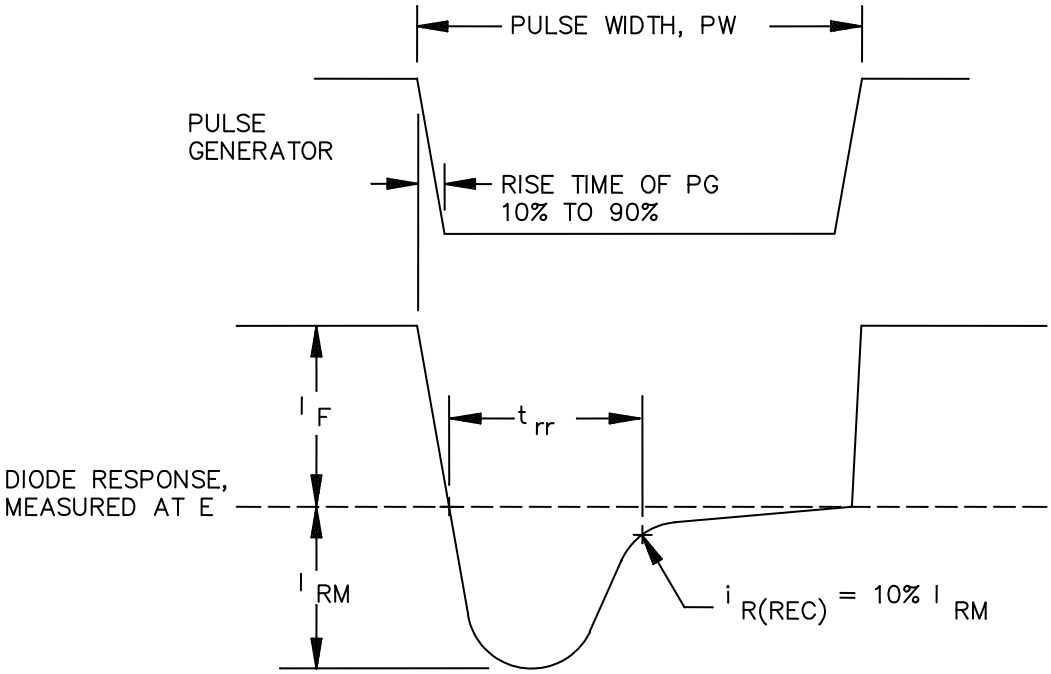


FIGURE 4031–2. Response pulse waveforms for condition A.

4. Test condition B. (See suggested conditions in table 4031–I (e.g., B1, B2) and figures 4031–3 and 4031–4 for test circuit and board layout.) This condition is particularly relevant to medium current (axial and similar) types of standard and fast rectifiers with maximum specified recovery times between 25 and 3,000 ns when measured at peak forward currents greater than 100 mA and less than or equal to 1.0 ampere. It is readily adapted to lower test currents. This test is also appropriate for devices with recovery times less than 25 ns that are measured at peak forward currents of 1A or less; below 25 ns, or at higher current, particular care shall be used to achieve low loop inductance and low circuit rise times to achieve acceptable repeatability.

This condition differs from condition D in that the reverse current (I_{RM}) is limited by the test circuit, not by the DUT.

The test circuit on figure 4031–3 and the method of achieving low inductance for resistor R4 on figure 4031–4 are intended only as a guide to generate the suggested pulse test conditions in table 4031–I.

TABLE 4031–I. Test condition B.

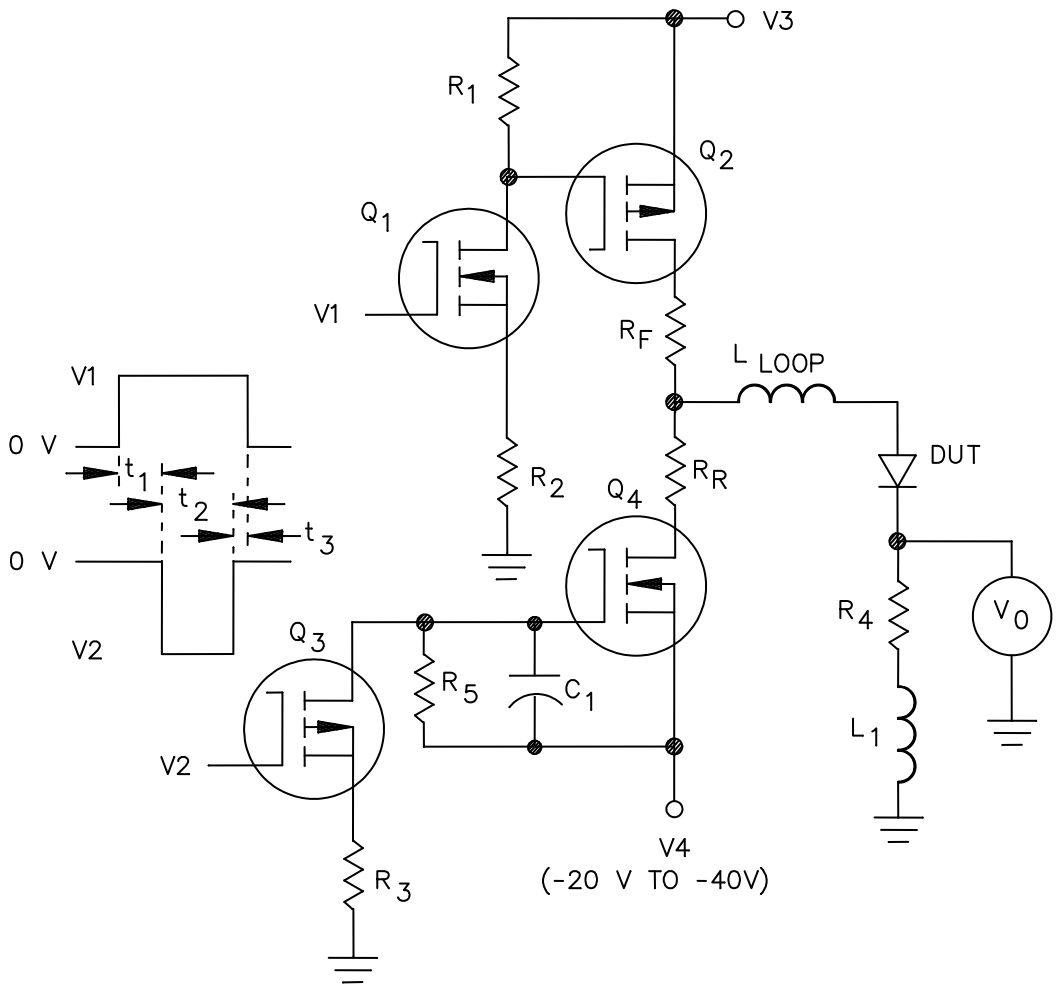
Designation (condition)		B1	B2	B3	B4	B5
Test current, (amperes) (see figure 4031–5)	I_F	0.5	0.5	1.0	1.0	0.01
	I_{RM}	1.0	0.5	1.0	1.0	0.01
	$i_{R(REC)}$	0.25	0.1	0.5	0.1	0.005
Circuit resistor 1/ (ohms)	R_F	33	33	50	50	1,200
	R_R	9	9	15	15	200
	R_4	1.00	1.00	1.00	1.00	10.0

1/ Preferred nominal resistance values are shown; modification of R_F and R_R may be needed to achieve the rise time of 4.1.a and the I_{RM} specified.

4.1 Circuit notes for condition B. The timing and test circuit on figure 4031–3 is only a guide for the pulse method shown to switch the DUT. Equivalent circuits or equivalent commercial equipment may be used with approval of the qualifying activity. Duty factor shall be 5 percent maximum to minimize heating effects.

a. The rise time of the reverse voltage pulse across a noninductive calibration resistor in place of DUT shall be less than 20 percent of the recovery time of the DUT.

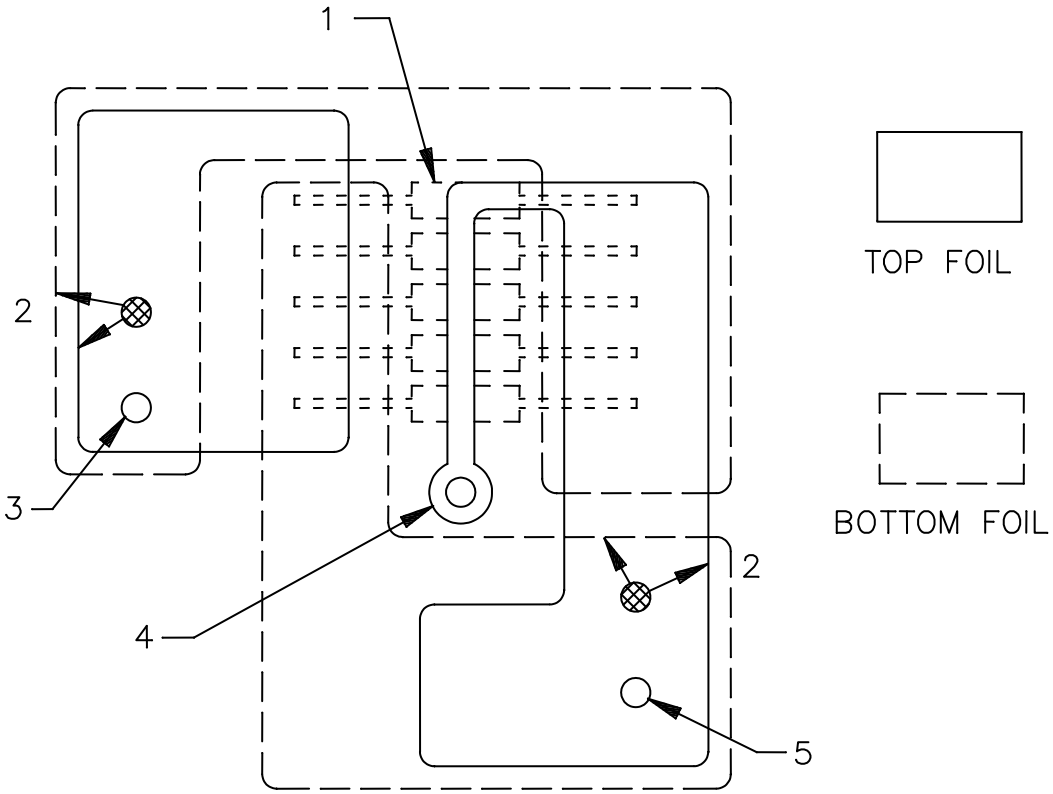
b. The oscilloscope rise time shall be less than 50 percent of the pulse generator rise time.



V_3 and R_F control forward current I_F.
V_4 and R_R control reverse current I_{RM}.
$t_{rr(max)}$ is the longest to be measured.
$t_{rr(min)}$ is the shortest expected.

$t_1 > 5\ t_{rr(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{rr(min)}/10$.
(L_1 is the self inductance of R_4)

FIGURE 4031–3. Test circuit for condition B.



NOTES:

1/ Resistor assembly R_4 may consist of 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L to R (⟶) is opposite to top current flow R to L (⟵), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.

2/ Cross hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.

3/ To ground of circuit and probe.

4/ To center conductor of miniature probe jack.

5/ To cathode of DUT.

NOTE: Parasitic inductance in the test fixture or in the sampling resistor R_4 of the test circuit on figure 4031–3 can distort or shorten the reverse recovery time giving misleading results of the DUT. To minimize parasitic inductance, the figure above (4031–4) provides a suggested configuration for R_4.

FIGURE 4031–4. Suggested board layout for low L_1/R_4 for condition B.

4.2 Procedure for test condition B. Specified forward current (I_F) shall be adjusted by varying positive voltage, V_3. Reverse current (I_{RM}) shall be controlled by varying the negative voltage, V_4 (see figure 4031–5). With the DUT in place the circuit shall be capable of higher than specified I_{RM}; the circuit, and not the diode, must limit I_{RM}.

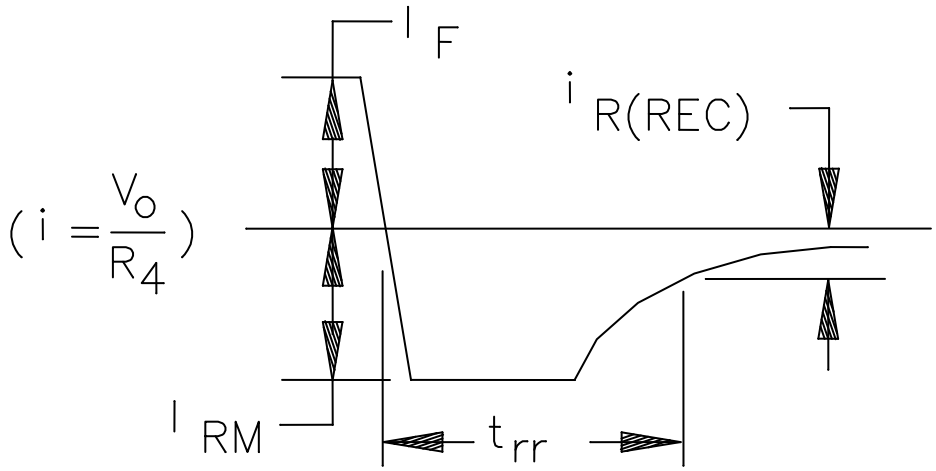


FIGURE 4031–5. Current through DUT (condition B).

4.3 Summary for test condition B.

a. The following conditions shall be specified in the applicable specification sheet.

(1) Test condition (e.g., B1, B2) (see 3.) If not in table 4031–I, specify c, d, and e.

(2) Ambient temperature, if other than +25°C.

(3) Forward current, I_F.

(4) Reverse current, I_{RM}.

(5) Load resistances R_F and R_R.

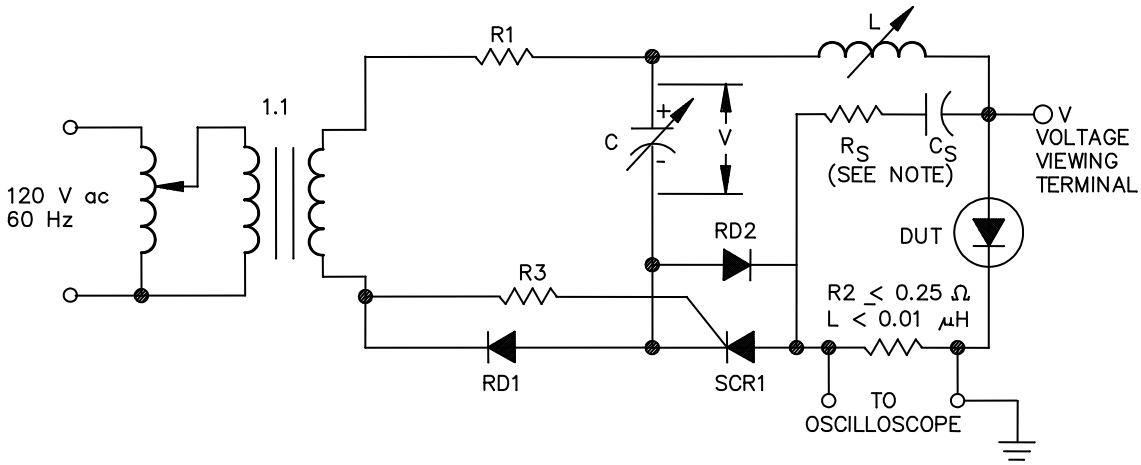
(6) Recovery measuring point, $i_{R(REC)}$.

NOTE: Specify c through f, only if not a condition designation in table 4031–I.

b. The following measurement shall be made:

(1) t_{rr} (see figure 4031–5).

5. Test condition C. This test is intended for high current rectifiers with reverse recovery times equal to or greater than 350 ns and tested with peak forward currents equal to or greater than 10 amperes. See figure 4031–6.



NOTE: R_S and C_S are snubber components, when their use is specified

FIGURE 4031–6. Circuit for measuring reverse recovery characteristics (condition C).

5.1 Circuit notes for test condition C

a. The circuit is designed to simulate the commutation duty encountered in power rectifier diode circuits while also keeping average power dissipation low to minimize the need for thermal management.

b. The resistance of the C, L, and DUT loop (R_2 and parasitics) is small, e.g., $2\pi\sqrt{L/C}$ much greater than R so the test current will essentially be sinusoidal, possessing a width of $\pi\sqrt{LC}$ a di/dt of V/L and a peak value of $V/\sqrt{L/C}$. The peak voltage across the capacitor shall be as small as practicable to achieve the desired test conditions. The effects of reverse voltage magnitude on the test device recovery characteristics are neglected.

c. The minimum forward current pulse time (t_p) shall be at least five times the recovery time (t_{rr}) of the DUT so that the di/dt will be linear and of the same value before and after current reversal.

d. The oscilloscope rise time shall be less than 20 percent of t_a or t_b (see figure 4031–7), whichever is less.

e. The inductance of the current viewing resistor shall be extremely low, e.g., 0.01 micro Henry. Abrupt recovery rectifiers (figure 4031–7) can cause current oscillations which may be reduced by using a lower inductance current viewing resistor and by properly terminating the oscilloscope cable. A current transformer ~~/~~ with suitable rise time may be substituted for the current viewing resistor 1/. Rectifier diode RD2 provides a very low inductance path around SCR1 if the reverse recovery time of SCR1 is shorter than that of the DUT. An external SCR triggering source may be required to achieve stable triggering.

f. A slight oscillation may appear on the waveform following device recovery. This may be reduced by lowering the current viewing resistor's inductance, or properly terminating the viewing cable. The oscillation, however, does not affect the test results.

g. D_2 and its circuit branch should provide a very low inductance path around the SCR if the reverse recovery time of the SCR is shorter than that of the DUT.

h. R_3 shall be sufficiently large such that the SCR triggers only after the capacitor, C, has had ample time to charge to its desired value. If stable triggering or ample charging is a problem, a momentary pushbutton switch may be inserted in line with R_3 to provide triggering. A pulse transformer technique is also acceptable in the triggering circuit.

NOTE: Pearson Electronics, Inc. or equivalent types.

5.2 Procedure for test condition C. C, L, and V are adjusted to obtain the specified test current di/dt and magnitude, I_{FM}. The recovery time for rectifier diodes is defined as $t_{rr} = t_a + t_b$ (see figure 4031–7), t_a is measured from the instant of current reversal to the instant that current reaches its peak reverse value $I_{RM(REC)}$ and t_b is measured from $I_{RM(REC)}$ to the instant the straight line connecting $I_{RM(REC)}$ and 0.25 $I_{RM(REC)}$ intercepts the zero current axis. The recovery time for devices with abrupt recovery characteristics is defined in the same manner except t_b is measured from $I_{RM(REC)}$ to the instant the test current waveform intercepts the zero current axis, if applicable.

5.3 Summary for test condition C.

a. The following conditions shall be specified in the applicable specification sheet:

(1) Case temperature in °C.

(2) Test repetition rate, in Hz.

(3) Peak forward current, I_{FM}, in amperes.

(4) Rate of decrease of forward current, di/dt, in A/μs.

(5) Minimum test current pulse width, tp, in microseconds. (Duty cycle shall be ≤ one percent to minimize heating effects).

b. The following characteristics shall be specified for measurement in the applicable specification sheet as required:

(1) Reverse recovery time (defined as $t_{rr} = t_a + t_b$), t_a, t_b.

(2) Reverse recovery current, $I_{RM(REC)}$, in amperes.

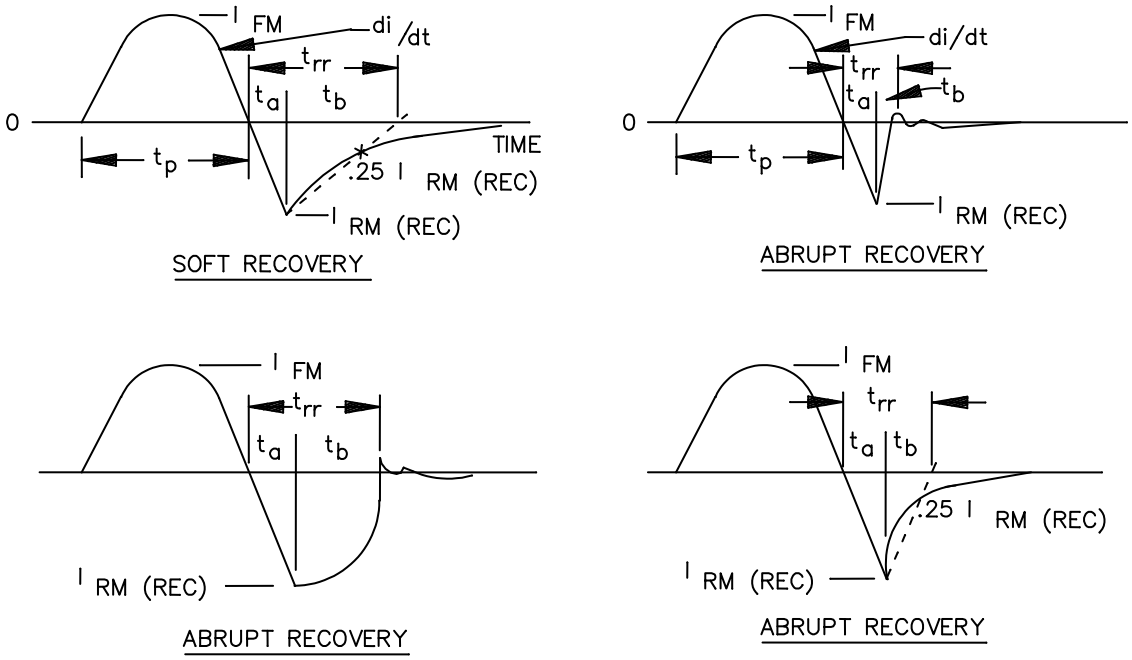


FIGURE 4031–7. Test current waveforms for various types of rectifier diodes under test in the circuit for measuring reverse recovery characteristics.

6. Test condition D. (See suggested conditions in table 4031–II, e.g., D1, D2, D3) This condition is intended for ultra-fast medium current rectifiers (axial and case mount, or equivalent styles) measured at $I_F \geq 1A$ and with reverse recovery time ≤ 100 ns. With good engineering practice, condition D can adequately measure t_{rr} down to about 10 ns; it can also utilize I_f up to at least 10 A.

TABLE 4031–II. Test condition D.

Device ratings		Designation (condition)	Values for testing	
I_O or I_F (AV) (A)	t_{rr} (ns)		I_F (A)	di/dt (μ/s)
1 to 4	> 65 to 100	D1	2	100
to 20	> 65 to 100	D2	6	100
over 20	> 65 to 100	D3	10	100
1 to 4	≤ 65	D4	2	200
to 20	≤ 65	D5	6	200
over 20 1/	≤ 65	D6	10	200

1/ For devices with substantially higher rated current, it is desirable to use test conditions for I_F close to rated current, and higher values of di/dt.

6.1 Test circuit for condition D. Refer to figures 4031–8 and 4031–9 for timing and circuit details. Equivalent circuits or approved commercial equipment may be used. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced with any functionally equivalent circuit. Likewise, the current-ramp generator consisting of Q_3, Q_4, R_3, and C_1. The duty factor shall be ≤5 percent to minimize heating effects.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, e.g., short leads, good ground plane, minimum inductance of the measuring loop, and minimum self-inductance (L_1) of the current sampling resistor (R_4). Also, appropriate high speed generators and instruments shall be used.

b. The measuring-loop inductance (L_{LOOP}, see figure 4031–8) represents the net effect of all inductive elements, whether lumped or distributed, e.g., bonding wires, test fixture, circuit board foil, or inductance of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics including C_T, determines the value of t_b.

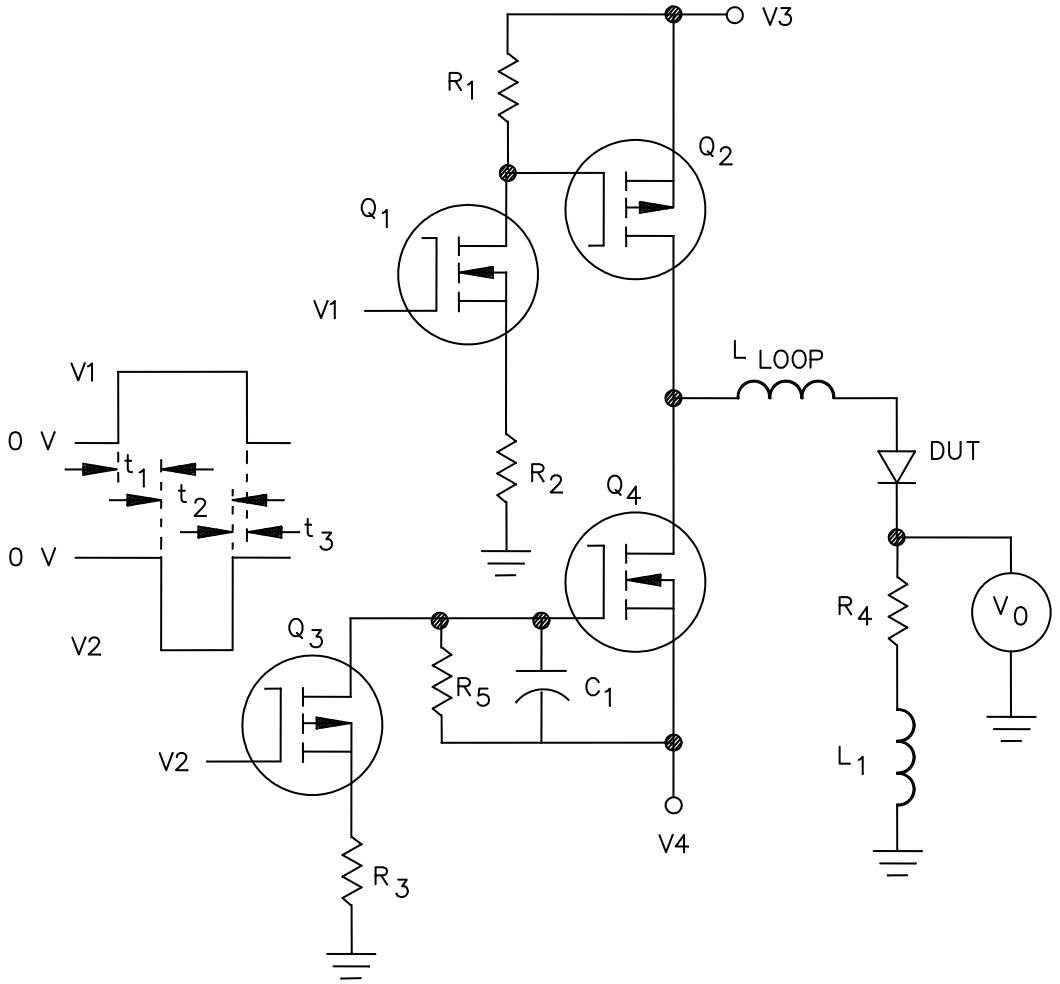
c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with $R_{LOOP} < 2\pi\sqrt{L/C}$ where $L = L_{LOOP}$. That is another reason for minimizing L_{LOOP}.

d. Regarding breakdown voltage, $-V_4$ should be kept as low as practicable, especially when test low voltage devices. A value of approximately 30 volts is recommended.

e. The time constant of the self-inductance of the current-sample resistor R_4 (see figure 4031–9) shall be kept low relative to t_a because the observed values of t_a and $I_{RM(REC}$ increase with increasing self-inductance. Since the value of R_4 is not specified, the recommended maximum inductance is expressed as a time constant (L_1/R_4) with a maximum value of t_a (minimum)/10, where t_a (minimum) is the lowest t_a value expected. This ratio was chosen as a practical compromise and would yield an observed t_a, which is 10 percent high ($\Delta t_a = L_1/R_4$). The $I_{RM(REC}$ error is a function of the L_1/R_4 time constant and di/dt. For a di/dt of 100 A/μs the observed I_{RM} would also be 10 percent high. $\Delta I_{RM} = L_1/R_4$ di/dt.

f. The di/dt of 100 A/μs was chosen so as to provide reasonably high signal levels and still not introduce the large I_{RM} errors caused by higher di/dt. Higher values of di/dt, without large errors, can be achieved with lower L_1/R_4.

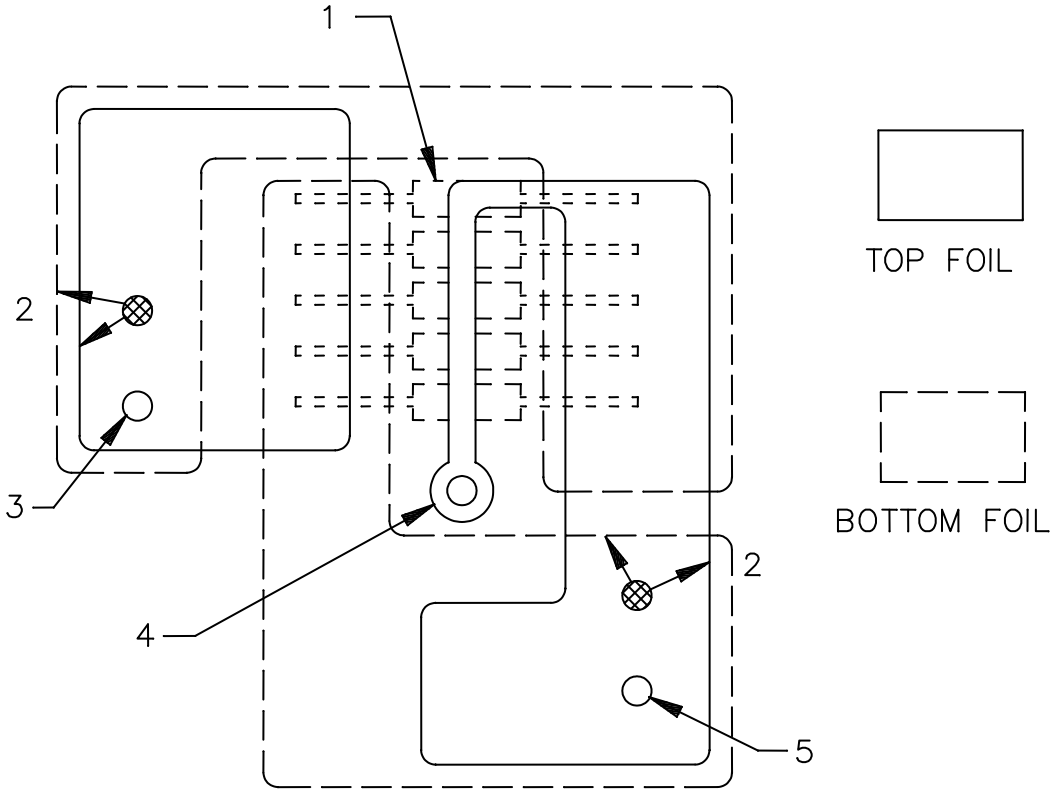
6.2 Procedure for test condition D. Adjust V_1 for the specified forward current, I_F. Adjust $-V_2$ for the specified di/dt (see figures 4031–8 through 4031–10).



V_1 amplitude controls forward current (I_F).
V_2 amplitude controls di/dt.
$t_{a(max)}$ is the longest t_a to be measured.
$t_{a(min)}$ is the shortest t_a to be measured.

$t_1 > 5\ t_{a(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{a(min)}/10$.
L_1 is the self inductance of R_4.

FIGURE 4031–8. Test circuit for condition D.



NOTES:

1. Resistor assembly R_f is made from 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L or R (⟶) is opposite to top resistor current flow R to L (⟵), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Crosses hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 4031–9. Suggest board layout for low L_1/R_4 for test condition D.

6.3 Summary for test condition D.

a. The following conditions shall be specified in the applicable specification sheet:

(1) Designation (condition, see table 4031–II). If another is desired, 4 and 5 herein shall be specified. If another is desired, d and e shall be specified.

(2) $-V_4$, reverse ramp power supply voltage.

(3) T_C, case temperature, if other than +25°C.

(4) I_F, .25 (minimum) of the continuous rated current is the suggested alternative (see table 4031–II).

(5) di/dt, 100 A/µs is the suggested alternative (see table 4031–II).

b. The following characteristics shall be specified for measurement:

(1) Reverse recovery time, t_{rr} (see figure 4031–10).

(2) $I_{RM(REC)}$ (see figure 4031–10).

NOTE: An additional measurement, t_a may be made if desired to compute $t_b = t_{rr} - t_a$, and the recovery softness factor, RSF = t_b / t_a.

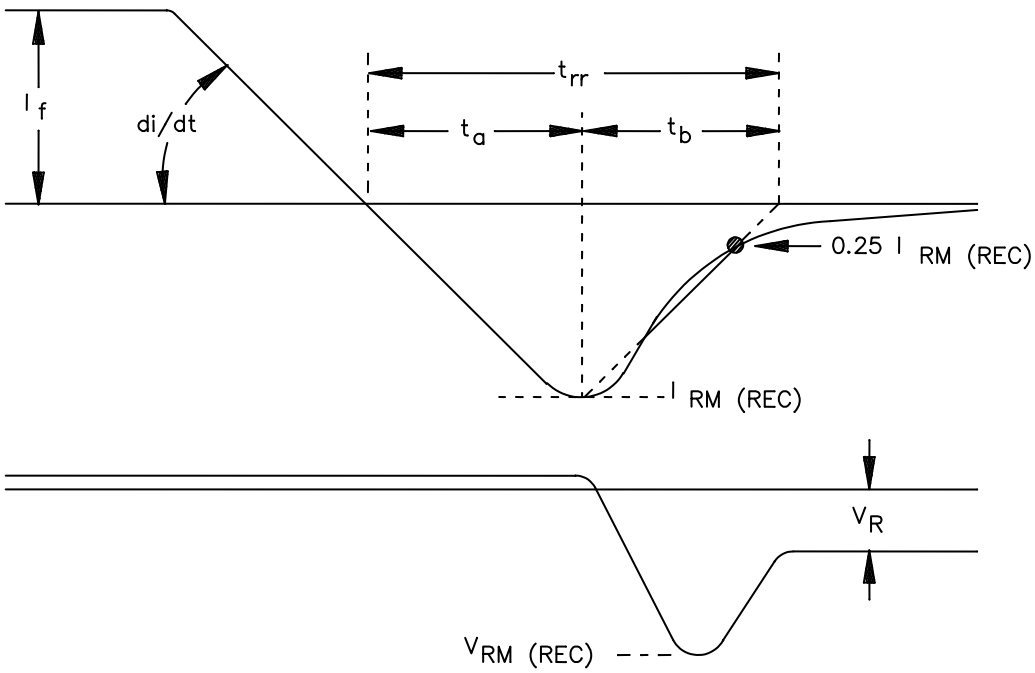


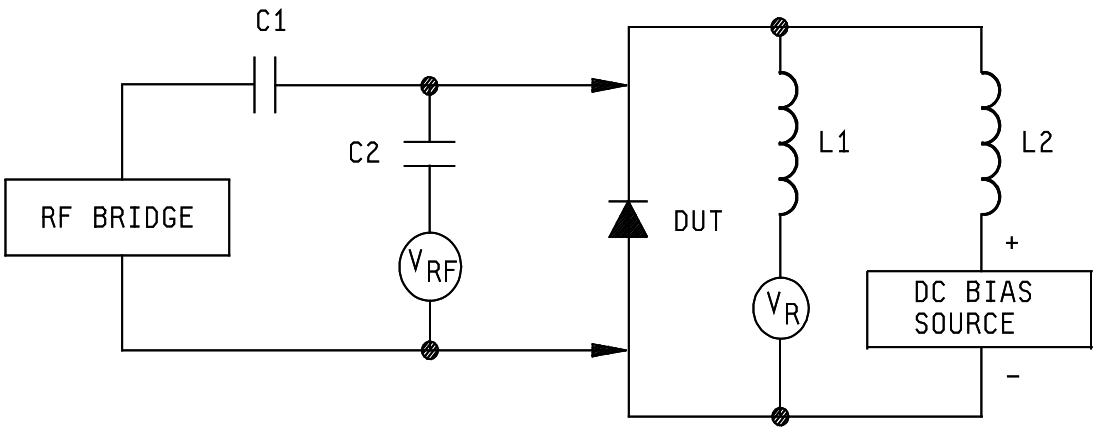
FIGURE 4031–10. Generalized reverse recovery waveforms for test condition D.

METHOD 4036.1

QUALITY FACTOR (Q) FOR VOLTAGE VARIABLE CAPACITANCE DIODES

1. Purpose. The purpose of this test method is to measure the quality factor (Q) of the device. By definition, Q expresses the ratio of reactance to effective resistance of the device, under RF signal conditions and specified dc bias conditions.

2. Test circuit. See figure 4036-1.



NOTE: The impedance of C1, C2, and L1, L2 shall be small and large, respectively, compared to the DUT at the frequency of measurement.

FIGURE 4036–1. Test circuit for measuring Q.

3. Procedure. The test equipment shall be connected as shown on figure 4036–1. The dc bias supply shall be adjusted for the specified voltage where Q is to be measured. Unless otherwise specified, the RF level shall be adjusted to 50 mV (rms). The parallel resistance Rp and capacitance Cp of the test device shall be measured using RF bridge methods. Unless otherwise specified, the point of measurement shall be .062 inch (1.57 mm) from the device body. Q shall be calculated using the following formula: $Q = 2\pi fRpCp$.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test frequency.

b. Reverse dc bias (V_R).

c. RF level if other than 50 mV (rms).

d. Required Q.

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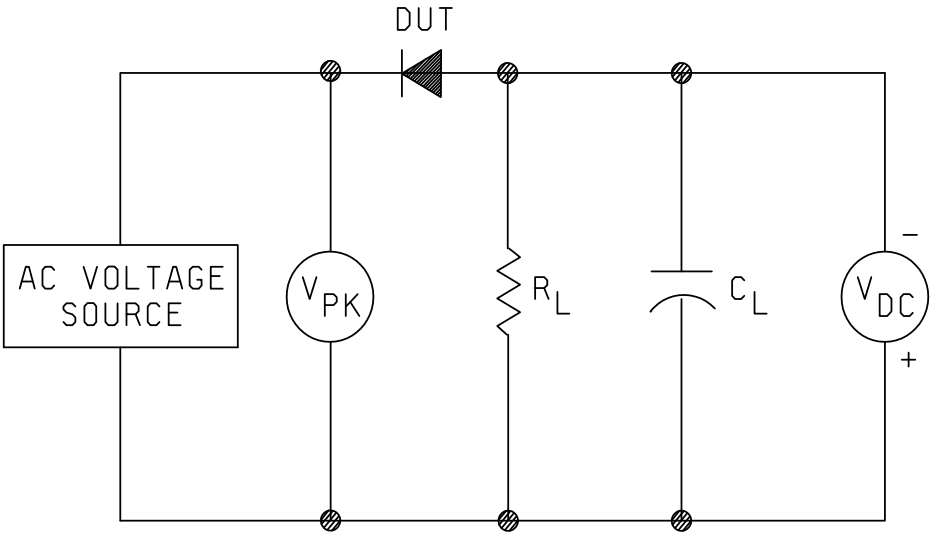
METHOD 4041.2

RECTIFICATION EFFICIENCY

1. Purpose. The purpose of this test method is to measure rectification efficiency which is the ratio of dc output voltage to peak ac input voltage.

2. Test circuit. See figure 4041–1.



NOTE: The voltmeter shall have a high impedance as compared with the load circuit of R_L and C_L.

FIGURE 4041–1. Test circuit for rectification efficiency.

3. Procedure. The ac signal shall be adjusted to the specified frequency and signal level measured by means of peak reading voltmeter (V_{pk}). The rectified output voltage shall be measured by means of voltmeter (V_{DC}).

$$\text{Rectification efficiency (\%)} = \frac{V_{DC}}{V_{pk}} \times 100$$

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Load capacitor (C_L) and load resistor (R_L).

b. Frequency and amplitude of ac source.

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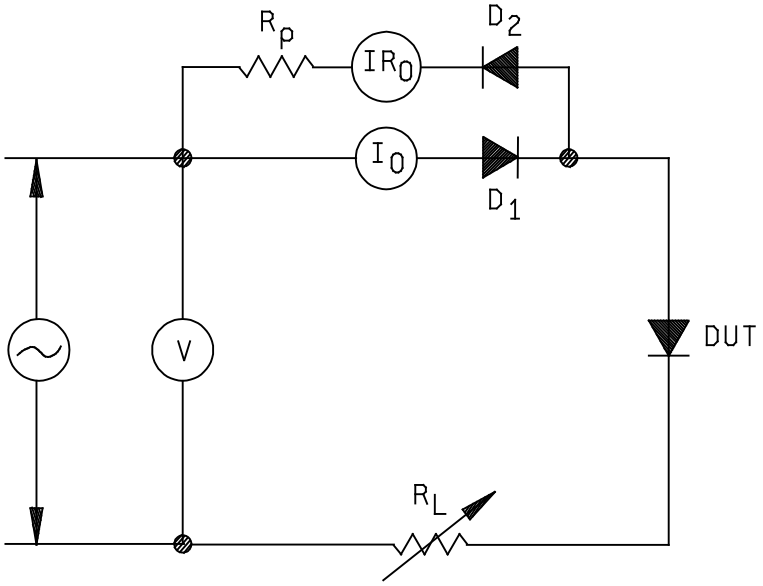
METHOD 4046.1

REVERSE CURRENT, AVERAGE

1. Purpose. This test method is designed to measure the average reverse current through the device under the specified conditions.

2. Test circuit. See figure 4046–1.



NOTE: The reverse leakage current at each device D_1 and D_2 shall be less than .05 percent of the maximum allowable specified leakage current of the DUT. In other respects, the devices D_1 and D_2 should be of the same type as the DUT.

FIGURE 4046–1. Test circuit for reverse current, average.

3. Procedure. After thermal equilibrium, at the temperature specified, the specified voltage shall be applied.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test temperature, when required (see 3).

b. Test voltage (see 3).

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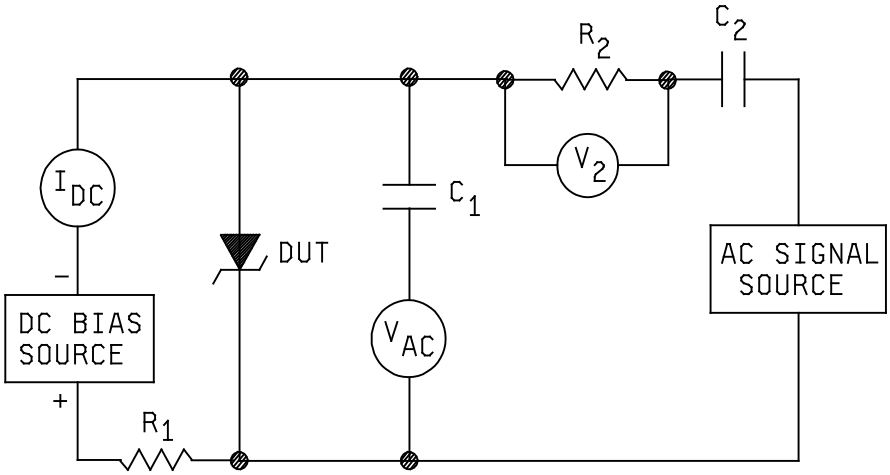
METHOD 4051.3

SMALL-SIGNAL REVERSE BREAKDOWN IMPEDANCE

1. Purpose. The purpose of this test is to measure the reverse breakdown impedance of the device under small-signal conditions.

2. Test circuit. See figure 4051–1.



NOTES:
1. The impedances of C_1 and C_2 shall be small compared to the DUT at the test frequency.
2. Voltmeters V_{AC} and V_2 shall be high input impedance rms types.
3. The resistance of R_1 shall be large compared with the breakdown impedance being measured.
4. A low pass filter may be installed in series with the ac signal source.

FIGURE 4051–1. Test circuit for small-signal reverse breakdown impedance.

3. Procedure. The specified reverse direct current shall be applied to the DUT. An ac signal in the frequency range of 45 through 1,000 Hz shall be applied to the DUT through coupling capacitor C_2. Associated specification limits for Z_{ZT} shall apply at 45 through 60 Hz. Tests at frequencies greater than 60 Hz shall be corrected to those readings taken at 45 through 60 Hz. This current shall be 10 percent of the value of the dc breakdown current through the DUT. The small-signal impedance shall be determined as follows:

$$Z_{ZT} = \frac{V_{(RMS)}}{I_{(RMS)}} = \frac{V_{AC}\, R_2}{V_2}$$

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. DC and ac test currents.

b. Test frequency, if other than 45 to 1,000 Hz.

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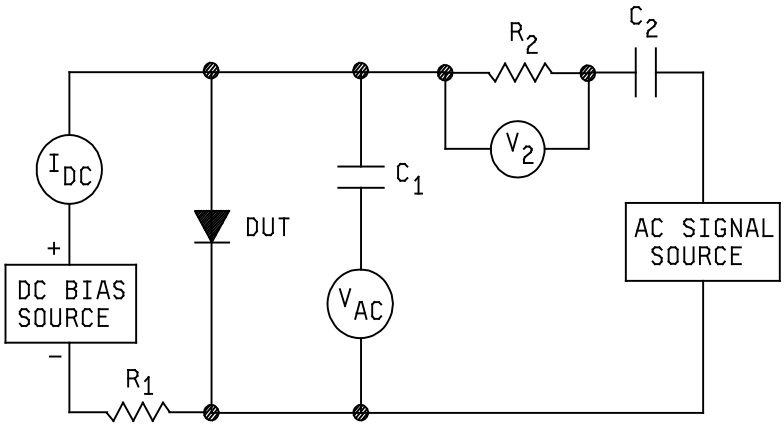
METHOD 4056.2

SMALL-SIGNAL FORWARD IMPEDANCE

1. Purpose. The purpose of this test method is to measure the forward impedance of the device under small-signal conditions.

2. Test circuit. See figure 4056–1.



NOTES:
1. The impedances of C_1 and C_2 shall be small compared to the DUT at the test frequency.
2. Voltmeters V_{AC} and V_2 shall be high input impedance types.
3. The resistance of R_1 shall be large compared with the forward impedance being measured.
4. A low pass filter may be installed in series with the ac signal source.

FIGURE 4056–1. Test circuit for small-signal forward impedance.

3. Procedure. The specified forward direct current shall be applied to the DUT. An ac signal in the frequency range of 45 through 1,000 Hz shall be applied to the DUT through coupling capacitor C2. associated specification sheet limits for Z_f shall apply at 45 through 60 Hz. Tests at frequencies greater than 60 Hz shall be corrected to those readings at 45 through 60 Hz. This current shall not be greater than 10 percent of the value of the dc forward current I_f. The small-signal impedance shall be determined as follows:

$$Z_f = \frac{V_{(RMS)}}{I_{(RMS)}} = \frac{V_{AC} R_2}{V_2}$$

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. DC and ac test currents.

b. Test frequency, if other than 45 to 1,000 Hz.

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METHOD 4061.1

STORED CHARGE

1. Purpose. The purpose of this test method is to measure directly the charge recovered from a semiconductor diode when it is rapidly switched from a forward biased condition to a reverse biased condition.

2. Test circuit. See figure 4061–1.

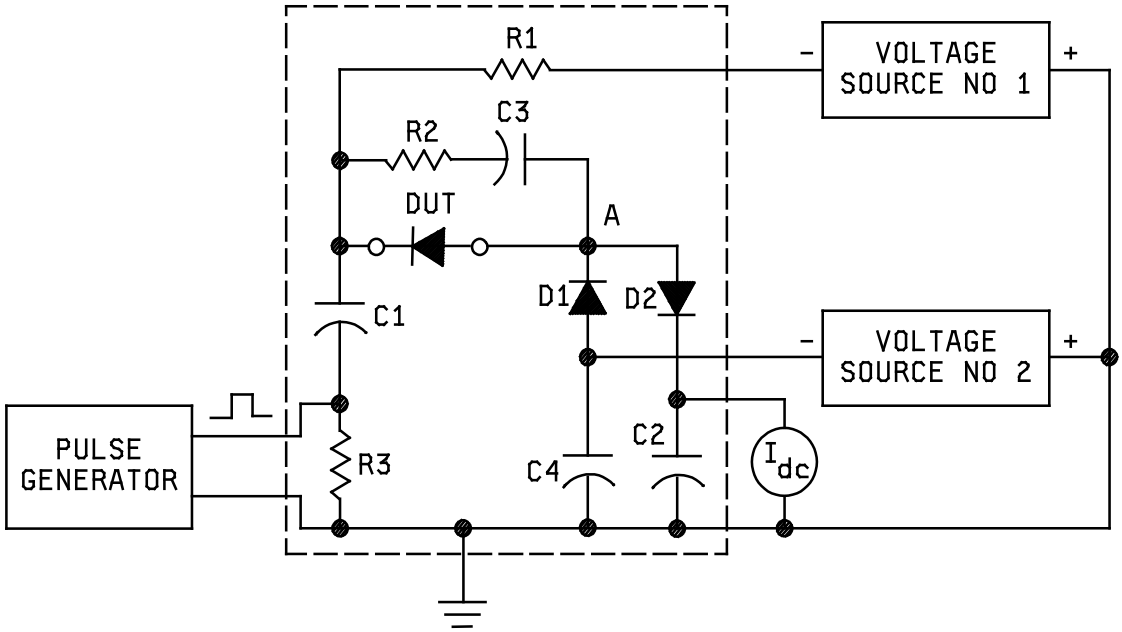

FIGURE 4061–1. Test circuit for stored charge.

3. Test precautions.

a. The diode under test is forward biased by the current flowing from voltage source number 2 through diode D1 and through resistor R1 to voltage source number 1. The diode under test is periodically reverse biased by the pulse from the generator and the charge stored in the diode is caused to flow through diode D2 and is measured on the current meter. A similar measurement is made at zero bias current to determine the component of charge resulting from the diode capacitance and the stray circuit capacitance. The stored charge can then be computed from the current readings and the pulse frequency.

b. Resistor R1 should be large enough to ensure a constant current through the diode under test. Capacitor C1 should be large enough to maintain a nearly constant voltage across the diode under test during the pulse. The output impedance of the pulse generator including R3 should have a low value, preferably 10 to 25 Ω. The rise time of the pulse should be short enough and the pulse length should be long enough so that further change will not alter the measurement results.

c. Diode D1 should have a much smaller stored charge than the diode under test. Diode D2 should have a fast turn on time, a low dynamic resistance at high currents, and a low reverse leakage current. Capacitors C2 and C4 should have low inductance and should be of sufficient capacitance so that a further increase in their values would not alter the measurement results. The current meter should be of sufficiently low impedance that the average voltage drop across it during any test does not exceed 10 millivolts. Capacitor C3 should be of sufficient size that a small current will flow through the current meter with the diode under test removed. Resistor R2 should have approximately the same value as the output impedance of the pulse generator.

d. The portion of the circuit within the dotted lines should be constructed in accordance with good practices for high speed pulse circuits. Particular attention should be paid to minimizing the circuit inductance including the connections to the diode under test. The capacitance between point A and ground should be made as small as possible.

4. Test procedure.

a. Adjust the pulse generator for the desired amplitude, pulse width, and frequency (f). Set voltage source one to zero. Insert the diode under test and adjust voltage source two for the specified voltage from point A to ground as measured on a high impedance voltmeter. A common value used for this voltage is –0.6 volts. Read the current, I_1, flowing through the current meter.

b. Set voltage source one for the specified forward current through the diode under test. Adjust voltage source two for the specified voltage from point A to ground. This voltage must be the same as used in 3.a. Read the current, I_2, flowing through the current meter.

c. The stored charge is given by:

$$Q_S = \frac{I_2 - I_1}{f}$$

5. Summary. The following conditions shall be included in the applicable performance specification sheet or acquisition document:

a. The bias current I_f at which the stored charge measurement is made (see 4).

b. Pulse generator rise time (1 percent to 50 percent), amplitude, width, impedance, and frequency (see 4).

METHOD 4064.1

INDUCTIVE AVALANCHE ENERGY TEST FOR DIODES

1. Purpose. The purpose of this test method is to determine the avalanche capability of diodes and rectifiers. The intent of the test is to stress the termination of the device.

2. Scope. This test method is intended as a test for avalanche rated Schottky rectifiers but it may also be applied to other avalanche rated diodes if applicable.

3. Circuitry. The circuit shall be designed so that all stray reactances are held to a minimum.

4. Symbols and definitions. The following symbols and terminology apply to this test method:

a. E_{AS}: Non-repetitive avalanche energy, minimum.

b. I_{AS}: Non-repetitive avalanche current, maximum.

c. L: Load inductance in accordance with device under test.

d. P_D: Power dissipation of device.

e. R_S: Stray circuit resistance.

f. I_{LPK}: Peak inductor current.

g. $V_{(BR)DUT}$: Breakdown or avalanche voltage of device under test.

h. V_{DD}: Power supply voltage.

i. t_{AV}: Time in avalanche.

5. Procedure.

5.1 Screening. The DUT must be screened prior to avalanche and meet all specified parameters.

5.2 Calculations. The energy delivered to the DUT can be calculated as follows:

a. For figure 4064–1 (test circuit 1):

$$E_{AS} \approx \frac{I}{2} * L * I_{LPK}^{2} * \left(\frac{V_{(BR)DUT}}{V_{(BR)DUT} - V_{DD}} \right)$$

NOTE: $R_S \neq 0$

b. For figure 4061–3 (test circuit 2):

$$E_{AS} \approx \frac{I}{2} * L * I_{LPK}^{2}$$

NOTE: It is assumed that R_S = 0 for these calculations.

5.3 Test circuit 1.

5.3.1 Circuit layout. The circuit shown below is typical for unclamped inductive switching. In this circuit design the V_{DD} power supply may contribute to the total energy transferred to the diode if its value is not small compared to the $V_{(BR)}$ of the device under test. The calculation of the energy shall include the transfer from the V_{DD} supply when the ratio of $V_{(BR)DUT}$ over V_{DD} is less than 10, which is calculation (a) in section 5.2.

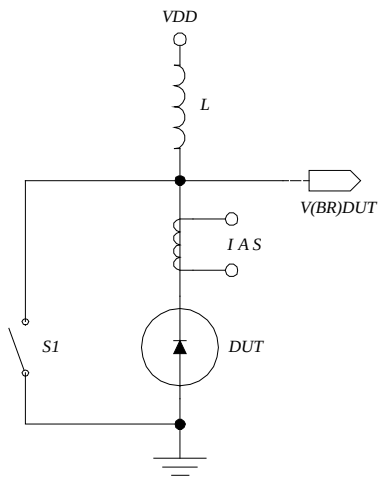

FIGURE 4064–1. Test circuit 1.

5.3.2 Switch. Switch S1 is normally a power semiconductor, such as a MOSFET but the breakdown voltage of this device must be greater than that of the device under test.

5.3.3. Transformer. A current transformer or probe should be used to monitor the avalanche current of the device. This probe must be mounted in either the cathode or anode leg of the device under test.

5.3.4 Inductance. The value of inductance (L) for the load should be selected to keep the time in avalanche (t_{AV}) below 200 µs. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance (L), which will lead to non-repeatable test results.

$$t_{AV} \approx \frac{L * I_{LPK}}{V_{(BR)DUT}}$$

5.3.5 Test circuit 1 response. The current and voltage waveform below shows typical response of a device in this test circuit.

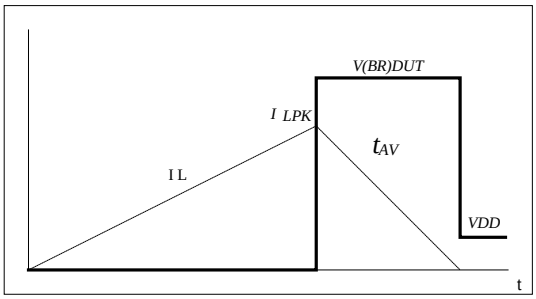

FIGURE 4064–2. Test circuit 1 response.

5.4 Test circuit 2.

5.4.1 Circuit. The circuit shown below is also applicable for unclamped inductive switching. In this circuit design the V_{DD} power supply is removed from the test circuit via S1 after the inductive load is fully charged. The calculation of the energy does not need to include the transfer from the V_{DD} supply when using this test circuit, which is calculation (b) in section 5.2.

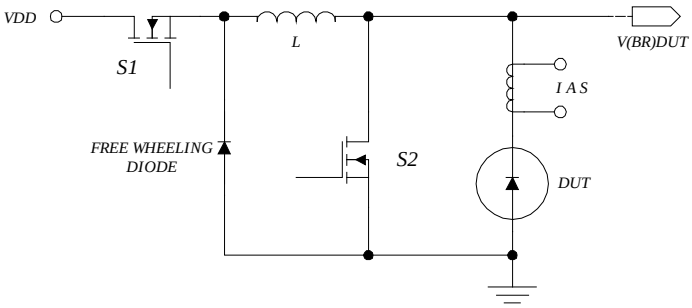

FIGURE 4064–3. Test Circuit 2.

5.4.2 Switches. Switches S1 and S2 are a power semiconductors, such as MOSFETs but the breakdown voltages of the devices must be greater than that of the device under test. These devices are switched off simultaneously in order to achieve the proper response on the device under test.

5.4.3 Diode. The free wheeling diode is required to close the current loop for the inductive load after S1 opens the connection to the V_{DD} power supply. The breakdown voltage of the free-wheeling diode shall be greater than that of the DUT.

5.4.4 Probe. A current transformer or probe should be used to monitor the avalanche current of the device. This probe must be mounted in either the cathode or anode leg of the device under test.

5.4.5 Inductors. The value of inductance (L) for the load should be selected to keep the time in avalanche (t_{AV}) 200 µs. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance (L), which will lead to non-repeatable test results.

$$t_{AV} \approx \frac{L * I_{LPK}}{V_{(BR)DUT}}$$

5.4.6 Waveform. The current and voltage waveform below shows typical response of a device in this test circuit.

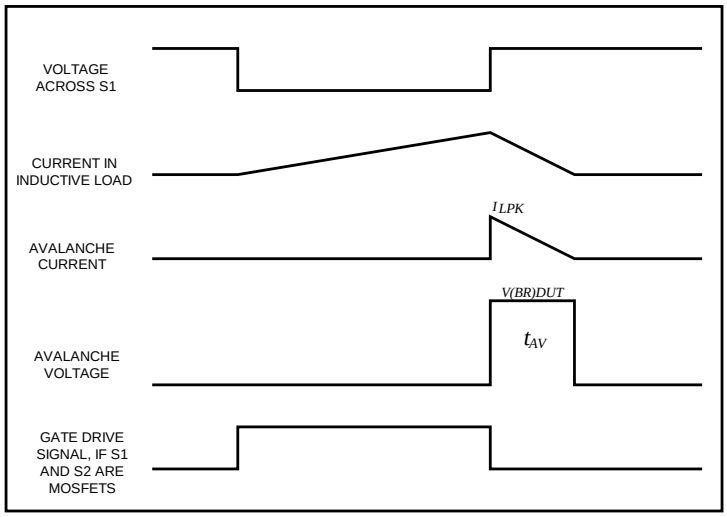

FIGURE 4064–4. Test Circuit 2 response.

6. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. E_{AS}: Non-repetitive avalanche energy, minimum (joules).

b. I_{AS}: Non-repetitive avalanche current, maximum (amperes).

c. V_{DD}: Power supply voltage, minimum (V).

d. L: Load inductance minimum (µH or nH) or optionally calculated from the formula.

e. Initial case, lead or end cap temperature: +25°C +10°C /-5°C, unless otherwise specified.

f. Number of pulses to be specified: 1 pulse minimum, unless otherwise specified.

7. Failure criteria. The DUT shall be tested and be within all specified static parametric limits at the completion of the test. Any DUT that failed to meet any of the post I_{AS}/E_{AS} electrical parametric limits is considered an avalanche energy test failure.

METHOD 4065

PEAK REVERSE POWER TEST

1. Purpose. This describes a test method for subjecting the device under test (DUT) to a high power stress condition in the reverse direction of rectifiers to determine the ability of the device to withstand a specified peak reverse power. This is intended to verify reverse power stress capabilities by various test conditions. Each condition is considered nonrepetitive where there is sufficient time between their applications to permit the device temperature to return to its original value before it may be repeated.

2. Applicability. A current impulse is applied for 20 µs that will provide a constant level of power in the reverse direction of the rectifier. This test method also utilizes a monitoring circuit to sense voltage for determination of power and possible voltage collapse during the current impulse.

3. Definitions. The following symbols and terms shall apply for the purpose of this test method.

a. I_{RSM}: Nonrepetitive reverse surge current (in Amps)

b. $v_{(BR)}$: Breakdown voltage (instantaneous value [in Volts])

c. $V_{(BR)}$: Minimum rated breakdown voltage (in Volts)

d. P_{RSM}: Reverse power nonrepetitive peak (in Watts)

e. d.f.: Duty factor = 100 t_p/ t_{rep} (percentage)

f. t_P: Duration of current surge pulse (in ms or µs).

4. Reverse power test of rectifiers.

4.1 Apparatus. A simplified circuit is shown on figure 4065–1 where the current source (I) and switch (SW1) combination shall apply the peak value of current pulse I_{RSM} for the pulse duration of 20 µs as required (see figure 4065–2). The rise and fall times of the pulse shall be less than 10 percent of the pulse duration and the I_{RSM} will not vary during the impulse by more than 10 percent. The DUT shall also be monitored during the pulse using an oscilloscope to verify the instantaneous $v_{(BR)}$ voltage. The monitored $v_{(BR)}$ will typically increase during the 20 µs impulse from heating effects as shown on figure 4065–3. The $v_{(BR)}$ may also simply be monitored at the end of the pulse duration by a gated switch (SW2) or other automated methods to determine its highest value and also ensure the $v_{(BR)}$ has not collapsed below the rated minimum breakdown voltage V_{BR} of the rectifier from excessive heat. Although a simplified circuit is depicted, there are other more automated test equipment (ATE) methods that can also accomplish this such as the Frothingham RE20A, B, or C as well as a FEC200 tester with a separate dual monitor oscilloscope for both current and voltage.

4.2 Procedure. No current is applied to the DUT prior to the starting time (t_O) of the test. At t_O, SW1 applies I_{RSM} for 20 µs after which SW1 causes the current to cease flowing in the DUT.

a. Apply a specified rectangular impulse level of current I_{RSM} as shown on figure 4065–2. The rectangular impulse may decline slightly to optimize a constant peak reverse power level (P_{RSM}) since the $v_{(BR)}$ will increase due to heating effects and positive temperature coefficient during the 20 µs impulse. This impulse shall control the effective power to within 10 percent during the impulse duration. The DUT is also monitored for the response in reverse voltage $v_{(BR)}$.

b. If testing to a specific peak reverse power (P_{RSM}) requirement, the current (I_{RSM}) will be increased to the level where the calculated P_{RSM} level meets or exceeds the requirement. The P_{RSM} value is determined with the average I_{RSM} and $v_{(BR)}$ values where $P_{RSM} = I_{RSM} \times v_{(BR)}$. These average values typically occur at 10 µs or half way into the 20 µs impulse

NOTE: The test may need to be repeated to achieve the desired power level after the initial $v_{(BR)}$ is determined. If repeated, the time between pulses shall be sufficient to permit the DUT temperature to return to its original value.

c. If it is noted that the $v_{(BR)}$ collapses below the minimum rated breakdown voltage $V_{(BR)}$ during the testing in 4.2.a and 4.2.b, this is considered a failure to the applied P_{RSM} level.

d. Electrical measurements shall also be performed after each reverse power test to ensure the DUT has not permanently degraded. As a minimum, this shall include verification the reverse current (I_R) does not exceed its maximum specified value at the rated voltage V_R for the DUT. Although a device can collapse in 4.2.c without permanently degrading, such a collapse will still be considered a failure to this Peak Reverse Power test method.

e. If characterizing the DUT for peak reverse power, steps 4.2.a through 4.2.d shall be repeated at higher levels until failure occurs. For this purpose, 10 percent progressive increases in I_{RSM} are recommended. The time between pulses shall be sufficient to permit the DUT temperature to return to its original value before it is repeated.

4.2 Test parameters to be specified and recorded. The following conditions shall be specified:

a. The peak reverse power (P_{RSM}) for rectifiers.

b. Duration of pulses (t_p), shall be 20 µs unless otherwise specified.

c. The $v_{(BR)}$ monitored during the 20 µs impulse. A collapse below minimum rated $V_{(BR)}$ is a failure.

d. Measurements after test.

e. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

f. Duty factor (d.f.) if more than one impulse is specified.

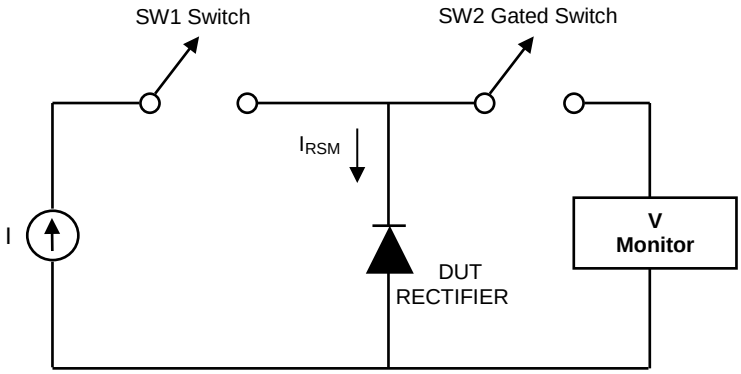

FIGURE 4065–1. Rectangular current pulse test setup.

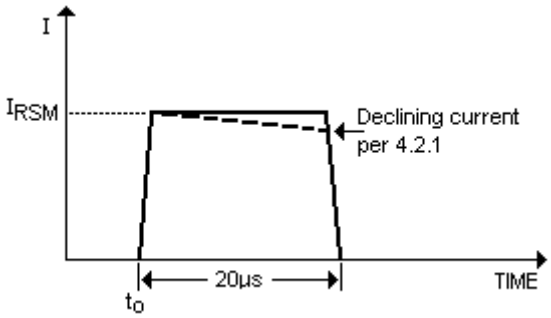

FIGURE 4065–2. Rectangular 20µs Current Pulse Waveform.

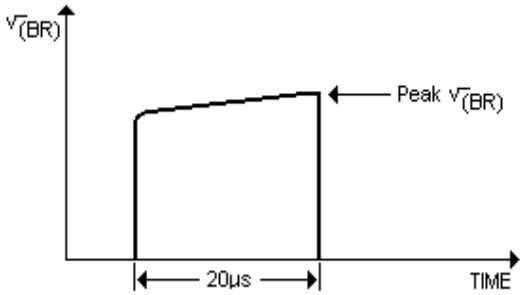

FIGURE 4065–3. Voltage response.

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METHOD 4066.6

SURGE CURRENT AND IMPULSE CLAMP VOLTAGE

1. Purpose. The purpose of this test method is to subject the device under test (DUT) to high current stress conditions to determine the ability of the device chip and contacts to withstand current surges. This is intended to verify a nonrepetitive surge rating where there is sufficient time between surges to permit the device temperature to return to its original value.

* 2. Applicability. This test describes five different conditions: A, B, C, D and E. Surge current is applied in the forward direction to signal diodes and rectifier diodes, and in the reverse direction to voltage regulator (zener) diodes.

Condition A uses half sinusoidal forward current surges, at low duty factor, applied to either a baseline ac or dc current.

Condition B uses rectangular current pulse(s) and is intended primarily for zener diodes or where otherwise applicable. When used with zener diodes, this method utilizes a monitoring circuit to sense possible voltage collapse during the current pulse.

Condition C is intended for high current devices that can be applied to either condition A or condition B.

Condition D uses an exponential rise, exponential fall Impulse current to test clamp voltage capability of transient voltage suppressors (TVS) as well as their ability to withstand the Peak Impulse Current. These devices are also known as avalanche breakdown diodes (ABDs) in JEDEC and the IEC.

Condition E uses an ESD impulse current to evaluate Schottky rectifier robustness in their reverse direction, or for other devices where required.

3. Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method.

a. d.f: Duty factor = 100 t_p / t_{rep}

b. Duty factor: Applied current surge pulses (in percent).

c. I_F: DC forward current (in A).

d. I_{FRM}: AC forward current repetitive peak (in A).

e. I_{FSM}: Nonrepetitive peak value of forward surge current (in A).

f. I_O: Average ac forward current (in A).

g. I_Z : DC reverse zener current (in mA).

h. I_{ZSM}: Nonrepetitive peak value of zener surge current (in mA).

i. n: Number of pulses.

j. t_p: Duration of current surge pulses (in ms).

k. V_{FSM}: Peak forward surge voltage (in V).

l. V_{RSM}: Nonrepetitive peak reverse voltage (in V).

m. V_{RWM}: Working peak reverse voltage (in V).

n. $V_{Z(min)}$: Specified minimum zener voltage (in V).

o. V_{ZSM}: Peak zener surge voltage (in V).

p. T_A: Ambient Temperature (in °C).

q. T_C: Case Temperature (in °C).

r. T_L: Lead Temperature (in °C).

s. I_{PP}: Peak pulse current (in A).

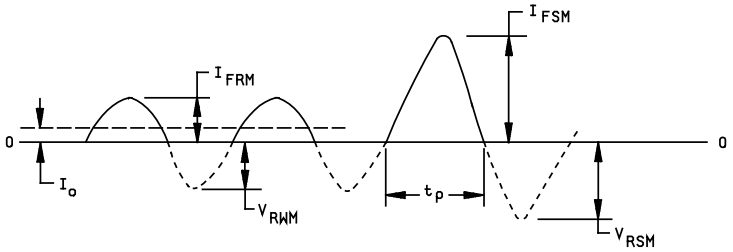
t. Double exponential current waveform (rise time/half time) ____ / ____ µs

u. V_C: Clamping Voltage (in V).

4. Condition A, sinusoidal current surge.

4.1 Apparatus. (As required).

4.2 Procedure. The continuously applied electrical conditions shall be specified and applied to the device under the specified conditions. Unless otherwise specified, the specified number of current pulses (n) shall be superimposed on the continuously applied electrical conditions at the specified duty factor in accordance with figure 4066-1 (condition A1) for rectifiers, or figure 4066-2, (condition A2) for signal and switching diodes, zeners or bridges, as applicable. The surge pulses shall be half-sine waveform and of specified duration (t_p). The duty factor shall be chosen so that the junction temperature is not changed significantly. The “continuously-applied electrical conditions,” shall be satisfied if the time of applied current permits the junction temperature rise to be within 10 percent of its final equilibrium value above ambient before each surge or if an additional temperature or surge current is applied beyond that specified to provide equivalent junction temperature heating during surge without the continuous applied electrical conditions. Also reference condition C for the external heating method.



NOTE: Surge current pulse (tp) does not require synchronization with applied baseline ac.

FIGURE 4066–1. Surge pulse applied to continuous halfwave conditions (condition A1).

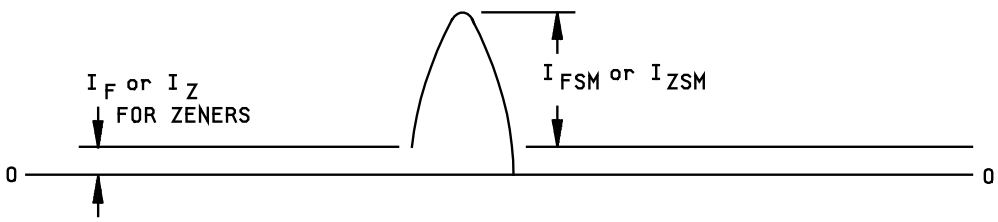


FIGURE 4066–2. Surge pulse applied to continuous dc conditions (condition A2).

4.3 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet:

a. Average forward current (I_O); or dc forward current (I_F) for rectifiers; or zener current (I_Z) for zener diodes; as applicable.

b. Number of current pulses (n).

c. Duration of pulses (t_p), normally 8.3 milliseconds.

d. Duty factor of pulses, normally less than .1 percent, or the period normally between 8 and 60 seconds.

e. Peak value of forward surge current pulse, I_{FSM} for rectifiers, or I_{ZSM} for zeners.

f. Nonrepetitive maximum reverse voltage (V_{RSM}), when applicable.

g. Measurements after test.

h. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

5. Condition B, rectangular current pulse.

5.1 Apparatus. The current source (I) and switch (SW1) combination shown on figure 4066-3 shall be able to apply the peak value of current pulse I_{FSM} or I_Z for the pulse duration (t_p) as required, and shall be able to handle any number of pulses (n) and duty cycle as required in the applicable specification sheet. The rise and fall times of the pulse shall be less than 10 percent of the pulse duration. For zeners, the dashed lines replace the solid connecting lines (vertical) to the DUT. The monitor shall sense V_{ZSM} voltage at the end of the pulse duration before the pulse is removed via gated switch (SW2) to ensure zener voltage has not collapsed below rated $V_{Z(min)}$

5.2 Procedure. As shown on figure 4066-4, no current is applied to the DUT prior to the starting time (t_o) of the test. For zeners, a maximum of 5 percent of rated I_Z may be used for baseline current flow. At t_o, SW1 causes the application of I_{FSM} or I_{ZSM} for time period t_p, after which SW1 causes the current to cease flowing in the DUT. For multiple pulse requirements, SW1 again causes current flow in the DUT after being off for a time necessary to meet the duty factor requirements; this process is repeated for n times as specified. The duty factor and pulse width (t_p) shall be chosen to ensure that the DUT average junction temperature is not changed significantly. For zeners, V_Z monitoring is mandatory. NOTE: If an excessive duty factor is applied where average junction temperature rises with each successive surge, the surge is considered repetitive and must be derated.

5.3 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. The peak surge current (I_{FSM}) for rectifiers or I_{ZSM} for zeners. For rectifiers, this is normally the equivalent rms current as the rated half sine condition. Zeners normally are specified with square wave value of surge current.

b. Number of current pulses (n), shall be five unless otherwise specified.

c. Duration of pulses (t_p), shall be 8.3 ms unless otherwise specified.

d. Duty factor of pulses, normally less than 0.1 percent.

e. V_{ZSM} to be monitored during I_{ZSM} for zeners. A collapse below $V_{Z(min)}$ is a failure.

f. Measurements after test (see 6.1).

g. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

5.4 Alternative to measurements after test. For rectifiers, there is a minor modification to the test that offers the advantage of immediately determining if the DUT survived the test. This consists of monitoring the forward voltage (V_{FSM}) during t_p to determine if device degradation, open-circuit or short-circuit conditions occur. A recorded value of V_{FSM} can be compared to minimum and maximum values in the applicable specification sheet to determine if the device survived the test. NOTE: Zener monitoring is mandatory; it is not an alternative. Collapse below $V_{Z(min)}$ is a failure.

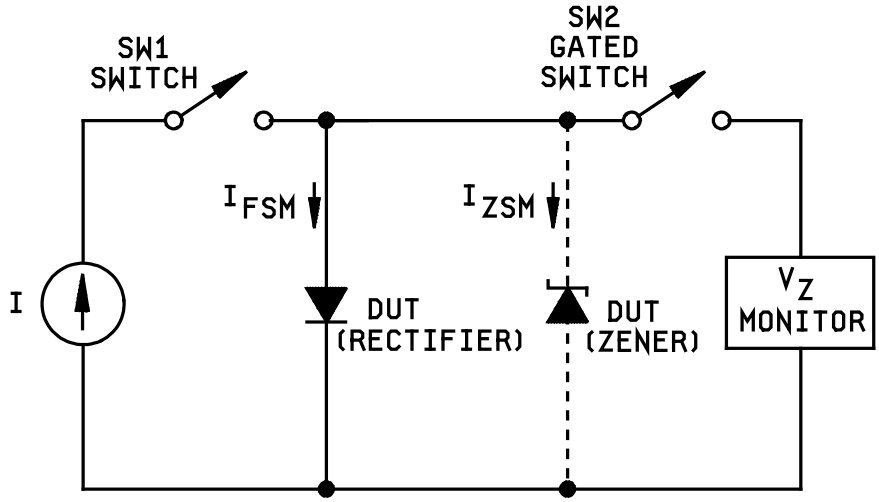


FIGURE 4066–3. Rectangular current pulse test setup.

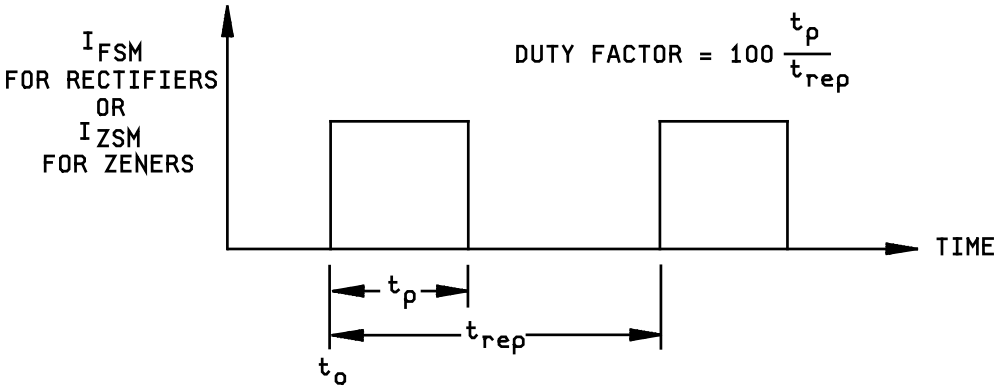


FIGURE 4066–4. Rectangular current pulse waveforms.

6. Condition C (external heating). The worst case test condition for surge current is for device junction temperature at the rated maximum allowable junction temperature. Test condition A approximates this condition by applying forward current to dissipate power in the DUT. The product of this power dissipation and the device thermal resistance produces a temperature rise of the junction over the case temperature at which the surge test is performed. This represents what actually happens to a device in use. However, the actual junction temperature during the surge current test is only at the rated allowable maximum for those individual devices which have both the worst case maximum forward voltage drop and the worst case maximum thermal resistance. Only a very small percentage of actual devices will truly be worst case. The vast majority of devices will be tested at junction temperatures below rated maximum.

Test condition C avoids this short fall in junction temperature and truly represents worst case operation by externally heating the DUT to the specified rated maximum operating junction temperature of the DUT. Consequently, there is no applied heating current prior to, or concurrent with, the surge current. Once the DUT has stabilized at thermal equilibrium at the specified maximum operating junction temperature, the desired surge current pulses are applied at the specified duty factor. The time between current surges shall be long enough to permit the device junction temperature to return to its original thermal equilibrium.

6.1 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet:

a. All conditions defined by the specified test condition in 4.3 or 5.3

b. External heating temperature, TA.

* 6.2 Summary Conditions (A, B, and C). The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test condition letter.

b. Case temperature, T_C.

c. Average forward current, I_O, or dc forward current, I_F for rectifiers, or dc zener current I_Z; as applicable for baseline current.

d. Number of current pulses (see 4.3)

e. Duration of pulses (see 4.3).

f. Duty factor of pulses (or time required between pulses).

g. Peak value of forward surge current for rectifiers or I_{ZSM} for zeners·

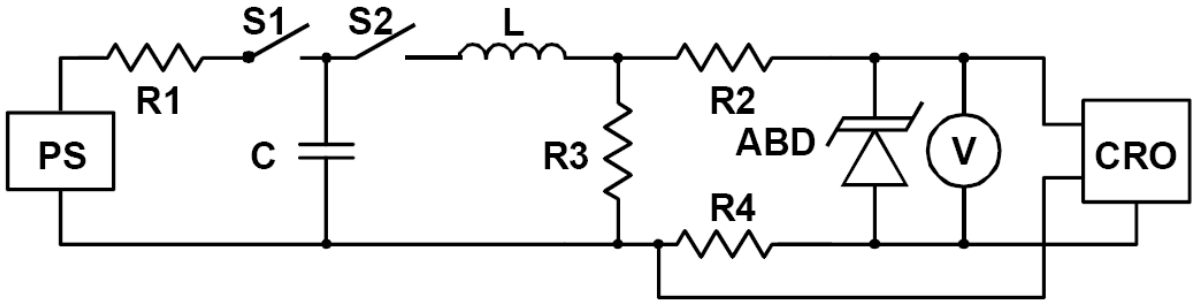
h. Maximum reverse voltage (non-repetitive), V_{RSM}. (V_{RSM} = 0 for conditions A2 and C.)

i. Measurements after test.

j. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

7. Condition D clamping voltage (V_C). The purpose of this test is to determine the peak clamping voltage in the breakdown region of a TVS or ABD, when it is conducting a current impulse (I_{PP}) of a specified waveform.

* 7.1 Procedure. The device under test is connected to a surge generator and the resultant peak clamping voltage is measured with a digital voltmeter or oscilloscope. The test circuit used shall be functionally equivalent to figure 4066–5. Typically waveshapes used for ABD device characterizations are 8/20 µs or 10/1,000 µs for an exponential rise and fall time as shown in figure 4066–6. Bidirectional devices require a test for each polarity. However, sufficient time shall be allowed between the testing of each polarity to allow junction cooling.



PS = Charging power supply
S1 = Charging switch
S2 = Impulse discharge switch
R3 = Impulse shaping resistor
R4 = Current sensing resistor
CRO = Oscilloscope for observing current and voltage

R1 = Charging resistor
C = Impulse shaping capacitor
L = Impulse shaping inductor
R2 = Impulse shaping and current limiting resistor
V = Peak reading voltmeter

CAUTION: The circuit shown is for description only. Measurement techniques for high current, high frequency testing should be observed, such as four point Kelvin contact, differential oscilloscope, short leads etc.

NOTE: The power supply and the charging and shaping components (R1 / C, S1, S2, L / R3) of the circuit can be replaced by a transient generator.

FIGURE 4066–5. Clamping voltage test circuit.

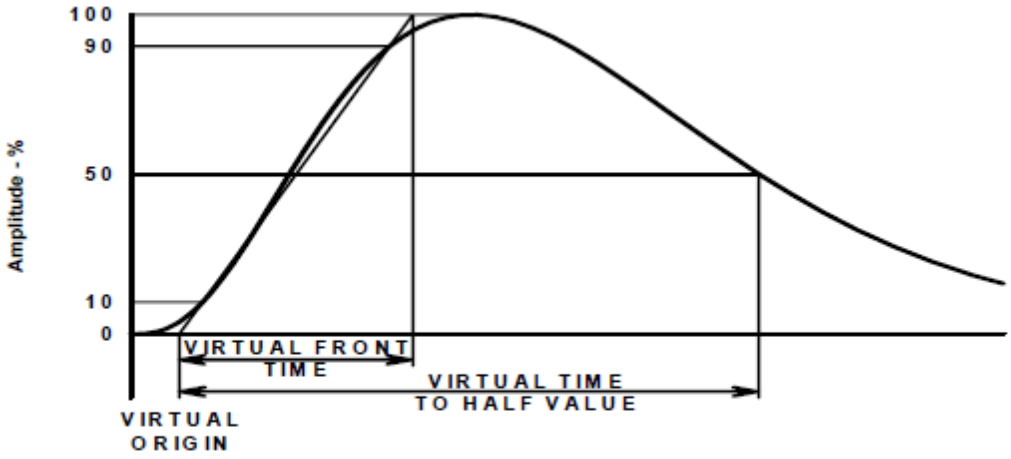


FIGURE 4066-6. Standard current impluse waveshape.

* 8. Condition E (ESD current impulse). The purpose of this test is to ensure Schottky rectifier (or other diode) robustness in the reverse direction from a very short ESD impulse where required. This may also correlate to short impulse currents produced by a high dv/dt rate in various applications. The test may also be performed as 100% ESD surge screening on automated test equipment (similar to TVS device screening).

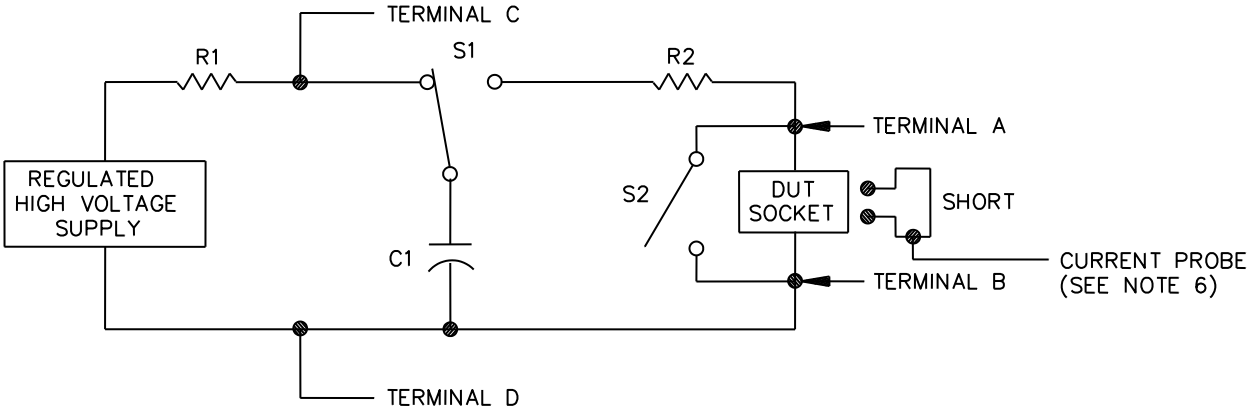
* 8.1 Procedure. The device under test is connected to an ESD surge generator. The test circuit used shall be functionally equivalent to Figure 4066-7 with a typical waveshape shown in Figure 4066-8 (as also shown in test method 1020 for ESD classification).

* 8.2 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet or acquisition document:

a. The peak ESD surge current or ESD classification equivalent in test method 1020.

b. Measurements after test. As a minimum this shall include I_R at rated V_{RWM}.

c. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.



R1 = 10^6 Ω to 10^7 Ω
C1 = 100 pF ±10 percent (Insulation resistance 10^{12} Ω minimum)
R2 = 1,500 Ω ±1 percent
S1 = High voltage relay (Bounceless, mercury wetted, or equivalent
S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

NOTE 1: The performance of this simulator circuit is strongly influenced by parasitics. Capacitances across relays and resistor terminals, and series inductance in wiring and in all components, shall be minimized.

NOTE 2: As a precaution against transients upon recharge of C1, the supply voltage V_S may be reduced before switch S1 is returned to the charging position.

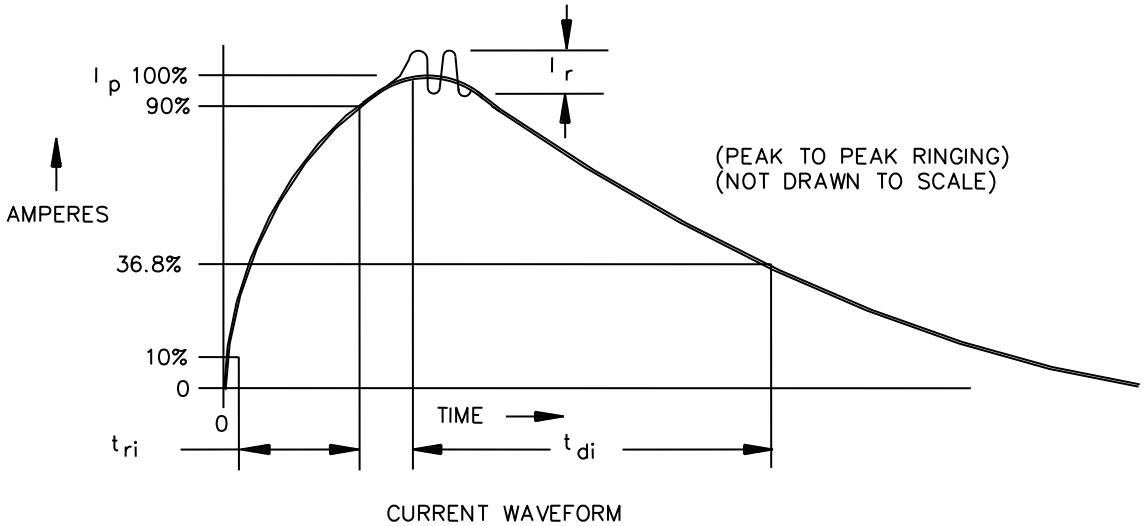
NOTE 3: Piggybacking DUT sockets is not permitted during verification or classification testing.

NOTE 4: Switching terminals A and B internal to the simulator to obtain opposite polarity is not recommended.

NOTE 5: C1 represents the effective capacitance (see 2.3.2).

NOTE 6: The current probe connection shall be made with double shielded cable into a 50 Ω termination at the oscilloscope. The cable length shall not exceed 3 feet (91.44 cm).

FIGURE 4066-7. ESD test circuit (human body model).



t_{ri} (rise time)----------Less than 10 ns.
t_{di} (delay time)----------150 ±20 ns.
I_p (peak current)--------Within ±10 percent of the I_P value shown in table 1020–II for the voltage step selected.
I_r (ringing)----------The decay shall be smooth, with ringing, break points, double time constants, or discontinuities less than 15 percent I_p maximum, but not observable 100 ns after start of the pulse.

NOTE 1: The current waveforms shown shall be measured as described in the waveform verification procedure of 3.2, using equipment meeting the requirements of section 2 herein.

NOTE 2: The current pulse shall have the following characteristics:

FIGURE 4066–8. ESD test circuit waveforms (human body model).

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METHOD 4071.1

TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE

1. Purpose. The purpose of this test method is to measure the temperature coefficient of breakdown voltage under specified conditions.

2. Apparatus. The apparatus used to measure the temperature coefficient of breakdown voltage shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The temperature coefficient of breakdown voltage is the percent of the voltage change from the breakdown voltage obtained at the specified reference temperature to the breakdown voltage obtained at the specified test temperatures.

αVZ shall be calculated using the following formula:

$$\alpha VZ = \frac{V_{(BR)(Test\ temperature)} - V_{(BR)(Reference\ temperature)}}{V_{(BR)(Reference\ temperature)}} X \frac{100}{T_{Test} - T_{Ref}} in\ \%/°C$$

Where the reference temperature is the actual ambient (+25°C ±3°C) and the test temperature is the extreme temperature employed in the measurement.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Temperatures.

b. Test current.

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METHOD 4076.1

SATURATION CURRENT

1. Purpose. The purpose of this test is to measure the saturation current under the specified conditions.

2. Test circuit. See figure 4076-1.

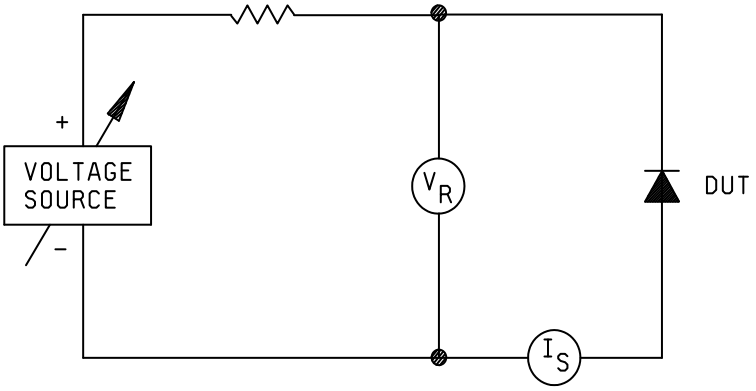

FIGURE 4076–1. Test circuit for saturation current.

3. Procedure. The supply voltage is adjusted until the specified reverse voltage across the diode is achieved. The saturation current is then read from the current meter. Unless otherwise specified, the reverse voltage for measurement of saturation current shall be approximately 80 percent of the nominal breakdown voltage for voltage regulator diodes and approximately 80 percent of the minimum breakdown voltage for rectifiers.

4. Summary. The test voltage (see 3) shall be specified in the applicable performance specification sheet or acquisition document:

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METHOD 4081.4

THERMAL RESISTANCE OF DIODES
(FORWARD VOLTAGE, SWITCHING METHOD)

1. Purpose. The purpose of this test is to determine the thermal resistance of lead, case, or surface mounted diodes under the specified conditions.

1.1 Definitions. The following symbols shall apply for the purpose of this test method:

a. D: Heating power duty factor.

b. I_H: Heating current in Amps applied to diode during P_H.

c. I_M: Measuring current in milliamperes.

d. P_C: Magnitude of power in watts applied to diode during measuring and calibration.

e. P_H: Magnitude of heating power in watts applied to diode causing temperature difference $T_J – T_R$.

f. $R_{\theta JR}$: Thermal resistance, junction-to-reference point, in degrees Celsius/watt.

NOTE: For different package designs, the reference point "R" will be the Lead "L" for axial-leaded packages or leaded-surface-mount packages, the Case "C" for case-mounted packages or surface mounted products mounted by integral electrical contacts in the case (e.g. SMD-.5, SMD-1, SMD-2) , and End Cap "EC" for surface mount MELF style packages.. These package configurations have thermal resistance acronyms of $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JEC}$ respectively. Other reference points may also be made such a "Solder Pad" on small surface mount products for $R_{\theta JSP}$.

g. T_{CC}: Case temperature in degrees Celsius, measured at the reference point prior to application of heating power P_H.

h. T_{CH}: Case temperature in degrees Celsius, measured at the reference point after the junction has been heated by P_H.

i. T_J: Junction temperature in degrees Celsius.

j. T_{LC}: Lead temperature in degrees Celsius, measured at the reference point prior to application of heating power P_H.

k. T_{LH}: Lead temperature in degrees Celsius, measured at the reference point after the junction has been heated by P_H.

l. T_{MC}: Calibration temperature in degrees Celsius, measured at reference point.

m. t_{MD}: Measurement delay time in microseconds. This is the delay between when P_H is removed and when the temperature sensitive parameter (TSP) is recorded to determine junction temperature rise (see 3.a).

NOTE: Delay shall be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture (short is always better), associated fixture inductances, package magnetic properties and chip charge storage properties. See further clarification of the use of t_{MD} in this test method and in Appendix A

n. T_R: Reference point temperature in degrees Celsius.

o. TSP: Temperature Sensitive Parameter, also known as K-factor. Thermal calibration factor equal to the reciprocal of VTC; in °C/mV. Shall be measured over a temperature range similar to the test temperature range at an I_M that will permit resolution at the highest temperatures reached during the test.

NOTE: It is important that the range of temperatures that TSP or K-factor is measured over approximately correlates to the range of temperature used for thermal measurements (unless limited by the test equipment). It is wise to characterize your product at least once over a broad temperature range using increments of 25°C as well as over several values of I_M. Some devices, especially gold doped devices and Schottky diodes, can have a saturation current at these elevated temperatures that can overwhelm the I_M current. Characterization is required as it might reveal that a higher value of I_M will be needed.

p. V_{MC}: Value of temperature-sensitive parameter in millivolts, measured at I_M and specific value of T_{MC}.

q. V_{MH}: Value of temperature-sensitive parameter in millivolts, measured at I_M, and corresponding to the temperature of the junction heated by P_H.

r. VTC: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_M; in mV/°C.

s. T_A: Ambient or free air temperature, the air temperature measured below a device in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

NOTE: Testing has historically been performed in an open lab or on the production floor subject to natural convection and air movement produced by HVAC (Heating, Ventilation and Air Conditioning) common to all industrial locations. The maximum air movement allowed for the testing of free air (ambient) thermal resistance is 1.0 m/s and any air movement exceeding this shall be blocked.

t. V_F: The forward biased junction voltage of the DUT used for junction temperature sensing parameter (TSP).

2. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

a. Thermocouple material may be copper-constantan (type T), chromal-alumel (type K) or equivalent, for the temperature range -180°C to +370°C. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted (exception is the type K open junction method where the junction is formed upon each wire's contact with the measured metallic surface). The accuracy of the thermocouple and associated measuring system shall be ±1.0°C.

b. Controlled temperature chamber or heat sink capable of maintaining the specified reference point temperature to within ±1.0°C of the preset (measured) value. For various package mounting configuration examples, see figure 4081–2 for axial-leaded, figures 4081–3 and 4081–4 for case mounted, figure 4081–5 for power SMD mounting, and figure 4081–6 for small signal LCC surface mounted.

c. Suitable electrical equipment as required to provide controlled levels of conditioning power and to make the specified measurements. The instrument used to electrically measure the temperature-sensitive parameter shall be capable of resolving a voltage change of 1.0 mV. An appropriate sample-and-hold unit or a cathode ray oscilloscope shall be used for this purpose

3. Procedure. In measuring thermal resistance, the forward voltage is used as the temperature-sensitive parameter (TSP) to indicate the junction temperature (see figure 4081–2 for mounting arrangement).

a. Power application test. The power application test shall be performed in two parts. For both portions of the test, the reference point temperature shall be held constant at the specified value. The value of the temperature-sensitive parameter V_{MC} shall be measured with a measuring current (I_M) that will produce negligible internal heating. The diode under test shall then be operated with heating power (P_H) intermittently applied at a greater than or equal to 0.98 duty factor. The temperature-sensitive parameter V_{MH} shall be measured during the interval between heating pulses with constant measuring current (I_M) applied.

The delay time between the heating power turning off and the V_{MH} being read is the measurement delay time $t_{MD.}$ If it is not possible to maintain the reference point temperature constant during the power application test [such as lead (T_{LH}) or case (T_{CH}) temperature], the difference in the reference temperature at which V_{MH} and V_{MC} are measured shall be recorded. For an axial-leaded device example, the lead temperature difference ($T_{LH} – T_{LC}$) divided by the average heating power (DP_H) shall be subtracted from the calculated thermal resistance to correct for this error. It is not possible, due to the presence of electrical transients in the voltage waveform, to measure the TSP at the instant that the heating current is removed.

For a particular device type or when the appropriate performance specification does not specify t_{MD}, the shortest t_{MD} time after removal of heating current before the TSP is measured shall be found by performing the test at various power levels and noting the shortest time where the measured value of thermal resistance is essentially independent of power dissipated. Power levels of 25 percent above and below the power corresponding to the specified heating current are recommended for determining this delay time. The junction-to-lead thermal resistance shall therefore be calculated from the value of the temperature-sensitive parameter V_{MH} as measured at the previously determined delay time. This will vary depending on package design and materials, particularly for metal package encapsulations for high power devices involving magnetic materials requiring longer delay time due to switching transients. The heating power (P_H) shall be chosen such that the calculated junction-to-reference point temperature difference as measured at V_{MH} is greater than or equal to +50°C.

b. Measurement of the temperature coefficient of the temperature-sensitive parameter (calibration). The temperature coefficient of the temperature-sensitive parameter (TSP) shall be measured utilizing the chosen measuring current (I_M) used during the Power Application Test. The DUT shall be externally heated in an oven, a heated bath, or on a temperature controlled heat sink. The measuring current shall be chosen such that the TSP varies linearly with temperature over the range of interest and that negligible internal heating ($P_C \approx 0$) occurs during the calibration procedure, i.e., $T_R \approx T_J$. The reference point temperature range used during calibration shall encompass the temperature range encountered in the Power Application Test. The value of the TSP temperature coefficient ($\Delta V_{MC}/\Delta T_{MC}$) shall be calculated from the calibration curve (V_{MC} versus T_{MC}). It can generally be assumed that, for devices of a given design and construction, the temperature coefficient of the TSP is constant. The temperature coefficient shall be measured on 10 devices to validate this assumption. If the relative sample standard deviation of these measurements is less than or equal to ±3 percent, the average of the measured temperature coefficients can be used in the calculation of thermal resistance for all other devices of the design and construction.

c. Calculation of thermal resistance. Examples shown are for thermal resistance junction to lead ($R_{\theta JL}$) for both axial-lead designs and surface mount configurations with very short terminations. Also thermal resistance junction to case ($R_{\theta JC}$) and thermal resistance junction to end cap ($R_{\theta JEC}$) for surface mount MELF packages DO–213AA and DO–213AB JEDEC outlines are described.

3.1 Package considerations and method of calculation.

3.1.1 Axial lead diodes. For axial-lead diodes, the reference point for calculations of the junction-to-lead thermal resistance ($R_{\theta JL}$) shall be at a point on the lead 0.375 inch (9.52 mm) from the body of the diode under test. For thermally unsymmetrical devices, the specified lead temperature shall be the average of the two lead temperatures measured with both leads terminated thermally in the same manner. For surface mount diode packages with short-lead terminations such as J-bends or gull wings, the reference point for calculation of thermal resistance shall be at or near the mounting plain of the terminal configuration of the diode under test. The following equation is used to calculate the junction-to-lead thermal resistance:

$$R_{\theta JR} = \frac{T_J - T_R}{DP_H} = \frac{V_{MH} - V_{MC}}{DP_H} \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1} Calibration - \left[\frac{T_{LH} - T_{LC}}{DP_H}\right] Optional$$

where V_{MC} is the value of the temperature-sensitive parameter for T_{MC} equal to T_{LC} and $T_{LH} - T_{LC}$ corrects for variations in the lead temperature during the Power Application Test.

3.1.2 Case mounted power diodes. For case-mounted power diodes such as TO–3, stud mounts (DO–4 thru DO–9), and high power surface mount devices (SMD) with a metal bottom for heat transfer, the reference point for calculation of the junction-to-case thermal resistance ($R_{\theta JC}$) shall be at or near the mounting plain and in the heat-flow path to the heat sink for a diode under test. This requires drilling a hole in the component case to insert a thermocouple for accurate measurement as shown on figure 4081–3, or providing an access-hole in the heat sink to locate the T_R reference point on the case in the heat-flow path as shown on figures 4081–4 and 4081–5. The T_{LH} and T_{LC} in 3.1.1 then become T_{CH} and T_{CC} respectively to calculate junction-to-case thermal resistance. The $T_{CH} - T_{CC}$ corrects for possible variations in the case temperature during the Power Application Test. For some of the surface mount designs, an accurate thermal resistance measurement may require soldering the device under test to a heat sink. In these examples, soldering methods should not exceed rated soldering temperatures for the package.

3.1.3 Low power surface mount. For lower power surface mount packages such as MELFs or LCC devices, this reference point may instead be identified as the end cap temperature (T_{EC}) or the solder pad (T_{SP}) as shown on figure 4081–6. The T_{LH} and T_{LC} in the above equation would then become T_{ECH} and T_{ECC} or T_{TPH} and T_{TPC} respectively to calculate the junction-to-endcap thermal resistance.

3.1.4 Multi-Junction packages (duals, quads, etc.). While the assumption has been that the specifications for thermal resistance apply to all elements in parallel, there has been no procedure on how to do this. The thermal resistance test setup cannot directly parallel the diodes junctions because the junction with the lower V_F may draw some of the current away from the other elements. For thermal resistance, measuring one junction while the other junctions are passively biased at the same power level does work. No power is to be applied until V_{MC} has been measured, however, V_{MH} will likely be unaffected if the passively biased junctions are turned off a little late. The Thermal Resistance value for the measured junction is divided by the total number of junctions being biased to calculate an overall package thermal resistance. To summarize:

1) Begin thermal resistance test of one junction while others are off.

2) Power up remaining junctions to same current as the junction under test.

3) Power off remaining junctions only AFTER the test junction reading has been acquired.

4) Calculate total device thermal resistance = reading of test junction divided by total junctions in package.

Measurements of T_R and T_{MC} for all examples are made by means of a thermocouple attached to the referenced point. The power dissipation in the DUT is calculated from the equation $P_H = I_H \times V_F$. If the power dissipation during measuring and calibration is not negligible, then P_C should be subtracted from P_H when calculating the thermal resistance. The P_C is calculated from the equation $P_C = I_M \times V_M$. The specimen junction-temperature shall be considered stabilized when doubling the time between the initial application of power and the taking of the reading causes no error in the indicated results beyond the required accuracy of measurement. The time for stabilization will typically be 20 to 60 seconds depending on package configuration and size.

3.2 Test circuit. See figure 4081-1.

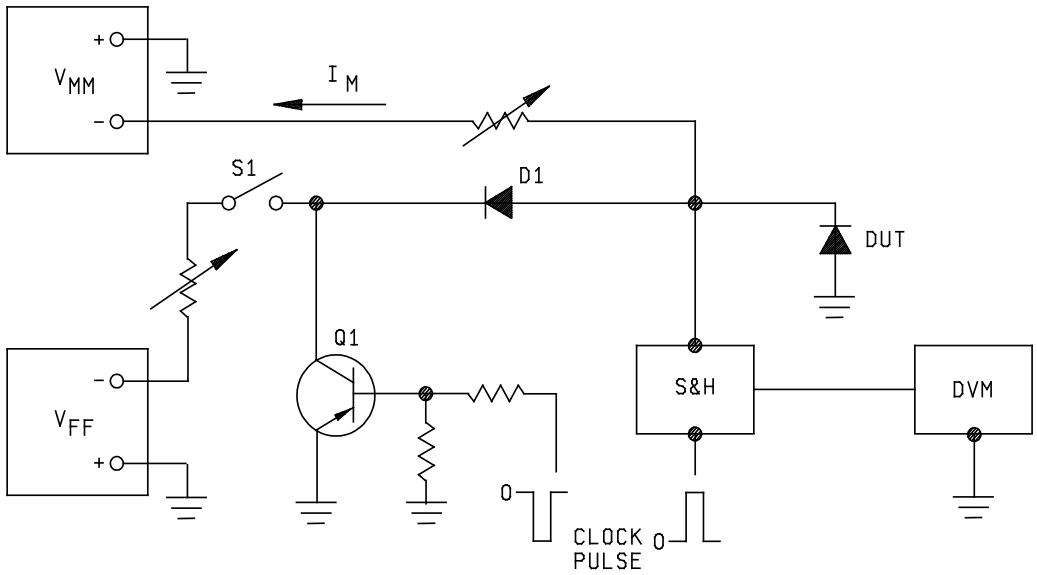

FIGURE 4081–1. Test circuit.

The circuit is controlled by a clock pulse with a pulse width less than or equal to 300 μs and repetition rate less than or equal to 66.7 Hz. When the voltage level of the clock pulse is zero, the transistor Q1 is off and the forward current through the DUT is the sum of the constant heating current and the constant measuring current. Biasing transistor Q1 on, shunts the heating current to ground and effectively reverse biases the diode D1. The sample-and-hold unit (S and H) (or cathode ray oscilloscope) is triggered when the heating current is removed and is used to monitor the forward voltage of the diode under test. During calibration, switch S1 is open.

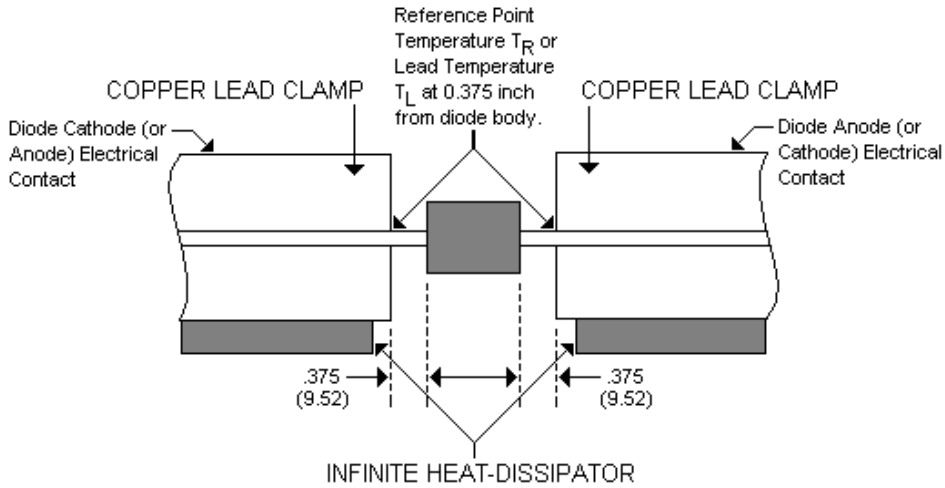

FIGURE 4081–2. Axial-leaded mounting arrangement.

4. Summary. The following conditions shall be specified in the detail specification:

   a. Reference point temperature for heating power measurements.

   b. Accept or reject criteria.

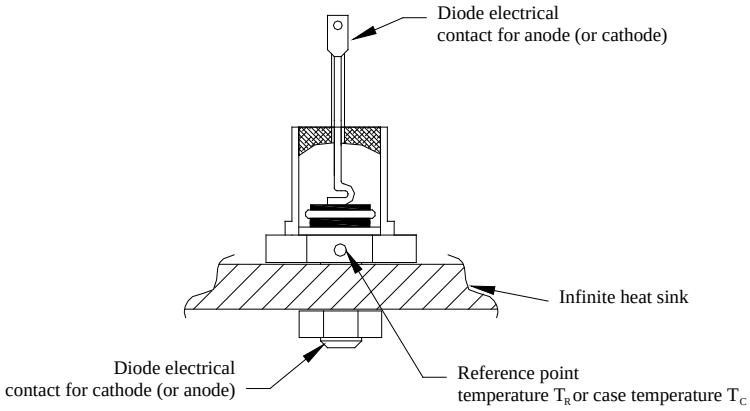

FIGURE 4081–3. Case mounting arrangement. (stud packages).

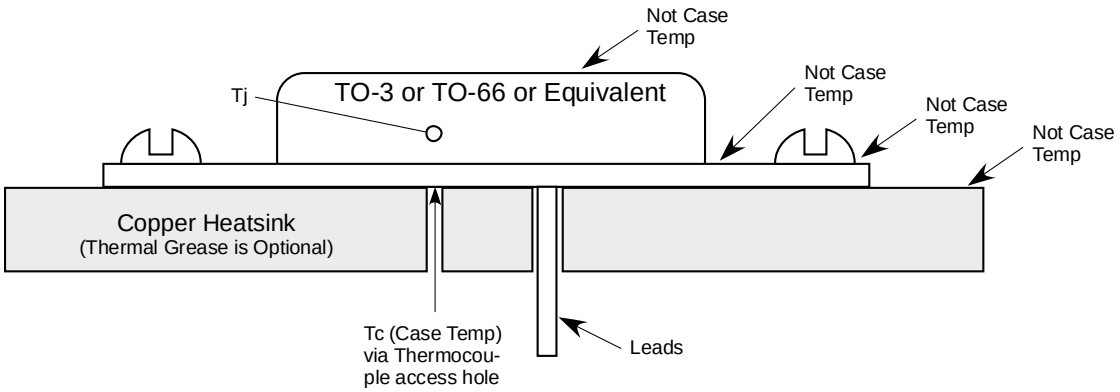

FIGURE 4081–4. Case mounting arrangement. (TO–3 or TO–66).

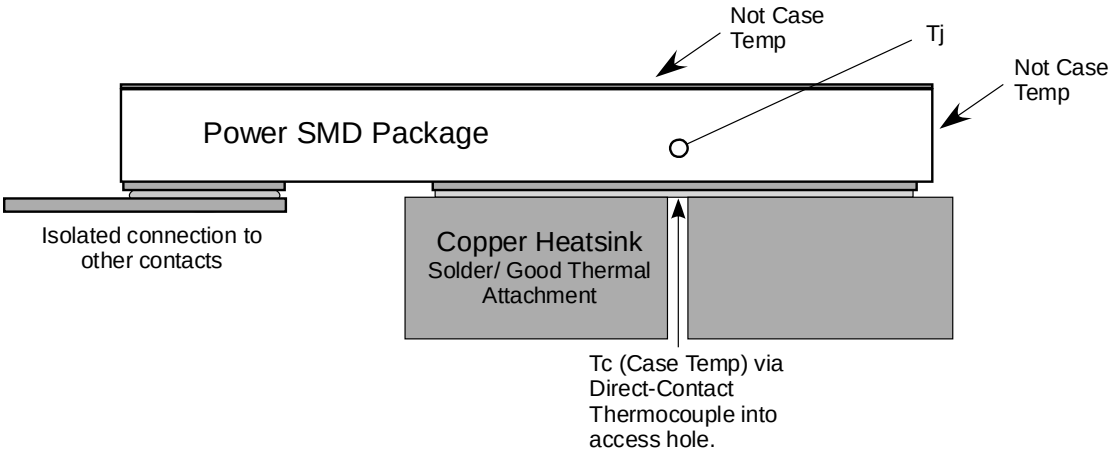

FIGURE 4081–5. Surface-Mount arrangement and Temperature Sensing Location (SMD)

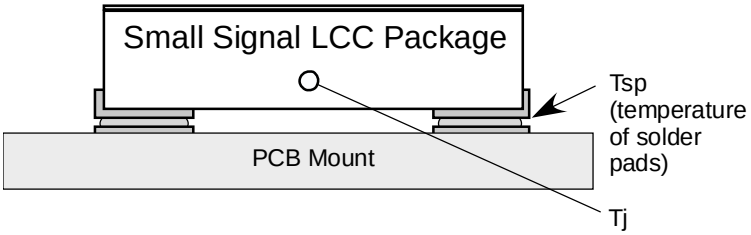

FIGURE 4081–6. Surface-Mount arrangement and Temperature Sensing Location (LCC).

APPENDIX

BACKWARD t_{MD} PROJECTOR CALCULATION METHOD

A.1 Backward t_{md} projector calculation method. While the thermal impedance test method makes allowances for devices that have either magnetic or stored charge issues that hinder using delay times under 100 µs, this "backward projector calculation method" actually gives one method to make the allowance. Generally this correction is only needed for steady-state thermal impedance (a.k.a. thermal resistance) because it is thermal resistance that usually has a specification maximum. Short-pulse-width thermal impedance used for SPC (Statistical Process Control) purposes and for screening out poor die bond problems is just as effective regardless of the value of t_{MD} used. However, if absolute thermal impedance accuracy is required, then a minimum delay time is still required for correlation reference.

Figure 4081–A1 illustrates what a thermal impedance tester sees when a test is performed. The first reading (V_F) is always the easiest to take. The second Reading (V_F) can be misled by ferromagnetic resonant delay, stored charge, etc. and must be delayed until the device has stabilized. When the device stabilized within the 100 µs t_{MD} period, no further compensation is required.

Analysis of a Theta Test

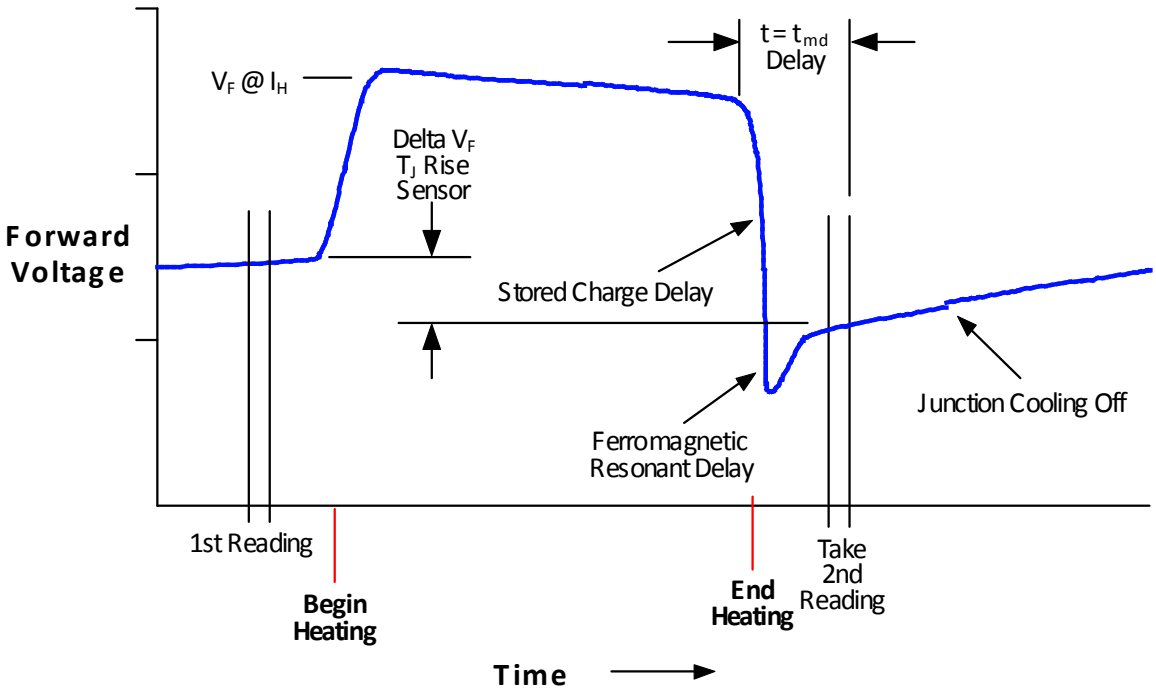

FIGURE 4081–A1. Analysis of theta test.

However, when a much longer t_{MD} is required to avoid the interference caused by magnetics and stored charge, the backward projector calculation method can be used.

APPENDIX

A.2 The backward t_{MD} projector calculation.

A.2.1 Definitions:

t_{MD} = Spec delay time for Theta (such as 70 µs when it otherwise cannot be measured directly).

t_{MD1} = Delay time that can be measured (such as 1000 µs) for Theta 1.

t_{MD2} = Forced 2nd delay = (approximately 2 to 3 times t_{MD1}) for Theta 2.

(Any units for t_{MD} and theta can be used, but be consistent throughout).

A.2.2 Constants:

c = (Theta1 - Theta2) / [SQRT(t_{MD1}) - SQRT(t_{MD2})].

k = Theta1 - c * SQRT(t_{MD1}).

Solve:

Theta(t_{MD}) = k + c * SQRT(t_{MD}).

NOTE: For ideal Theta value, set t_{MD} = 0 in the equation, which yields the value of just k.

While it is possible to have a thermal impedance tester programmed to do this automatically, it is also possible to calculate a one-time correction factor that can be applied to the test limit and allow testing using t_{MD1} and theta1 to adjusted limits.

Calculate the correction factor for a given design and use it instead:

Factor = theta(t_{MD})/ theta1,
Factor = [k + c * SQRT(t_{MD})] / [k + c * SQRT(t_{MD1})]

So that the correct theta (t_{MD}) = measured theta1 at t_{MD1} * Factor.

Likewise, the new screening max theta1 limit using t_{MD1} becomes theta(t_{MD})/ Factor.

This "Factor" value can be used to apply to any one design (same chip, same package)
using the same test setup conditions (I_H, I_M, V_{CE}, etc.) without the need to do any future re-calculations.

Figure 4081–A2 shows examples of a device that benefits immensely from the use of the backward t_{MD} projector. (plus the same part with the "trouble maker" removed) and a device that doesn't need the "projector" at all. Note that using the "projector" for a device that does not need the "projector" does not cause any error. The point is also made that the backward t_{MD} projector can work for any semiconductor device including bipolar transistors, field-effect-transistors and diodes.

A.3 Figure 4081–A2. Figure 4081–A2 shows a device that is very much in need of correction. This particular example is for a rectifier but this "projector" method works equally well for diodes and transistors. The dashed line is the output of the "projector", where the value of t_{MD} is varied from zero out to T_{MD2}. The magnetic (due to steel cap) and stored charge perturbations end between 700 µs and 800 µs.

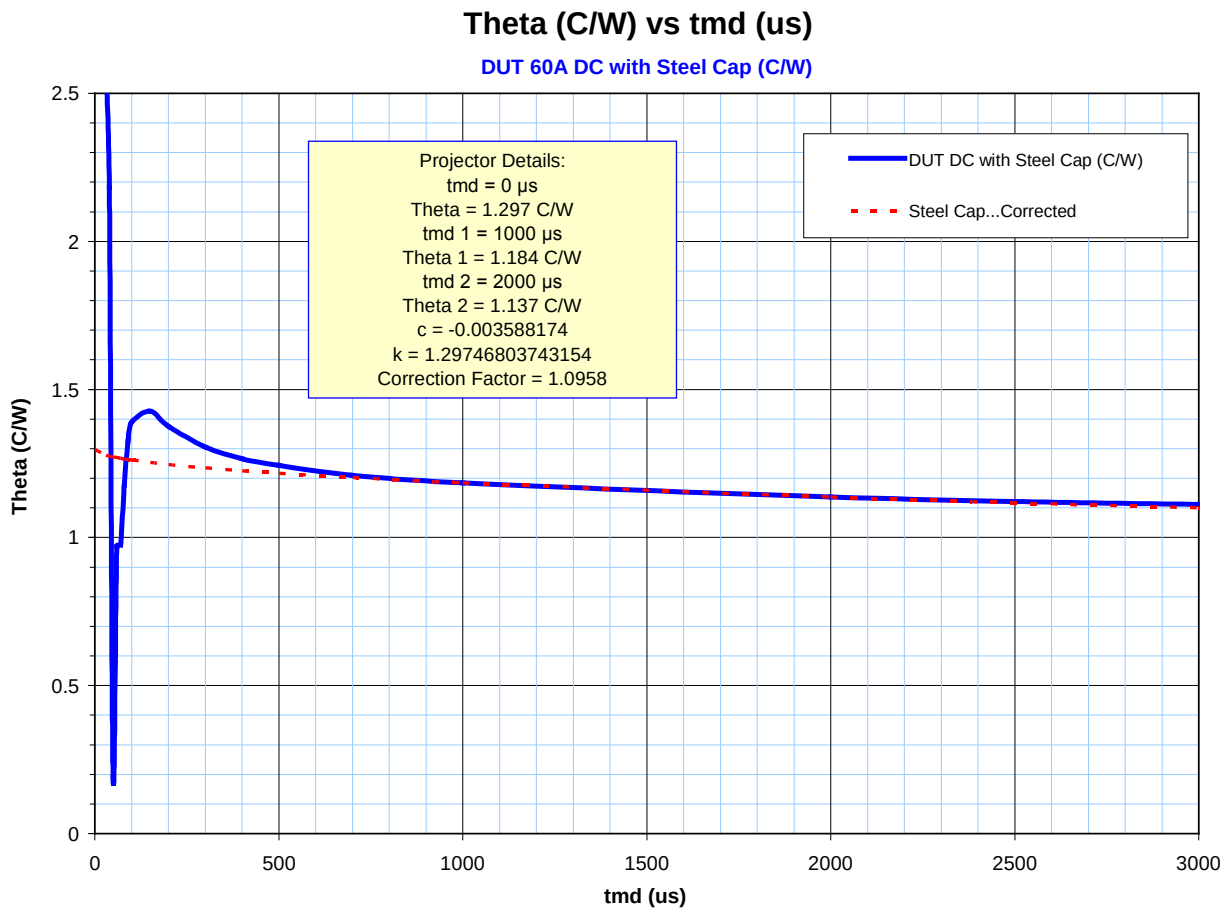

FIGURE 4081–A2. Theta vs. t_{MD}.

NOTE: Observe closely on the curve above that if the "projector" had not been used, e.g. t_{MD} = 50 µs had been used instead, a theta value less than 25 percent of the actual theta value would have been measured. The next measurement would have likely been erratic and your SPC charts would be plotting setup errors and not product integrity.

A.4. Figure 4081–A3. Figure 4081–A3 shows the identical device depicted above except that the steel cap, the cause of much of the magnetic perturbations, has been removed. The perturbations are quite natural since the current carrying terminals pass through the cap creating an artificial magnetic core in which to store energy.

This figure does show that other problems can cause unnatural oscillations (especially at these high currents) where error begins to creep in below 400 µs.

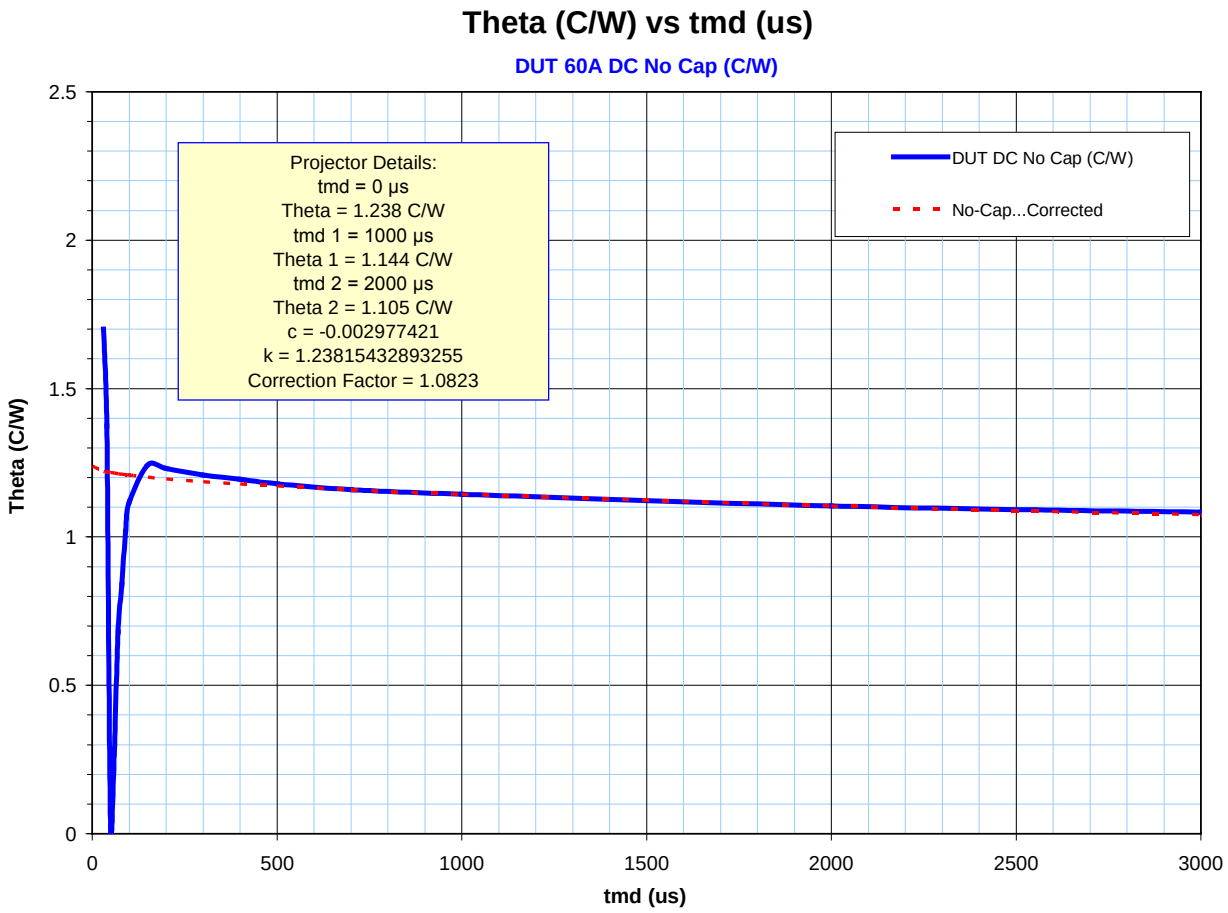

FIGURE 4081–A3. Theta vs t_{MD}.

NOTE: The magnetic disturbances removed, there only remains the effects of stored charge and/or recovery delay in the thermal resistance tester as, in this case, the power source shall switch from I_H=60 A to I_M=50 mA.

A.5. Figure 4081–A4. Figure 4081–A4 shows a device that requires almost no correction at all. The plot shows measured thermal impedance essentially tracking with the "projector" plot. One of the reasons this part performs so well is that the test current is very low (1 A), the chip is very fast, and the case has very little magnetic influence.

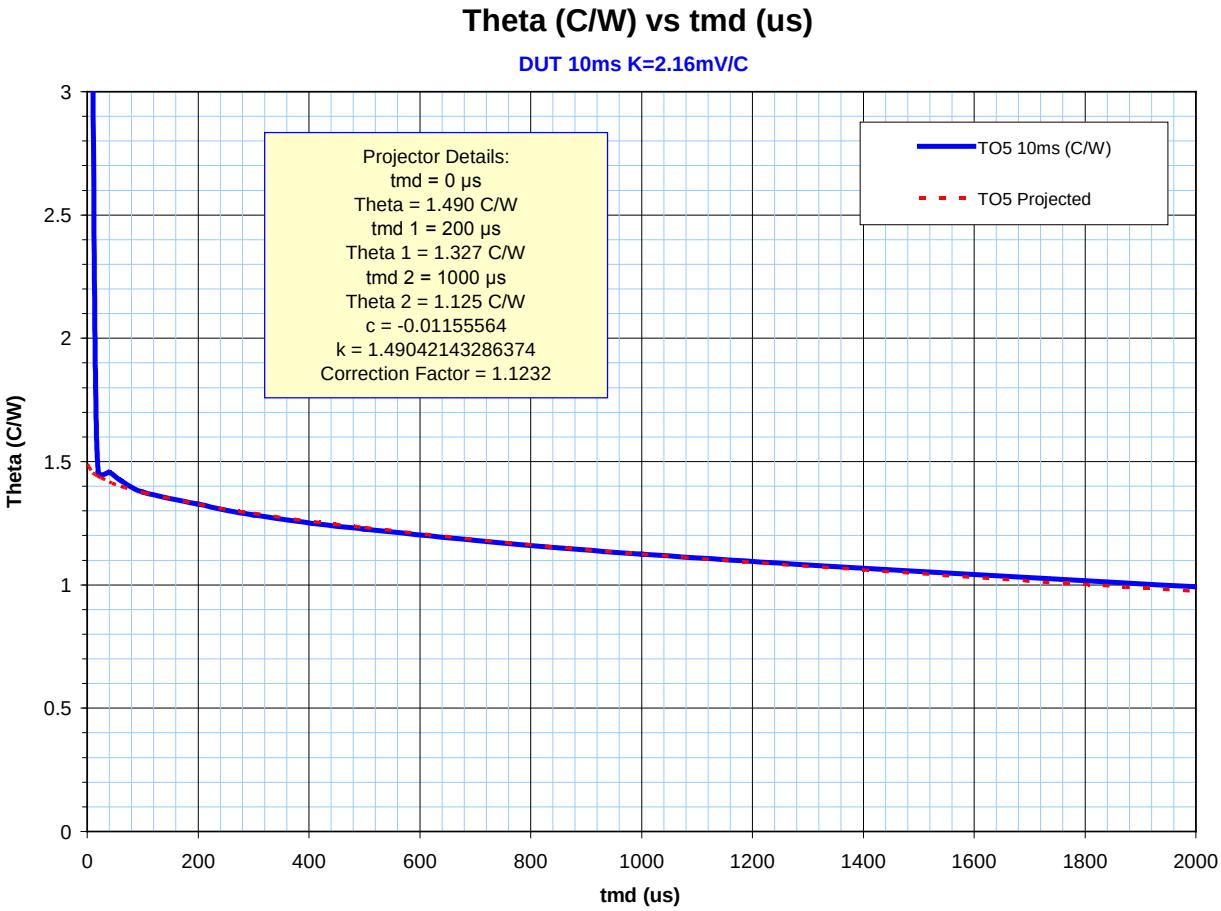

FIGURE 4081–A4. Theta vs. t_{md}.

NOTE: Knowing exactly how to select t_{MD1} and t_{MD2} is important. Note that t_{MD1} shall be selected just past the point where various perturbations occur and this can be accomplished by making "cooling plots" like the plots used for the figure above. For t_{MD2}, usually pick a value between 2 to 3 times t_{MD1}.

A.6. Figure 4081–A5. Figure 4081–A5, a finite element analysis cooling plot, has been prepared for which the thermal resistance at $t_{MD} = 0$ is known by definition. This provides evidence that the "projector" actually shows what is happening at $t_{MD} = 0$.

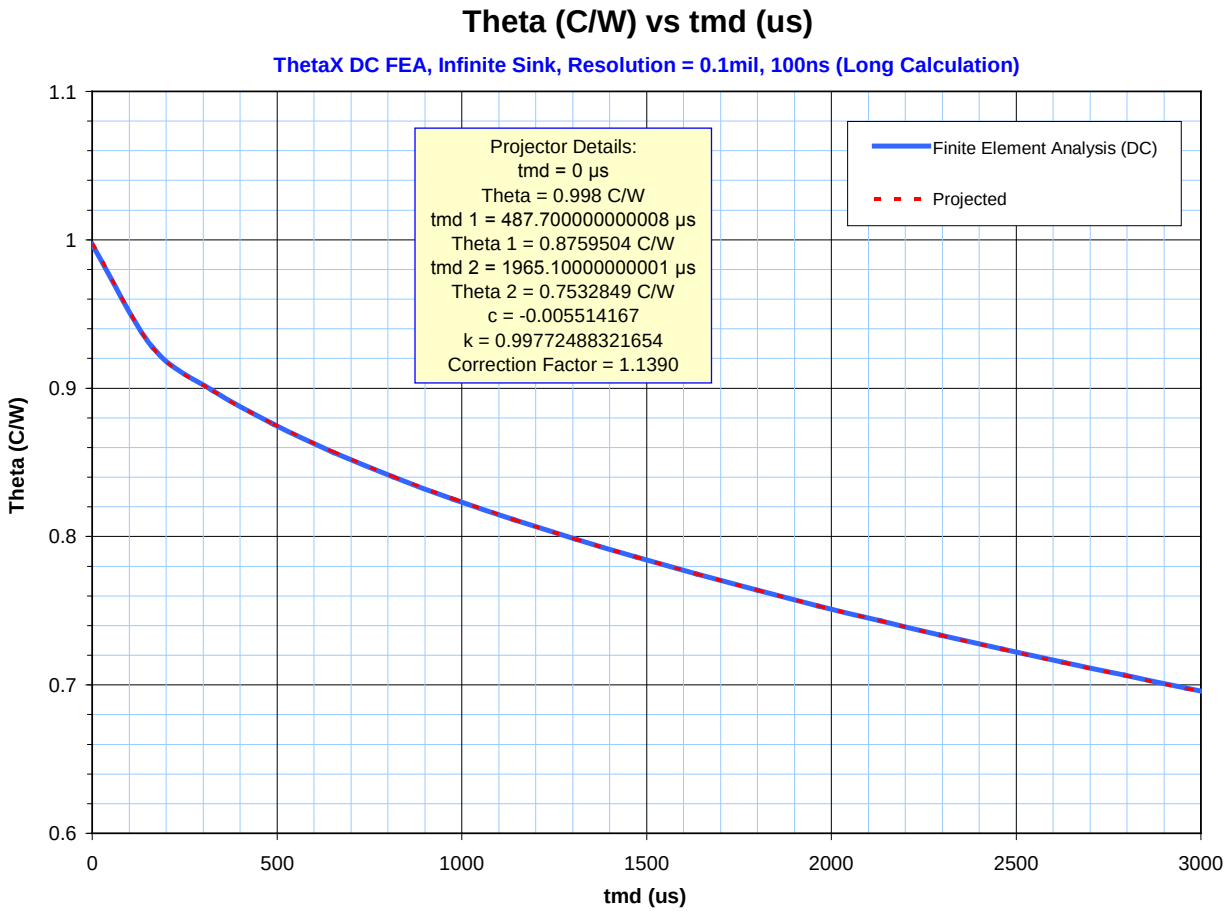

FIGURE 4081–A5. Theta vs. t_{md}.

NOTE 1: The selection of "odd" values of t_{MD1} and t_{MD2} is because these were provided by the computer. It can be seen that the FEA output (solid line) and the "projector" overlay each other perfectly.

NOTE 2: Closing: Be aware that when measuring thermal resistance, the "projector" works very easily with very little guess work. When used for pulsed thermal impedance, some error can creep in if t_{MD1} and/or t_{MD2} is selected carelessly. Again, be prepared with the appropriate cooling plot curve for a given semiconductor family.

NOTE 3: It has always been believed that measuring theta at $t_{MD} = 0$ was impossible. With this method, it can be done.

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METHOD 4101.3

CONVERSION LOSS

1. Purpose. The purpose of this test is to determine the ratio of the available RF input power to the available IF output power under specified conditions.

2. Test circuits. The following test circuits shall apply. (See figures 4101–1 through 4101–4).

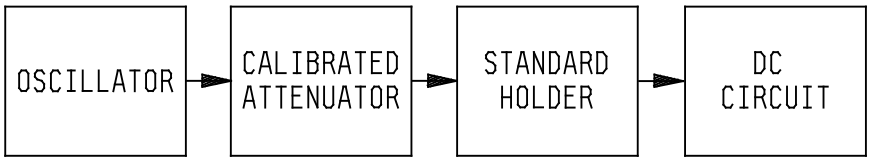

FIGURE 4101–1. Test setup for incremental measurement.

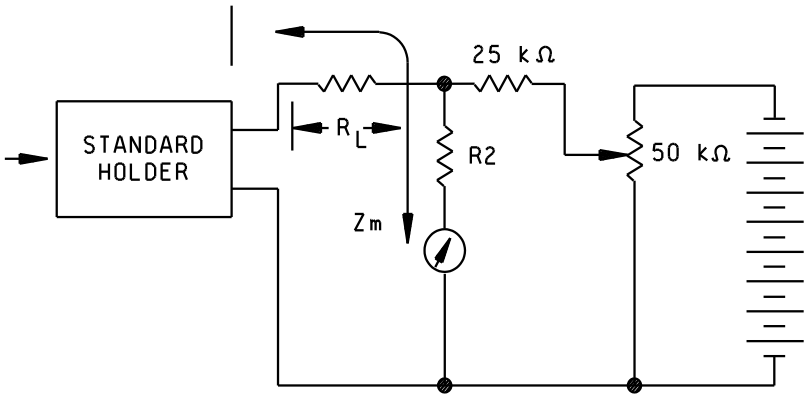

FIGURE 4101–2. Output circuit for the incremental measurement.

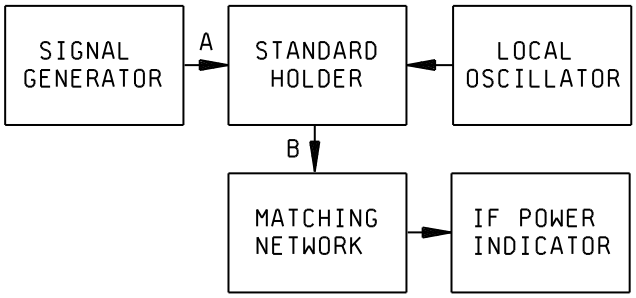

FIGURE 4101–3. Test setup for heterodyne measurement.

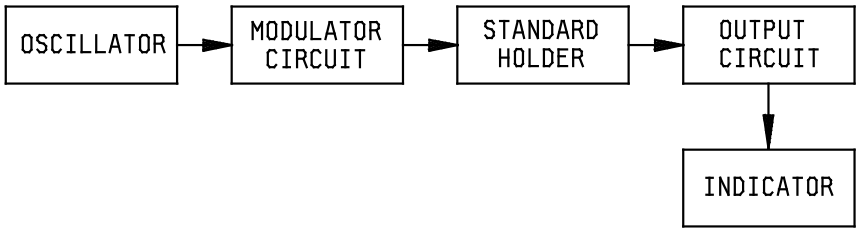

FIGURE 4101–4. Test setup for modulation measurement.

2.1 Overall noise figure method. See figure 4121–1method 4121 for output noise ratio and test method 4126 for overall noise figure.

3. Procedure.

3.1 Test condition A (incremental). The equipment for this test is shown on figures 4101–1 and 4101–2. An expression for conversion loss is shown in the equation:

$$L = \frac{G_b}{2P_o\left(\frac{\Delta I}{\Delta P}\right)^2}\left[\frac{4G_b\frac{\Delta I}{\Delta V}}{\left(\frac{G_b+\Delta I}{\Delta V}\right)^2}\right]$$

L = Conversion loss.
ΔI = Incremental change in current.
ΔP = Incremental change in power.

P_o = Average power ($P + 0.5\Delta P$).

$$G_b = \frac{1}{Z_m}$$

$\frac{\Delta I}{\Delta V}$ = IF conductance of diode under test.

IF conductance $= \frac{1}{Z_{if}}$

The diode is loaded by the resistance $R_L + r_2$ that is adjusted to the specified load impedance (Z_m). $Z_m R_L$ is the dc load resistance; load resistance shall be specified. The current supplied by the battery balances out the diode current at some standard power level P, and makes the current in the microammeter zero. With a change in power ΔP, ΔI can be measured directly. With the injection of a small voltage (few millivolts) ΔV at P_o power level, ΔI can be directly measured. (This impedance can be measured by other means. See IF impedance, method 4116, Z_{if}.) These values can be inserted in the equation and the conversion loss can be calculated for the conditions of test.

3.2 Test condition B (heterodyne). A signal generator feeds signal power to the mixer that converts the power to the IF by beating with the local oscillator. The converted power is measured with an IF power meter. Both the available signal power from the generator at A, shown on figure 4101-3, and the increase in the available IF power at B shall be measured when the noise is applied, their ratio being the conversion loss.

3.3 Test condition C (modulation). The equipment for this test is shown on figure 4101–4. Conversion loss is given by the equation:

$$L = \frac{4n}{(1+n)^2} \bullet \left[\frac{m^2 p}{G_b \ x \ E_B^{\ 2}}\right]$$

m = modulation coefficient.

P = available power.

E_B = rms modulation voltage across load.

n = ratio of load conductance to IF conductance.

$G_b = \frac{1}{Zm}$

To avoid measuring G_b for each unit, the factor $\frac{4n}{(1+n)^2}$ is assumed to be unity.

The error caused by this approximation is less than 0.5 dB and is in such a direction to make a unit with an extreme conductance seem worse.

$$L = \frac{m^2 p}{G_b E_B^{\ 2}}$$

Since the modulation coefficient is difficult to measure, this equipment is calibrated with standard diodes measured by any absolute method.

$$L(dB) = 10 \log \frac{(m^2 p)}{(G_b)} = 20 \log E_B$$

A high impedance voltmeter can be used to measure 20 log E_B directly. The voltmeter is set on the 0.01 volt full scale, and the modulation voltage set so that the term 10 log(m^2p/G_p) is equal to 20.0 on the dB scale. To obtain this setting, the modulation is adjusted, so the voltmeter reading on the decibel scale is 20.0 minus the value of conversion loss for the standard diodes. This corresponds to a value of m of 1.58 percent for P = 1.0 mW and G_p = .0025 Ω. The conversion loss for unknown diodes is then 20.0 minus the reading of the output meter in decibels.

3.4 Test condition D (overall-noise-figure). The overall-noise-figure method derives the conversion loss by known properties of the apparatus and is expressed by the equation:

$$F_o = L(N + F_i - 1)$$

Where:

L = conversion loss of the mixer.

N = output noise ratio of the diode.

F_i = noise figure of the IF amplifier.

L is measured as described in method 4101 and N is measured as described in method 4121.

All terms are ratios.

4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 103, 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017, and C66053.

5. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test condition (see 3).

b. Load impedance (Z_m) (see 3.1).

c. Local oscillator power (see 3.2).

d. Load resistance (R_L) (see 3.1).

e. Local oscillator frequency (see 3.2).

METHOD 4102

MICROWAVE DIODE CAPACITANCE

1. Purpose. The purpose of this test is to measure the low frequency capacitance of a semiconductor diode. The capacitance is the small signal capacitance of the diode as measured in a defined test holder under specified bias conditions.

2. Test circuit. A bridge or meter should be used for the measurement. The specified signal level at the diode terminals, as measured with a suitable voltmeter, should be low enough so that a doubling of the level produces no measurable change in either the capacitance or shunt conductance of the diode. The test holder should be constructed so that the fringing capacitance is not altered by inserting the diode.

3. Procedure. The measurement shall be made at a specified frequency and bias voltage. A low frequency capacitance bridge or meter is used to measure the capacitance of the diode at a specified bias point. The effective case capacitance is measured in the same test holder as the diode. Junction capacitance may be determined by subtracting the effective case capacitance from the total measured capacitance.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Frequency (see 3).

b. Bias voltage (see 3).

c. Signal level at diode terminals (see 2).

d. Bias point (see 3).

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METHOD 4106

DETECTOR POWER EFFICIENCY

1. Purpose. The purpose of this test is to measure the detector power efficiency.

2. Test circuit. See figure 4106–1.

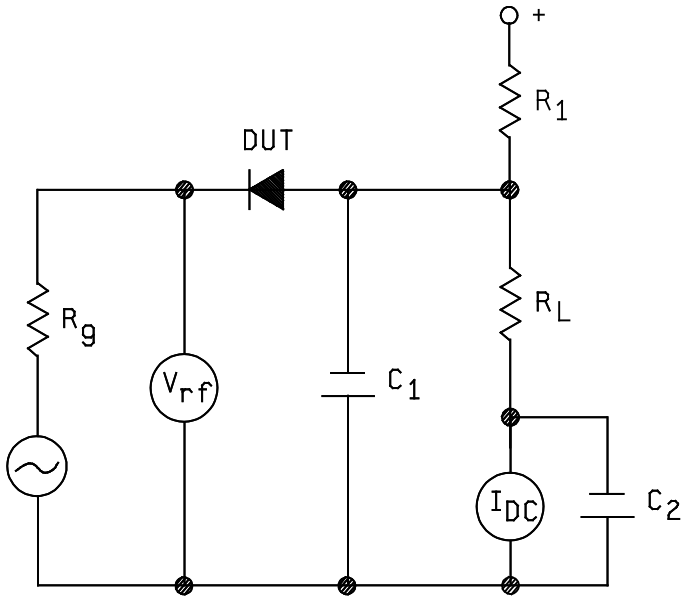

FIGURE 4106–1. Test circuit for detector power efficiency.

3. Procedure. Resistor R_L and capacitor C_1 comprise the load circuit and shall be as specified. Resistor R_1, in conjunction with R_L, provides the specified bias current for the DUT. Capacitor C_2 provides RF bypass for the output current meter I_{DC}. The frequency and amplitude of the ac signal and the output impedance of the generator shall be as specified. The change in output current I_{dc} is measured when the ac signal is applied.

$$Then: \ Detector\ power\ efficiency = \frac{4(\Delta I_{DC})^2 R_L R_G}{V^2 rms} x\, 100\ percent.$$

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Values for circuit components R_L and C_1 (see 3).

b. Bias current (see 2).

c. Frequency and amplitude of ac signal (see 3).

d. Impedance of signal generator (see 3).

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METHOD 4111.1

FIGURE OF MERIT (CURRENT SENSITIVITY)

1. Purpose. The purpose of this test is to measure the figure of merit of a semiconductor detector diode. The figure of merit is as follows:

$$M = \frac{\beta R_V}{\sqrt{R_V + R_a}}$$

2. Test circuit. The following test circuit shall apply. (See figure 4111–1).

NOTE: For power calibration.

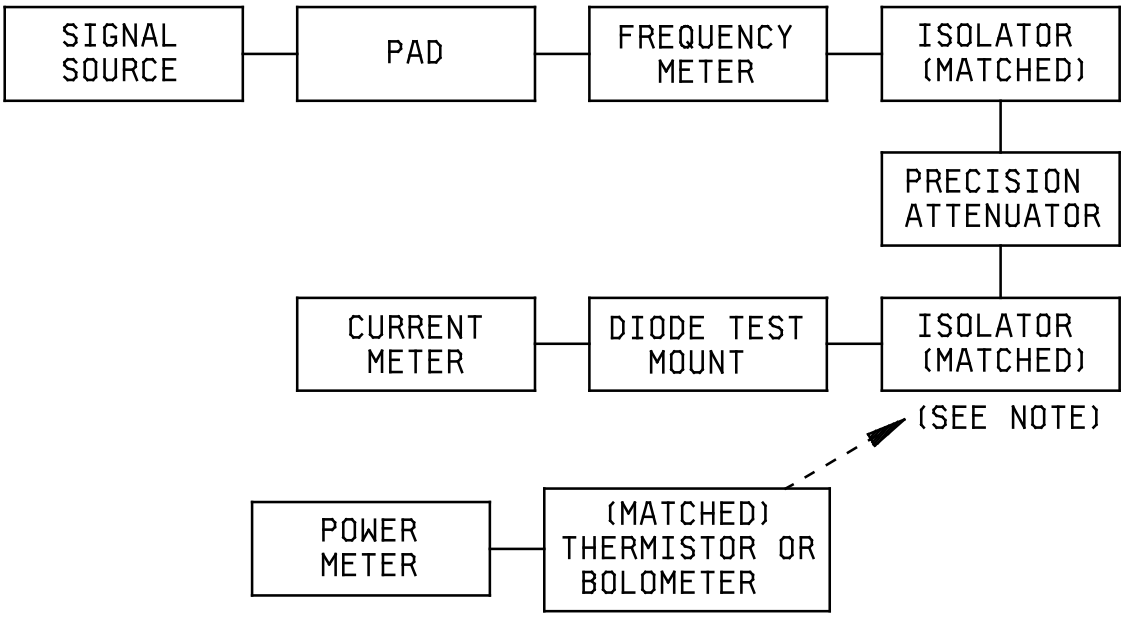

FIGURE 4111–1. Test setup for figure of merit measurement.

3. Procedure. The equipment for this test is shown on figure 4111–1. A continuous wave (cw) radio frequency (RF) signal is applied to the detector whose output short circuit current is measured and the short circuit current sensitivity (ß) is computed. The figure of merit (M) is then determined from:

$$M = \frac{\beta R_V}{\sqrt{R_V + R_a}}$$

Approximate method:

$$M = \beta\, 2\sqrt{R_X}\ \frac{1 + 1/2\zeta}{\sqrt{1+\zeta}}$$

Where:

ß = i/P

and

i = short circuit diode current

P = power incident at the diode holder

Where:

$$R_X = \frac{1}{\sqrt{(R_1 + R_a)(R_2 + R_a)}}$$

and

R_1 = lower limit of video resistance

R_2 = upper limit of video resistance

R_a = equivalent amplifier noise generating resistance.

and where:

$$\frac{1 + 1/2\zeta}{\sqrt{1+\zeta}}\ \textit{is the correction factor}$$

and:

$$\zeta = \frac{R_V + R_a}{R_X} - 1$$

When the extreme values of the video resistance for a given diode type are known, it is possible to relate figure of merit to rectified current if other conditions are satisfied.

For all normal ranges of video resistance, the correction factor is very close to unity and an approximation:

$$M = 2\beta\sqrt{R_X}$$

therefore, the figure of merit (M) may be determined by measuring the rectified current under proper conditions.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test oscillator frequency (see 2).

b. Maximum permissible test oscillator power (see 2).

c. DC bias if supplied by an external source.

d. Ra, if other than 1,200Ω.

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METHOD 4116.1

INTERMEDIATE FREQUENCY (IF) IMPEDANCE

1. Purpose. The purpose of this test is to measure the real part of the impedance at the IF output terminals of the mixer diode under test.

2. Test circuit. The following test circuits shall apply. (See figures 4116–1 and 4116–2).

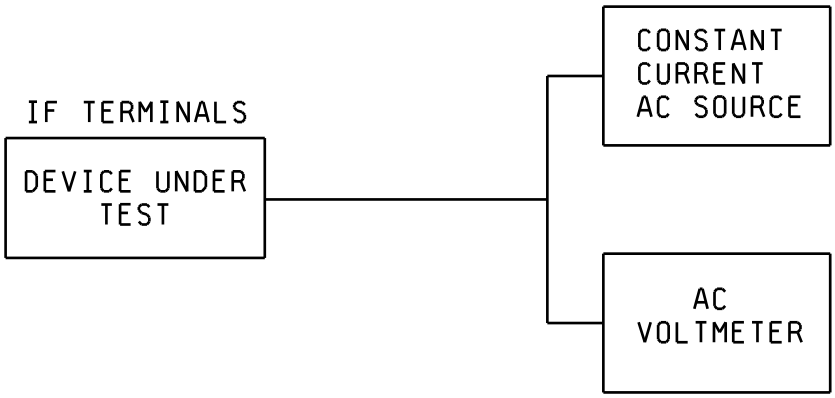

FIGURE 4116–1. AC method.

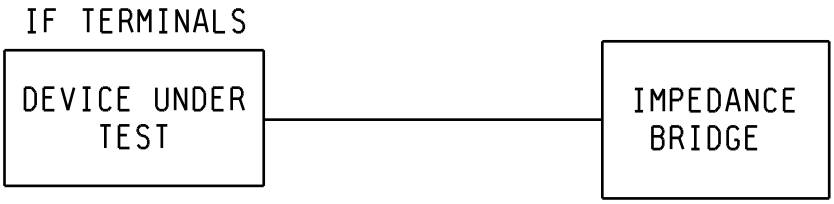

FIGURE 4116–2. Impedance bridge method.

3. Procedure. Since the IF resistance is the slope of the mixer diode's I-V characteristic under the specified test conditions, the requirement of any measuring technique is to measure the slope without affecting the operating characteristics of the DUT. At all times, the device holder RF input port should see a broadband match (minimum of two times IF frequency). The IF test frequency, local oscillator frequency, and power shall be specified.

3.1 Test condition A (ac). With equipment arranged as shown on figure 4116-1, a constant current ac generator is coupled to the diode under test. The dc and ac diode loads are arranged as specified and the ac current is set at a level low enough so that halving the level produces a change in the measured IF impedance of the diode of less than 5 percent. The IF impedance is calculated as follows:

$$Z_{if} = \frac{V}{I}$$

Where:

Z_{if} = diode IF impedance.
V = measured ac voltage.
I = ac current.

3.2 Test condition B (impedance bridge). The equipment is arranged as shown on figure 4116-2. The impedance bridge signal level is adjusted to a low level using the same criterion in 3.1. The diode IF impedance is determined from the impedance bridge.

4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017, and C66053.

5. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test condition (see 3).

b. Local oscillator frequency (see 3).

c. Local oscillator power or diode rectified current (see 3).

d. DC load resistance (see 3.1 and 3.2).

e. AC load impedance (see 3.1 and 3.2).

f. IF test frequency (see 3).

g. DC bias, if applicable.

METHOD 4121.2

OUTPUT NOISE RATIO

1. Purpose. The purpose of this test is to measure the output noise ratio of a mixer diode. Since the output noise ratio is a measure of the excess noise generated by a mixer diode in its normal operating condition, the measurement should be in the appropriate standard holder.

2. Test circuit. The following test circuits shall apply. (See figures 4121-1 and 4121-2).

FIGURE 4121–1. Direct measurement method.

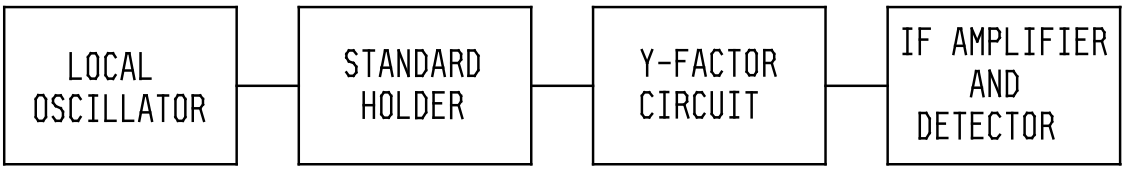

FIGURE 4121–2. Y-factor method.

3. Procedure.

3.1 Test condition A (direct measurement). In this method, the output noise ratio is determined by establishing a reference output reading on the output meter shown on figure 4121-1, with the diode operating under specified test conditions, then a resistor equal to the specified IF impedance of the diode is substituted for the diode. The resistor becomes noisy when the current passes from a noise diode (temperature limited diode). Value for noise resistor shall be specified. The current is adjusted to provide the reference output reading and the noise ratio is computed from the relationship:

$$N = \frac{e\,IR}{2\,kT_o} + 1 = 20\,IR + 1$$

Where:

T_o = +293°K ±5°K and I is the current of the noise diode in amperes.

R = the resistance of the noise resistor.

k = Boltzmann's constant (1.38×10^{-23} joules per °K).

e = the electronic charge (1.6×10^{-19} coulombs).

3.2 Test condition B (computational). In this method, the output noise ratio is determined from the equation:

$$N = \frac{\bar{F}_o}{L} - \bar{F}_i + 1$$

Where:

F_o = overall receiver noise figure.

L = diode conversion loss.

$\bar{F}_i$ = noise figure of the IF amplifier.

All terms are ratios.

F_o and $\bar{F}_i$ are determined as described in test method 4126; L is determined as described in method 4101.

3.3 Test condition C (Y-factor). In this method, the output noise ratio is determined by establishing a reference output reading on the output meter shown on figure 4121-2, with the diode operating under specified test conditions, then a resistor equal to the specified IF impedance of the diode is substituted for the diode by a switch in the Y-factor circuit. The output noise ratio is then determined from:

$$N = \bar{F}_i (Y - 1) + 1$$

Where:

$Y = N_{oc}/N_{or}$

N_{oc} is the reference output reading on the output meter with the diode connected to the circuit.

N_{or} is the output reading with the resistor connected to the circuit.

$\bar{F}_i$ is determined as described in method 4126.

All terms are ratios.

4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 103, 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017 and C66053.

5. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test condition (see 3).

b. Local oscillator frequency (see 2).

c. Local oscillator power (see 2).

d. IF frequency (see 2).

e. Value for noise resistor (see 3.1).

f. DC bias, if applicable.

METHOD 4126.2

OVERALL NOISE FIGURE AND NOISE FIGURE OF THE IF AMPLIFIER

1. Purpose. The purpose of this test is to measure the overall noise figure of a mixer diode and the noise figure of the associated IF amplifier. Since the noise figure of a network is defined as follows:

$$\overline{F}_O = \frac{(available\,input\,signal\;power)/(available\,input\,noise\;power)}{(available\,output\,signal\;power)/(available\,output\,noisepower)}$$

It is necessary to measure the noise power that is actually delivered to the output termination. This measurement is divided by a similar measure of the output noise that would have been obtained if the network were noiseless and only transmitted the thermal noise of the input termination. In making noise figure measurements, the standard practice is to provide matched impedance at the signal and image frequencies and make suitable corrections (by calculations or appropriate filtering) to obtain an equivalent single-side-band noise figure. The noise figure obtained without a signal band-pass filter to eliminate the image-frequency band is commonly referred to as the double-side-band noise figure and is approximately 3 dB smaller than the single-side-band noise figure, depending on the exact transmission characteristics of the particular mixer. If a single-side-band noise figure is being measured directly, it is necessary to terminate the image resistively in a matched load (isolator) to avoid errors due to second-order effects. These second-order effects may arise from reflection of the image back into the mixer to give a larger or smaller than true value of noise figure, depending on the phase of the reflected image.

2. Apparatus. The apparatus shall be arranged as follows. (See figure 4126-1).

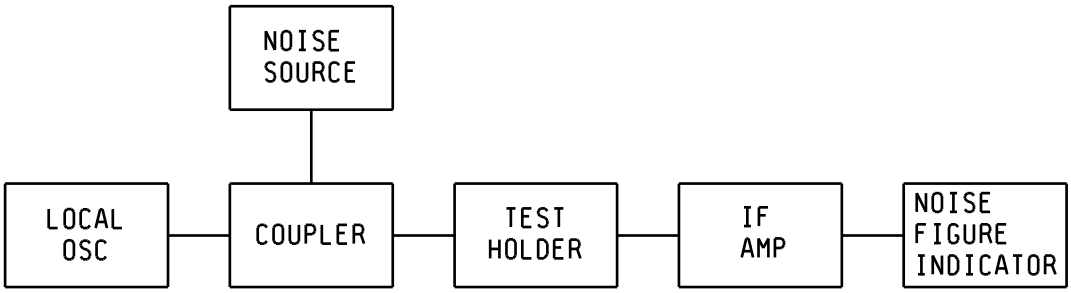

FIGURE 4126–1. Test setup for overall noise figure.

3. Procedure. When using test conditions A and C, the local oscillator frequency and power, IF, and excess noise ratio of noise source shall be specified.

3.1 Test condition A (dispersed-signal-source). A signal source with available power dispersed uniformly over the pass band of the network, and calibrated in terms of available power per unit bandwidth, is used to determine that portion of the output noise power that results from the input termination noise. Suitable dispersed-signal generators are thermionic-noise diodes, gas discharge tubes, resistors of known temperature, or an oscillator whose frequency is swept through the band at a uniform rate. Single-side-band noise figure is obtained by adding 3 dB to the measured (double-side-band) noise figure. At all times, the device holder rf input should see a broadband match (minimum of two times IF frequency).

3.2 Test condition B (computation). Assuming the IF amplifier noise figure is known, the overall noise figure can be computed as follows:

$$\overline{F}_O = L\left(N + \overline{F}_i - 1\right)$$

Where:

L = diode conversion loss.

N = output noise ratio of the diode.

$\overline{F}_i$ = noise figure of the IF amplifier.

L is measured as described in test method 4101 and N is measured as described in test method 4121.

All terms are ratios.

3.3 Test condition C (IF amplifier noise figure). Resistors in the particular diode type cases are required, constructed so that when they are inserted in the standard holder (mixer), the output susceptance of the holder is approximately the same as when the diodes are inserted. A sufficient number of resistors should be used so that the output conductance of the standard holder may be finely varied over the specified maximum range for the diode type. A common junction (defining the mixer IF port) joins the holder to the IF amplifier and the noise (temperature-limited diode). The entire circuit, including the noise diode power supply and the current meters, shall be well shielded or filtered to avoid IF feedback. With the resistor in the holder, the IF amplifier gain is adjusted to give an output meter reference reading near full scale. Precise IF attenuation is then inserted, and the noise diode turned on and adjusted in emission to restore the output meter reference reading. The average (dc) noise anode current is then noted and used to compute the IF average noise figure from:

$$F_i = 1 + \frac{eIR}{2kT_o(A-1)} - \frac{T_a}{T_o}$$

$$F_i = 1 + \frac{20IR}{A-1} - \frac{T_a}{T_o}$$

Where:

F_i = noise figure of the IF amplifier (power ratio).

e = electronic charge (1.6×10^{-19} coulombs).

k = Boltzmann's constant (1.38×10^{-23} joules per °K).

T_o = standard noise temperature (+293°K).

T_a = temperature of resistor (°K).

A = inserted IF attenuation (power ratio).

I = average (dc) noise diode current (amperes).

R = reciprocal of IF conductance (ohms).

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test condition (see 3).

b. Local oscillator frequency (see 3).

c. Local oscillator power (see 3).

d. IF (see 3).

e. DC bias, if bias is supplied by an external source.

f. Excess noise ratio of noise source (see 3).

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METHOD 4131.1

VIDEO RESISTANCE

1. Purpose. The purpose of this test is to measure the video resistance of the device. Video resistance shall be defined as the reciprocal of the slope of the current versus voltage characteristic curve at the operating point.

2. Test circuits. The test circuits shall be as follows. (See figures 4131–1 through 4131–4).

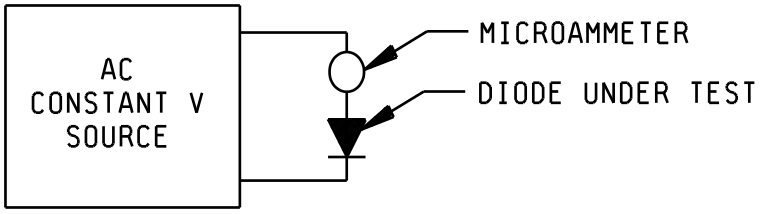

FIGURE 4131–1. Constant voltage method.

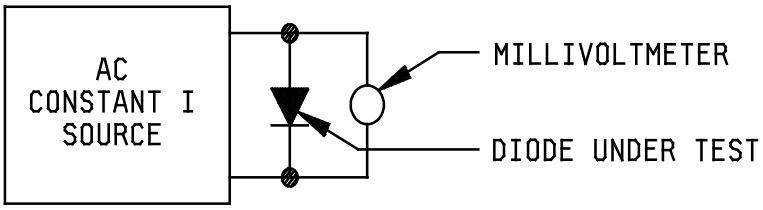

FIGURE 4131–2. Constant current method.

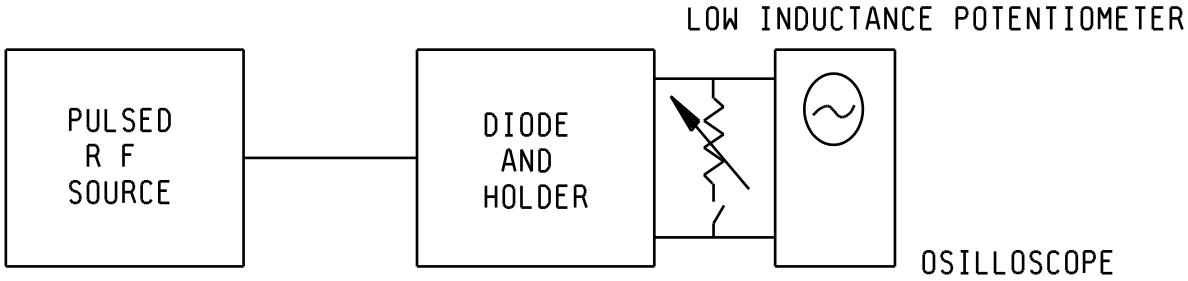

FIGURE 4131–3. Pulsed RF method.

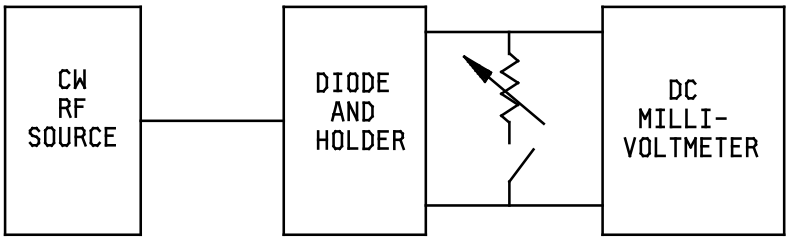

FIGURE 4131–4. Continuous wave RF method.

3. Procedure. The measurement shall be made with the diode operating under the specified test conditions. The applied signal used and the instrument impedance shall be such that doubling or halving their value does not change the video impedance by more than ±5 percent.

3.1 Test condition A (constant voltage). Test equipment used is shown on figure 4131-1. A small specified ac signal is applied to the diode from a constant voltage source. Current is measured with a low resistance microammeter. R_V equals e/i.

3.2 Test condition B (constant current). Test equipment used is shown on figure 4131-2. A small specified ac current is passed through the diode from a constant current source. The voltage is measured across the device with a high impedance millivoltmeter. R_V equals e/i.

3.3 Test condition C (pulsed RF). Test equipment used is shown on figure 4131-3. A pulsed rf signal, as specified, is fed to the diode whose output is fed into the vertical amplifier of an oscilloscope. A resistor is placed in parallel with the device and varied to lower the rectified pulse to half its value. R_V equals the resistance required to halve the pulse. Bandwidth of vertical amplifier should be a minimum of two times the reciprocal of the pulse width.

3.4 Test condition D (continuous wave (cw) radio frequency (RF)). Test equipment used is shown on figure 4131-4. A specified cw RF signal is applied to the detector whose output open circuit rectified voltage is measured on a high impedance dc millivoltmeter. A resistor is placed in parallel with the device and varied to lower this voltage to half its initial value. R_V equals the resistance required to halve the voltage.

4. Summary. The following conditions shall be included in the applicable performance specification sheet or acquisition document:

a. Test condition (see 3).

b. Maximum signal voltage (see 3.1).

c. Maximum current (see 3.2).

d. Maximum power (see 3.3 and 3.4).

e. DC bias, if applicable.

METHOD 4136.1

STANDING WAVE RATIO (SWR)

1. Purpose. The purpose of this test is to measure the SWR of the device at the local oscillator terminals. SWR shall be defined as the ratio of the maximum voltage (or current) to the minimum voltage (or current) along the transmission line between the device and the local oscillator terminals. The measurement shall be made with the diode operating under normal operating conditions.

2. Test circuits. The test circuits shall be as follows: (See figures 4136-1, and 4136-2).

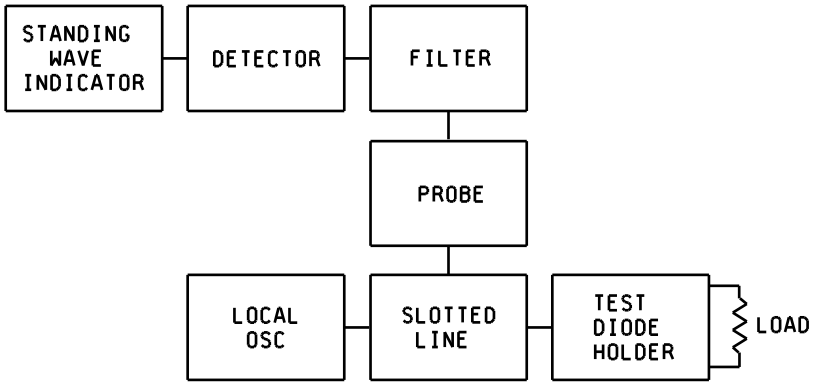

FIGURE 4136–1. Slotted line method.

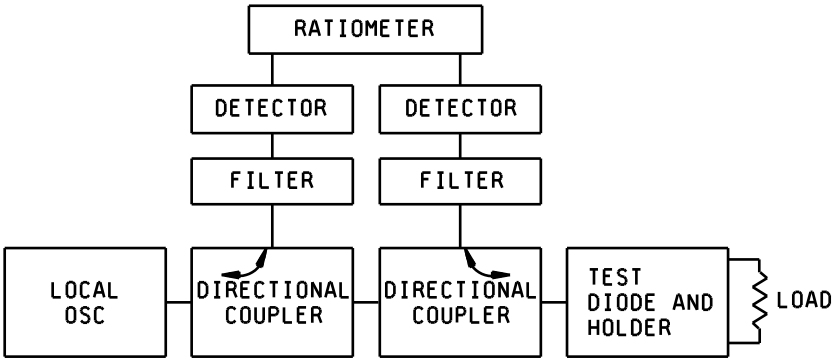

FIGURE 4136–2. Reflectometer method.

3. Procedure.

3.1 Test condition A – slotted line. A slotted line is inserted between the device in its holder and the local oscillator, and the probe is moved to determine the maximum and minimum voltage or current points. To limit probe errors and keep the power in the slotted line section at a level high enough to operate the standing wave indicator and low enough to maintain small signal conditions, the normal signal generator and indicator connections to the slotted line as shown on figure 4136-1 should be interchanged. That is, the signal generator should be connected to the moving probe and the detector indicator should be connected to the slotted line section opposite the test diode holder.

a. The power source may be used without modulation if a sensitive galvanometer is substituted for the standing wave indicator (tuned voltmeter).

b. The dc load resistance is set to that specified.

c. Insert diode into test holder.

d. Adjust frequency and power level to those specified.

e. Move the probe in the slotted line until the standing wave indicator shows at voltage maximum (or current). Adjust the range switch and gain until an SWR of 1 is indicated.

f. Move the probe until a minimum is indicated.

g. Read the SWR directly at the minimum point.

3.2 Test condition B – reflectometer. A calibrated reflectometer is inserted between the device in its holder and the local oscillator; then the SWR is read, see figure 4136-2.

a. Adjust frequency and power level to those specified.

b. The dc load resistance is set to that specified.

c. Insert diode into the test holder.

d. The reflection coefficient and the SWR can be read directly.

NOTE: When this technique is used, the filter detector combination shall have an SWR < 1.2.

4. Summary. The following conditions shall be as specified in the applicable performance specification sheet or acquisition document:

a. Test condition (see 3).

b. DC load resistance (see 3.1 and 3.2).

c. Test frequency (see 3.1 and 3.2).

d. Power level (see 3.1 and 3.2).

e. Maximum voltage (or current), if applicable.

METHOD 4141.1

BURNOUT BY REPETITIVE PULSING

1. Purpose. The purpose of this test is to determine the capabilities of the device to withstand repetitive pulses.

2. Test circuit. See figure 4141–1.

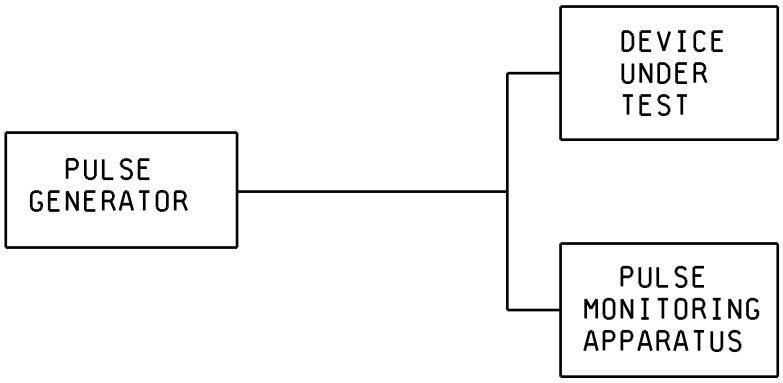

FIGURE 4141–1. Test setup for repetitive pulsing.

3. Procedure. This method shall be acceptable to determine the device capability to withstand repetitive pulses. The general method of measuring device capability to withstand burnout by repetitive pulsing is to apply the specified number of pulses to the DUT and then measure the specified electrical parameters. The pulse polarity shall be such as to cause the current to flow in the forward direction. When the maximum change in the specified electrical parameter is exceeded, the device shall have failed to meet this burnout test. The pulse generator source impedance shall be specified. While the device to be tested is not in the circuit, adjust the pulse generator output for the specified open-circuit pulse voltage, pulse width, and pulse repetition rate. Then insert the device in the circuit. The device shall be left in the circuit for a minimum specified time.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Pulse generator source impedance (see 3.).

b. Pulse width (see 3).

c. Pulse voltage (see 3).

d. Pulse repetition rate (see 3).

e. Minimum time that the device is under test (see 3).

f. Polarity of applied pulse (see 3).

g. Minimum pulse energy per pulse absorbed by diode, if applicable.

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METHOD 4146.1

BURNOUT BY SINGLE PULSE

1. Purpose. The purpose of this test is to determine the capability of the device to withstand a single pulse.

2. Test circuit. The test circuit shall be as follows: (See figure 4146–1).

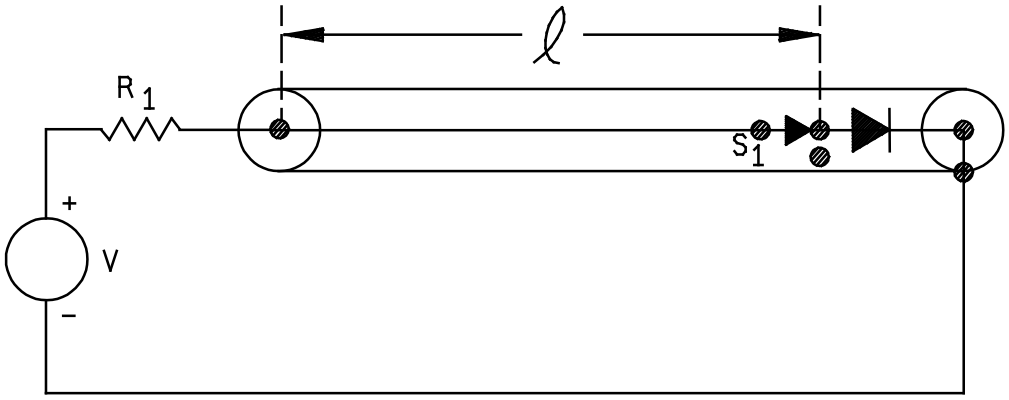

FIGURE 4146–1. Burnout by single pulse.

3. Procedure. The device shall be subjected to a pulse from the coaxial line shown on figure 4146-1. The line shall be charged with the specified voltage, and the contact shall be made by dropping the center conductor vertically from a height of 2 ±.05 inches (50.8 ±1.27 mm) above the contact position. The electrical and mechanical connection shall be such as to have a minimum effect on the free fall of the conductor. The polarity of the inner conductor with respect to the outer conductor shall be such as to cause the device current to flow in the forward direction or as specified.

4. Detail drawings. DSCC drawings B66054 and C66058 as applicable, are used to perform this test.

5. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test voltage (see 3).

b. Polarity, if required.

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METHOD 4151

RECTIFIED MICROWAVE DIODE CURRENT

1. Purpose. The purpose of this test is to measure the rectified microwave diode current under conditions for conversion loss.

2. Apparatus. The apparatus used for this test should be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The rectified microwave diode current shall be measured under the conditions for conversion loss. The test shall be conducted in the mixer shown on the specified drawing under the conditions specified for the conversion loss test.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

   a. Test apparatus (see 2).

   b. Conversion loss test conditions (see 3).

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METHOD 4201.2

HOLDING CURRENT

1. Purpose. The purpose of this test is to measure the holding current of the device under the specified conditions.

2. Test circuit. See figure 4201–1.

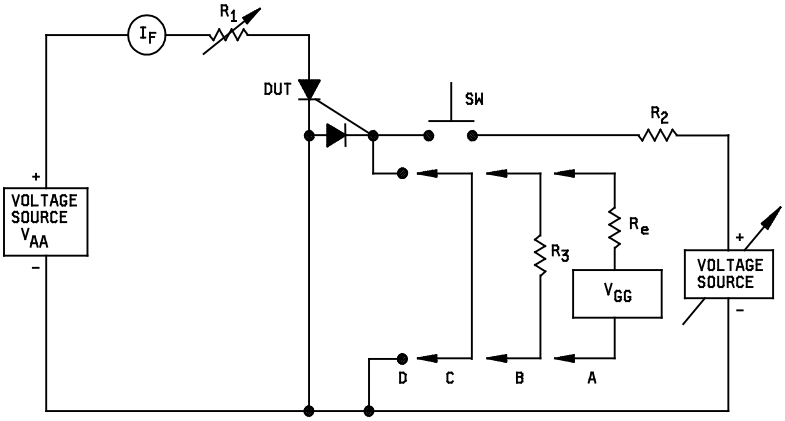

FIGURE 4201–1. Test circuit for holding current.

3. Procedure. The anode supply voltage is set at its specified value with resistance R_1 adjusted so that the initial forward current, I_{F1}, which flows when the device is triggered, equals the value specified. Switch SW is then momentarily closed to trigger the device and reopened. The initial current is quickly reduced to the specified test current I_{F2}. Then the specified gate bias condition is applied. The resistance R_1 is then gradually increased, until the device turns off. The value of forward current immediately prior to turn-off is the holding current.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Anode supply voltage, V_{AA}.

b. Initial forward current, I_{F1}.

c. Forward test current, I_{F2}.

d. Bias condition, gate to cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_3).

C: Short-circuit.

D: Open-circuit.

e. Gate trigger source voltage, open circuit magnitude and pulse width.

f. Total gate trigger circuit resistance, R_2.

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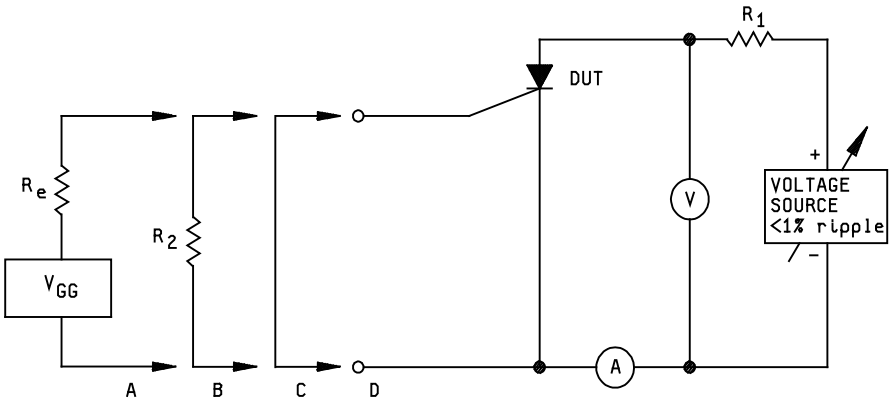
METHOD 4206.1

FORWARD BLOCKING CURRENT

1. Purpose. The purpose of this test is to measure the forward blocking current under the specified conditions, using the dc method or the ac method, as applicable.

2. DC method.

2.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device switches to the on state. (See figure 4206–1).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4206–1. Test circuit for forward blocking current (dc method).

2.2 Procedure. The supply voltage is adjusted to obtain the specified value of forward voltage across the device with the specified gate bias condition applied (see figure 4206-1). The forward blocking current is then read from the current meter.

2.3 Summary for DC method. The following conditions shall be specified in the applicable specification sheet:

a. DC method.

b. Test voltage.

c. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

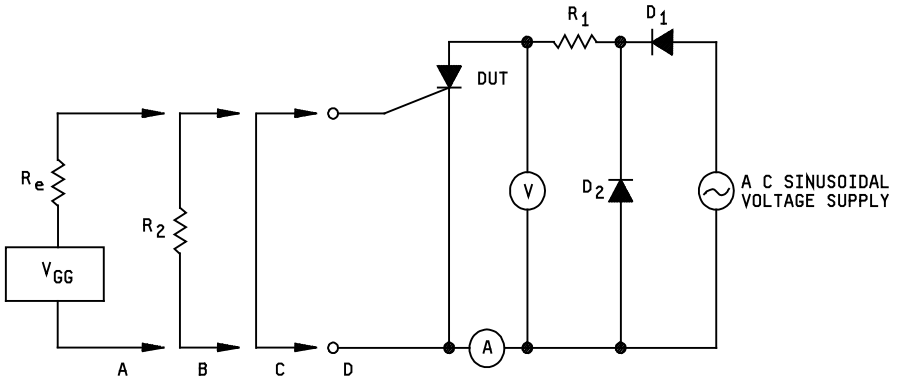
B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

3. AC method.

3.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device switches to the on state. D_1 and D_2 are diodes capable of blocking the peak value of the ac voltage supply. Peak reading techniques shall be used to measure the necessary parameters. (See figure 4206–2).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4206–2. Test circuit for forward blocking current (ac method).

3.2 Procedure. The peak supply voltage is adjusted to obtain the specified peak forward voltage across the device with the specified gate bias condition applied (see figure 4206–2). The peak forward blocking current is then read from the current indicator. Voltage should be gradually applied to prevent turn-on of the device due to excessive dv/dt.

3.3 Summary for AC method. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. AC method.

b. Peak forward test voltage.

c. Frequency.

d. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

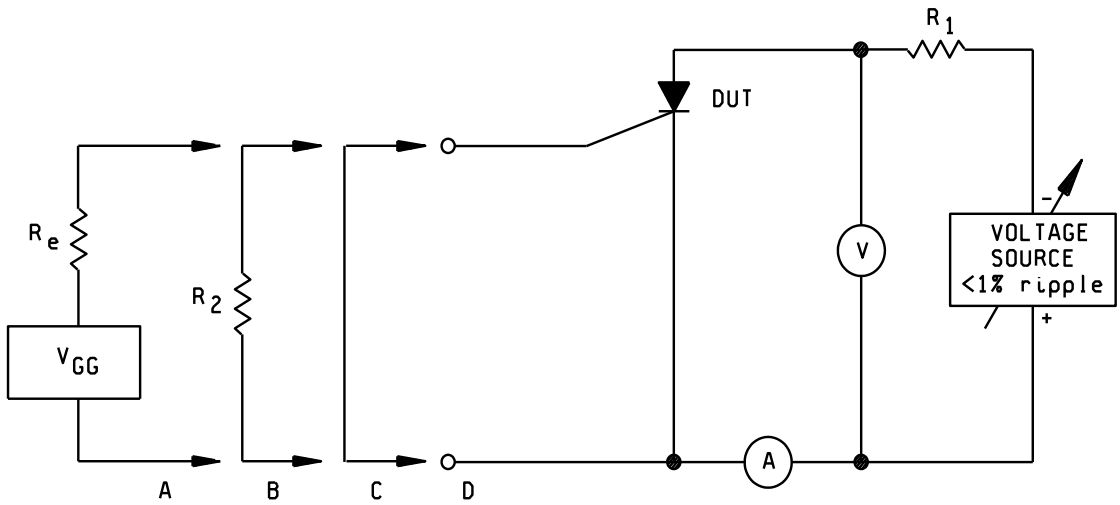
METHOD 4211.1

REVERSE BLOCKING CURRENT

1. Purpose. The purpose of this test is to measure the reverse blocking current under the specified conditions, using the dc method or the ac method, as applicable.

2. DC method.

2.1 Test circuit. R_1 shall be chosen to limit the current flow in the event of the device goes into reverse breakdown.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the readings shall be corrected for the drop across the ammeter.

FIGURE 4211–1. Test circuit for reverse blocking current (dc method).

2.2 Procedure. The supply voltage is adjusted to obtain the specified value of reverse voltage across the device with the specified gate bias condition applied (see figure 4211–1). The reverse blocking current is then read from the current meter.

2.3 Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. DC method.

b. Test voltage.

c. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

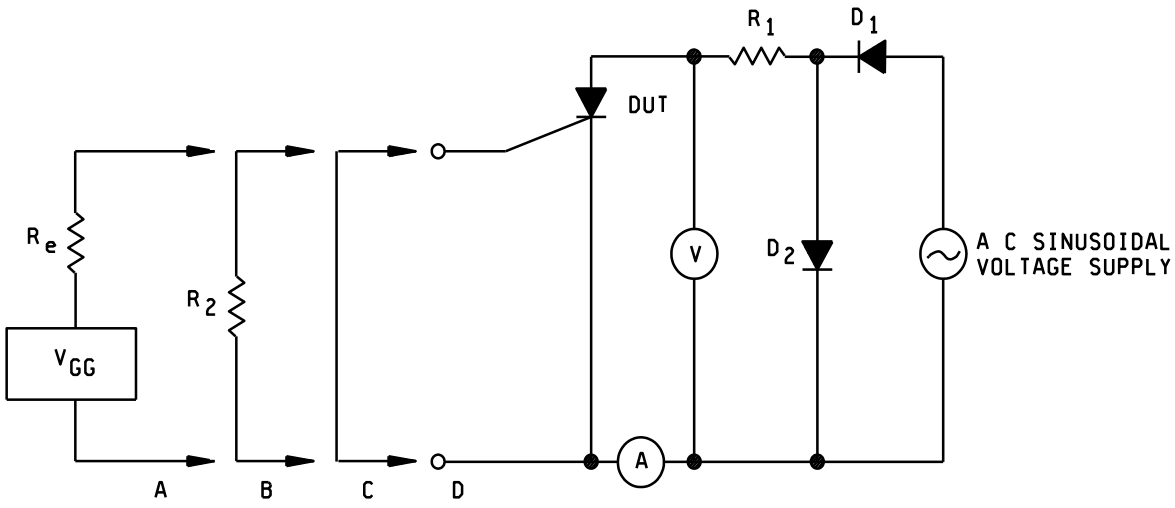
B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

3. AC method.

3.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device goes into reverse breakdown. D_1 and D_2 are diodes capable of blocking the peak value of the ac voltage supply. Peak reading techniques shall be used to measure the necessary parameters. (See figure 4211–2).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4211-2. Test circuit for reverse blocking current (ac method).

3.2 Procedure. The peak supply voltage is adjusted to obtain the specified peak reverse voltage across the device with the specified gate bias condition applied (see figure 4211–2). The peak reverse blocking current is then read from the current indicator.

3.3 Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. AC method.

b. Peak reverse test voltage.

c. Frequency.

d. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

METHOD 4216

PULSE RESPONSE

1. Purpose. The purpose of this test is to measure the pulse response of the device under the specified conditions.

2. Test circuit. See figure 4216–1.

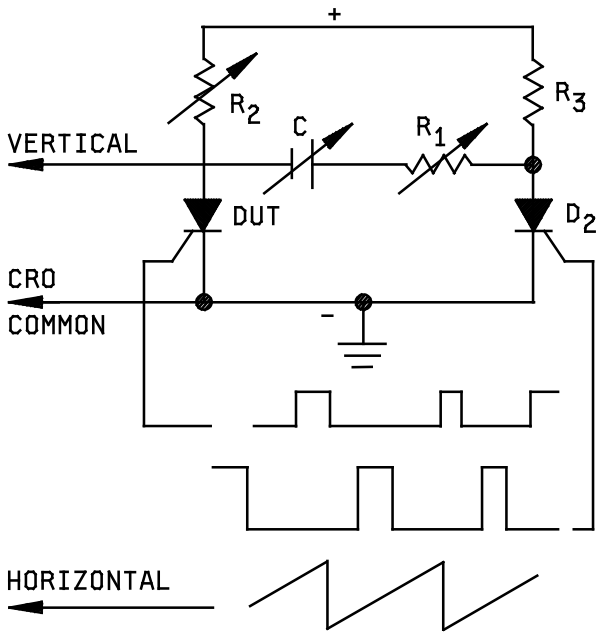


FIGURE 4216–1. Test circuit for pulse response.

3. Procedure. The pulse response of the device shall be measured in the circuit on figure 4216–1. R_2 is adjusted to permit the specified value of forward current to flow in the device being measured when it is the on-state. C, R_1, and the secured controlled rectifier, D_2, are used to switch off the device being measured. C shall be large enough to ensure that the device will turn off. R_1 limits the recurrent peak reverse current to below the rated value. The pulse repetition rate should be low enough to ensure that the anode-cathode voltage of the device being measured reaches the value of forward working voltage specified for the measurement.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Anode voltage (see 3).

b. Resistor R_2 (see 3).

c. Test current.

d. Repetition rate.

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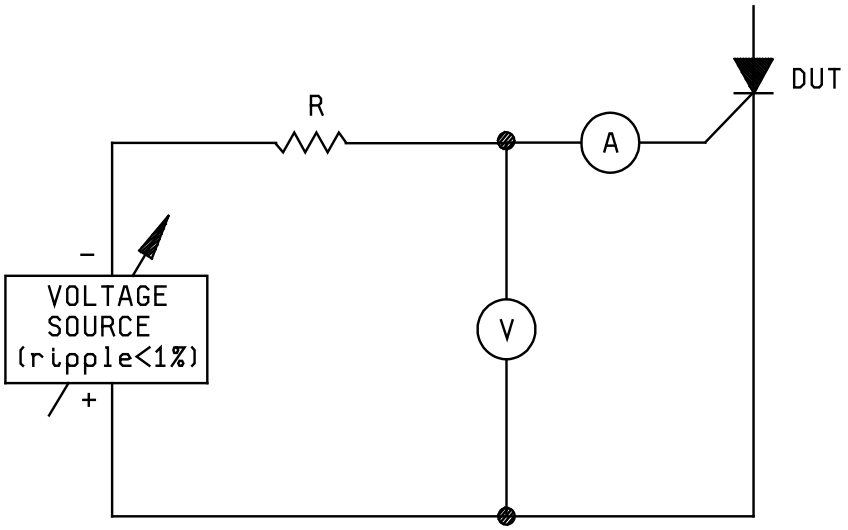
METHOD 4219

REVERSE GATE CURRENT

1. Purpose. The purpose of this test is to measure the dc reverse gate current of the device at a specified reverse gate voltage.

2. Test circuit. R is chosen to limit the current in the event the reverse gate breakdown voltage is exceeded. (See figure 4219–1).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4219–1. Test circuit for reverse gate current.

3. Procedure. Set the specified reverse gate voltage and read the reverse gate current.

4. Summary. The dc reverse gate voltage shall be specified in the applicable performance specification sheet or acquisition document:

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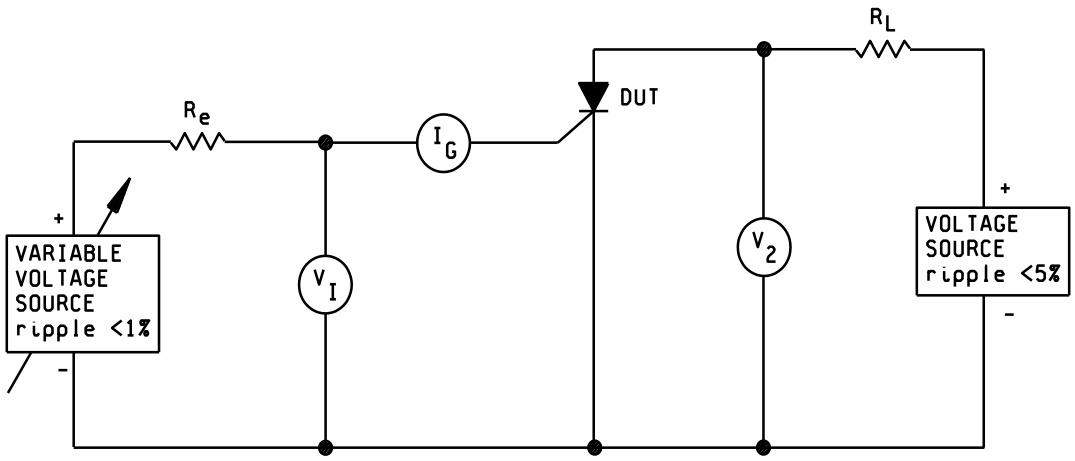
METHOD 4221.1

GATE-TRIGGER VOLTAGE OR GATE-TRIGGER CURRENT

1. Purpose. The purpose of this test is to measure the dc gate-trigger voltage or dc gate-trigger current.

2. Test circuit. Care should be taken to minimize noise or spurious signals in the trigger circuit (see figure 4221-1).



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4221–1. Test circuit for gate-trigger voltage or gate-trigger current.

3. Procedure. The anode voltage, V_2, is set to the specified value. The gate voltage, V_1, is slowly increased from zero. The gate-trigger current or gate-trigger voltage is read as the highest value achieved prior to a sharp decrease in anode voltage.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Anode voltage, V_2 (see 3).

b. Load resistance, R_L.

c. Equivalent gate circuit resistance, R_e (the resistance looking into the gate circuit from the DUT gate-to-cathode terminals).

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METHOD 4223

GATE-CONTROLLED TURN-ON TIME

1. Purpose. The purpose of this test method is to measure the time between initiation (10 percentage point) of gate pulse and the time at which the output pulse is at 90 percent of its final value.

2. Test circuit. The anode circuit loop L/R shall be >0.01 and <0.1 of the forward current rise time, t_r. The open-circuit, gate-voltage rise time shall be <0.1 of the delay time, t_d of the DUT. V_{AA} must have stabilized at its peak value prior to triggering the gate pulse generator. (See figures 4223–1 and 4223–2.)

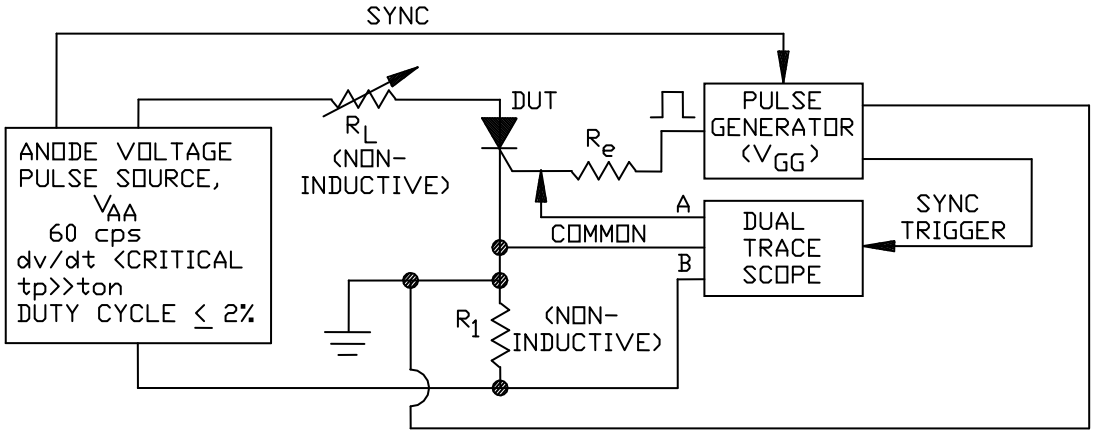


FIGURE 4223–1. Test circuit for gate-controlled turn-on time.

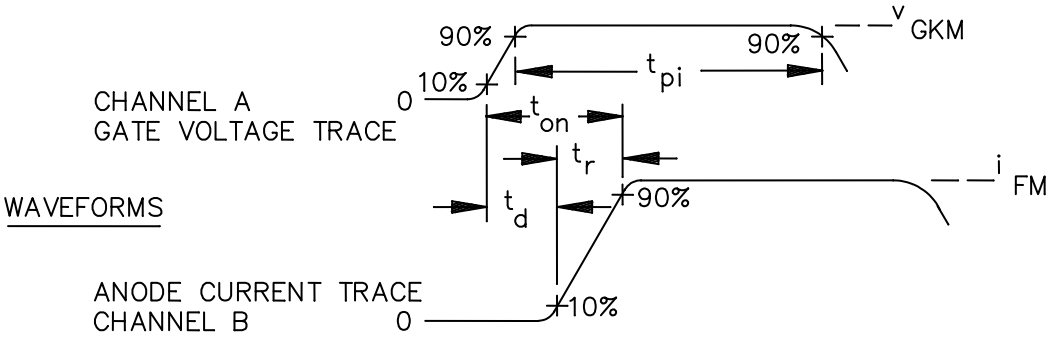


FIGURE 4223–2. Waveforms, gate-controlled turn-on time.

3. Procedure. Set the anode voltage pulse source and the gate conditions as specified. Adjust R_L to achieve the specified i_{FM}. The turn-on time is then read from the dual trace scope as shown on figure 4223–2.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Peak anode supply voltage, V_{AA}.

b. Peak forward current, i_{FM}.

c. Peak open-circuit, gate supply voltage, V_{GG}.

d. Gate pulse width, t_{p1}.

e. Equivalent gate-source resistance, R_e.

f. Minimum and maximum allowable di/dt of the forward current pulse.

METHOD 4224

CIRCUIT-COMMUTATED TURN-OFF TIME

1. Purpose. The purpose of this test method is to measure the turn-off time of the device under the specified conditions.

2. Test circuit. (See figures 4224–1, and 4224–2).

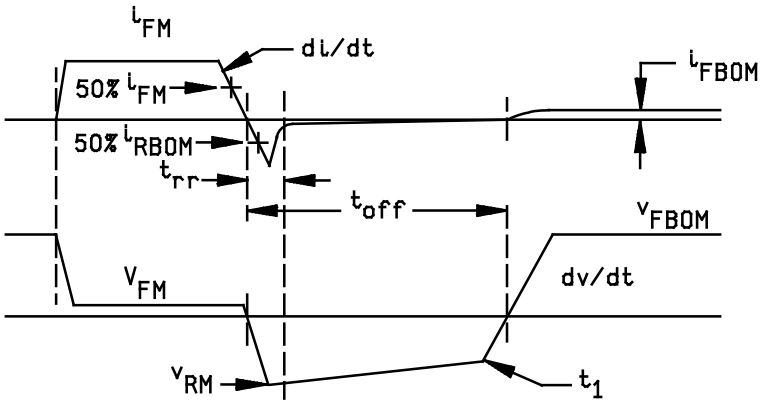
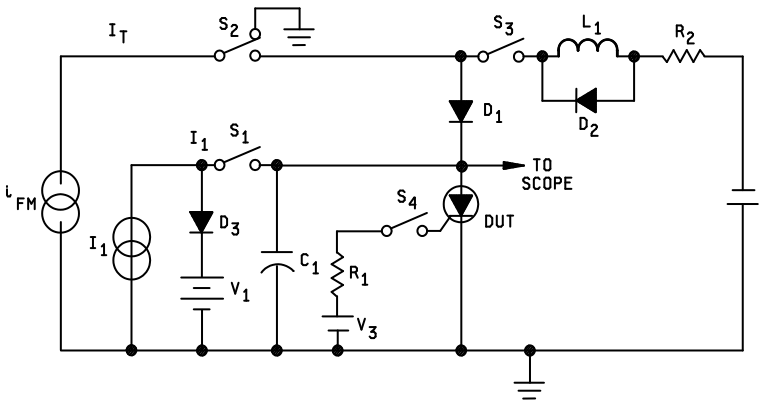


FIGURE 4224–1. Circuit-commutated turn-off time waveforms.



NOTE: The simplified circuit diagram on figure 4224–2 illustrates the operating principles of a circuit used to generate the waveforms illustrated on figure 4224–1. For purposes of clarity, the circuit diagram utilizes current generators, ideal switches, and no provision for repetitive test cycles.

FIGURE 4224–2. Test circuit for circuit-commutated turn-off time.

3. Test description. The test is performed by first causing the thyristor under test to conduct the specified on-state current at the specified thermal condition. This current is conducted for the specified time (a period long enough to establish carrier equilibrium). Next, the current is reversed through the thyristor at the specified rate (di/dt) by means of an externally applied reverse blocking voltage. The reverse current recovers stored charge from the anode and cathode junctions of the thyristor, allowing the thyristor to support the specified reverse blocking voltage. A further waiting time is required for the collector junction charges to recombine before the thyristor is capable of blocking forward voltage. Since this recombination cannot be observed directly, the test is performed by applying an off-state voltage at the specified rate of rise (dv/dt) after successively shorter waiting times until it is observed that the thyristor is unable to support the off-state voltage (without switching to the on-state). The thyristor current and voltage waveforms are illustrated on figure 4224–1.

4. Procedure.

a. S_2 and S_4 are closed simultaneously causing the thyristor under test to switch to the on-state and conduct the specified current i_{FM}; S_4 is then opened to disconnect the gate trigger supply R_1 and V_3.

b. After the specified on-state current duration, S_3 is closed to cause current reversal. The rate of current change (di/dt) is determined by L_1 and R_2. Diode D_2 prevents a commutation voltage transient when the thyristor under test begins to recover its reverse blocking capability. Diode D_1 shall have a longer reverse recovery time than the thyristor under test so that the reverse voltage appears across the thyristor under test.

c. The application of off-state voltage is initiated by closing S_1. The current I_1 completes the reverse recovery of D_1 and is then diverted to C_1. C_1 charges linearly with time at a rate equal to I_1/C_1 producing the required dv/dt illustrated on figure 4224–1. This voltage rises to a value equal to V_1 which is adjusted to the specified off-state voltage.

5. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. On-state current amplitude.

b. On-state current duration, t_{on}.

c. Commutation rate (di/dt) (the slope of the line from 50 percent of + peak to 50 percent of - peak).

d. Peak reverse voltage (maximum).

e. Reverse voltage at t_1 (minimum).

f. Operating temperature.

g. Test repetition rate.

h. Rate of rise of reapplied off-state voltage (dv/dt).

i. Off-state voltage.

j. Gate bias conditions (between gate trigger pulses):

(1) Gate-source voltage.

(2) Gate-source resistance.

METHOD 4225

GATE-CONTROLLED TURN-OFF TIME

1. Purpose. The purpose of this test method is to measure the gate-controlled turn-off time of the device under the specified conditions.

2. Test circuit. The circuit used for the test is shown on figure 4225–1. The thyristor is turned on by the gate pulse delivered by the on pulse generator. On-state current is determined by the off-state supply voltage and the load resistor R_L.

After a predetermined time, a specified gate turn-off current is supplied to the gate terminal by the off pulse generator.

The storage time and fall time may be observed by means of an oscilloscope connected across the current sensing resistor.

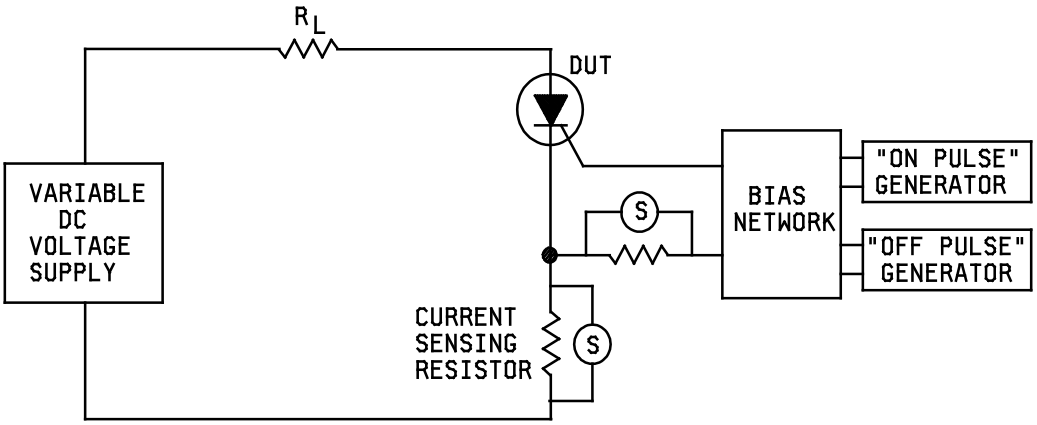


FIGURE 4225–1. Gate turn-off test circuit.

Storage time is the time interval between the 10 percent point on the leading edge of the gate current off-pulse and the 90 percent point on the trailing edge on-state current waveform. Fall time is the time interval between the 90 percent and 10 percent points on the trailing edge of the on-state current waveform. Turn-off time is the sum of storage time and fall time. Typical waveforms are shown on figure 4225–2.

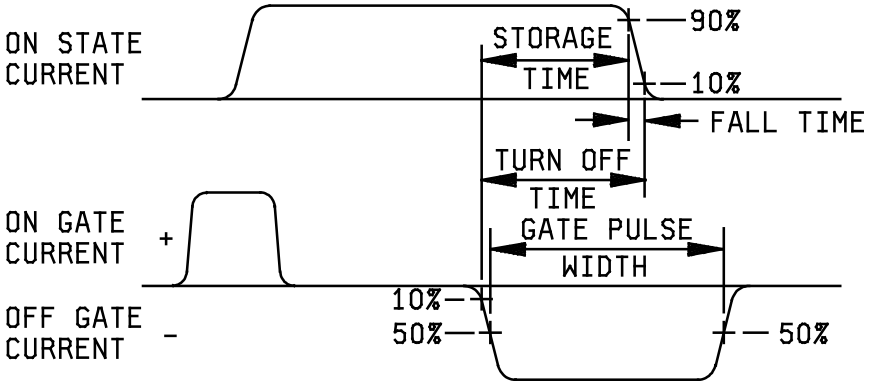


FIGURE 4225–2. Typical gate turn-off circuit waveforms.

3. Test description. A turn-off thyristor can be switched from the on-state to the off-state with a control signal of appropriate polarity to the gate terminal. The delay and fall times of anode current during the turn-off of the thyristor are affected by gate trigger pulse variations and anode circuit conditions. This method establishes a test circuit and provision for measuring of critical test conditions.

4. Procedure.

a. Gate current or gate source voltage rise time shall not exceed 10 percent of the storage time interval.

b. Duty cycle should be chosen considering heating effects of switching power losses. Sufficient anode current off time of at least 10 times the off pulse width shall be allowed to ensure that the DUT remains turned off after the turn-off pulse ends.

c. The inductance of the anode circuit should be minimized to prevent anode voltage overshoot on turn-off.

5. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Off-state voltage.

b. On-state current.

c. Switching repetition rate.

d. Duty cycle (percent on-time).

e. Operating temperature (case or ambient).

f. Bias network (show circuit).

g. Gate turn-off current (peak); or gate source voltage and gate source resistance.

h. R_L.

i. Gate on pulse width and amplitude.

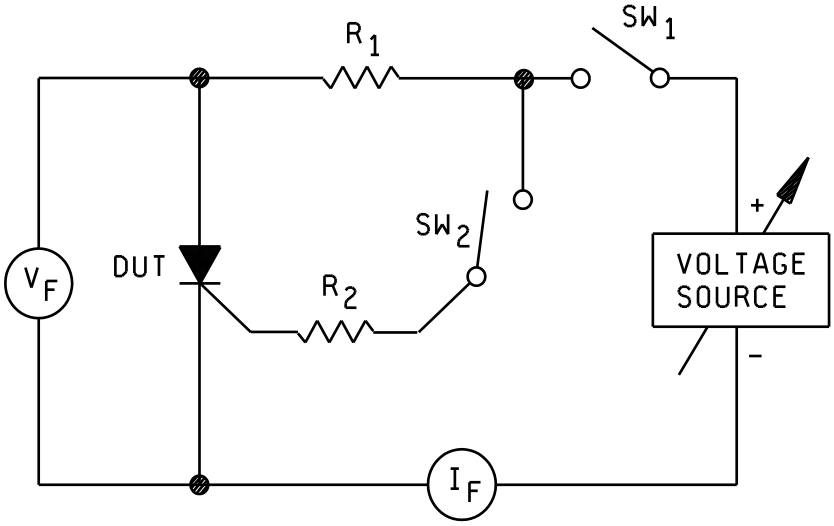
j. Gate off pulse width, amplitude, and delay time from gate on pulse.

METHOD 4226.1

FORWARD ON VOLTAGE

1. Purpose. The purpose of this test method is to measure the voltage in the forward direction across the device under the specified conditions.

2. Test circuit. See figure 4226–1.



NOTE: When specified, switch SW_1 shall be used to provide pulses of short-duty cycle to minimize device heating. When pulsing techniques are used, other suitable peak-reading techniques shall be used to measure the necessary parameters, and the duty cycle and pulse width shall be specified.

FIGURE 4226–1. Test circuit for forward on voltage.

3. Procedure. The supply voltage is adjusted to obtain the specified value of forward current through the device with SW_1 and SW_2 closed. SW_2 shall be opened, and then the forward voltage is read when the forward current equals the specified value. When the specified test current is greater than 0.20 ampere, the voltage measuring probes shall be connected to the device inside of the current carrying connections. For axial lead devices, the voltage measuring probe(s) shall contact the lead(s) at a point .375 ±.062 inch (9.52 ±1.57 mm) from the case. For all other devices, the voltage shall be measured across the normal electrical connection points.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test current (see 3).

b. Duty cycle and pulse width when pulse techniques are to be used (see above note).

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METHOD 4231.2

EXPONENTIAL RATE OF VOLTAGE RISE

1. Purpose. The purpose of this test is to determine if the device is capable of blocking a forward voltage which is increasing at an exponential rate starting from zero without switching on in the forward direction.

2. Test circuit. R_2 is chosen to discharge C between cycles when SW is opened and R_L is a protective resistor chosen to limit the maximum device current if the device turns on during the voltage rise. Switch SW should have a closure time (including bounce) of not more than 0.1 T and be closed a minimum of 5 T (see figures 4231–1 and 4231–2).

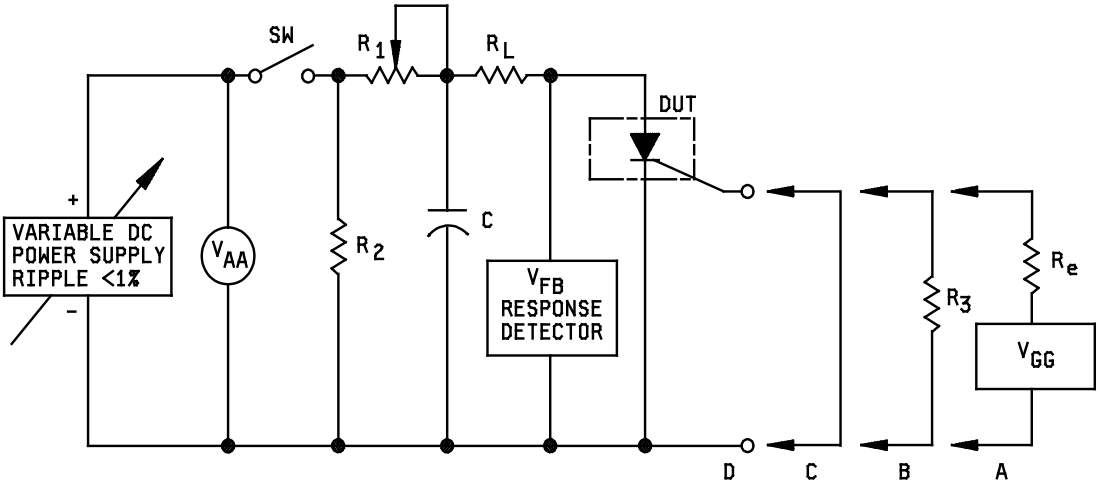

FIGURE 4231–1. Test circuit for exponential rate of voltage rise.

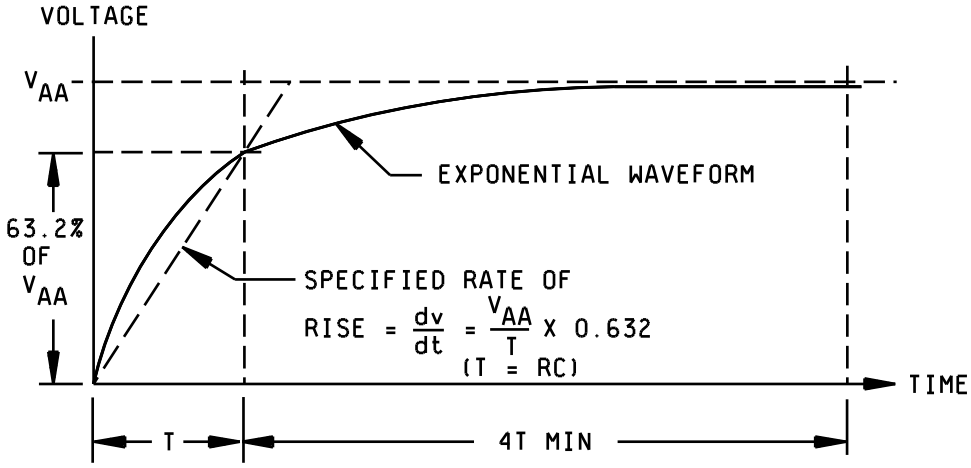

FIGURE 4231–2. Waveforms across the DUT.

3. Procedure. The voltage V_{AA} shall be adjusted to the specified value with switch SW open (see figure 4231–1). The resistor, R_1, shall be adjusted to achieve the specified rate of voltage rise, dv/dt, across the DUT with the specified gate bias condition applied. The rate of voltage rise is defined as shown on figure 4231–2. Close SW and monitor V_{FB} on the response detector. A device shall be considered a failure if V_{FB} does not rise to, and maintain, a value greater than the minimum specified forward-blocking voltage during the first 5 T of each voltage pulse after switch SW is closed.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Test voltage, V_{AA}.

b. Rate of voltage rise, dv/dt (see figure 4231-2).

c. Value of C and R_L.

d. Repetition rate.

e. Duration of test.

f. Minimum forward-blocking voltage, V_{FB}.

g. Test temperature.

h. Bias condition, gate-to-cathode, as applicable:

(1) Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

(2) Resistance return (specify value of R3).

(3) Short-circuit.

(4) Open-circuit.

METHOD 4301

JUNCTION CAPACITANCE

1. Purpose. The purpose of this test method is to determine the small signal junction capacitance of the tunnel diode under the specified conditions.

2. Test circuit. See figure 4301–1.

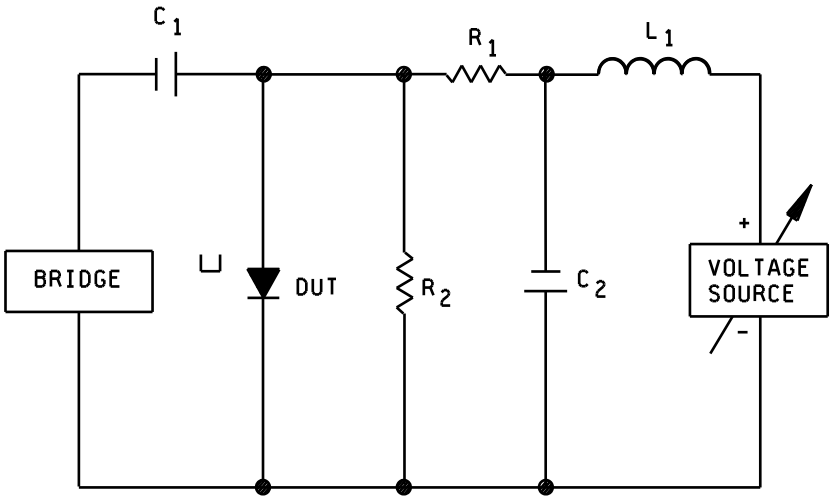

FIGURE 4301–1. Test circuit for junction capacitance.

3. Procedure. Since junction capacitance is a function of bias, it is necessary to specify the forward bias at which C_1 is to be determined. The true value of junction capacitance (at a given bias) is obtained by subtracting the capacitance of the diode package from the observed capacitance. Isolation of the dc power supply from the complex impedance bridge (see figure 4301–1) is affected by the R_1, L_1, C_2 branch of the circuit.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Values for the circuit elements R_1, C_1, C_2, L_1, and R_2.

b. Signal frequency.

c. Bias level.

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METHOD 4306.1

STATIC CHARACTERISTICS OF TUNNEL DIODES

1. Purpose. The purpose of this test method is to measure the static characteristics (V_p, V_v, I_p, I_v, V_{FP}, and R_d) of the tunnel diode under the specified conditions:

2. Test circuit. See figures 4306–1, 4306–2, and 4306–3.

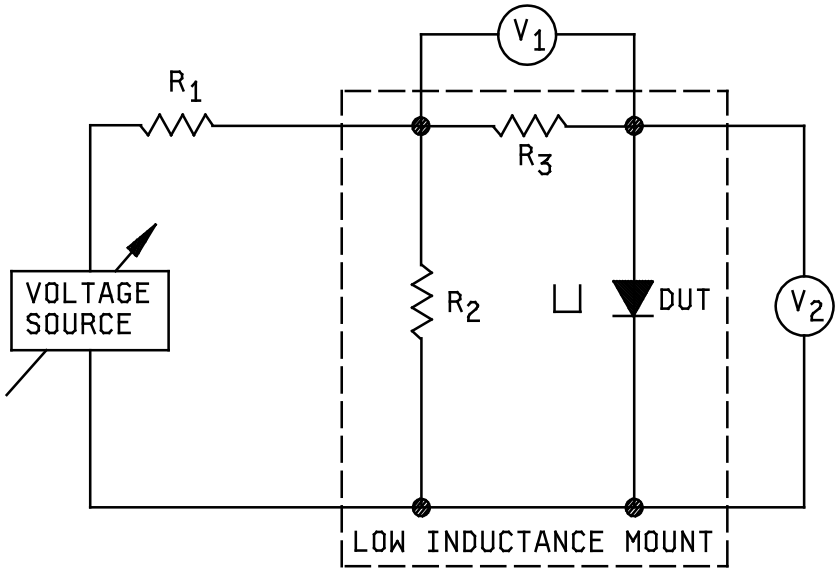

FIGURE 4306–1. Test circuit for static characteristics of tunnel diodes (dc method).

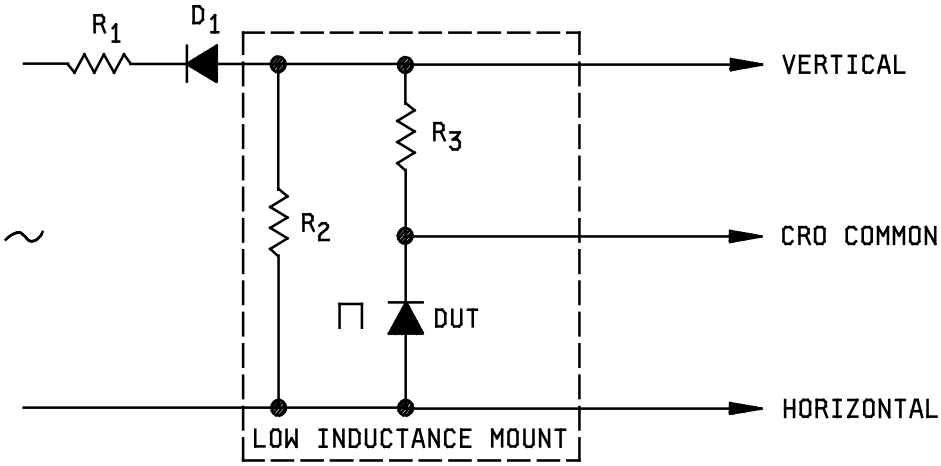

FIGURE 4306–2. Test circuit for static characteristics of tunnel diodes (ac method).

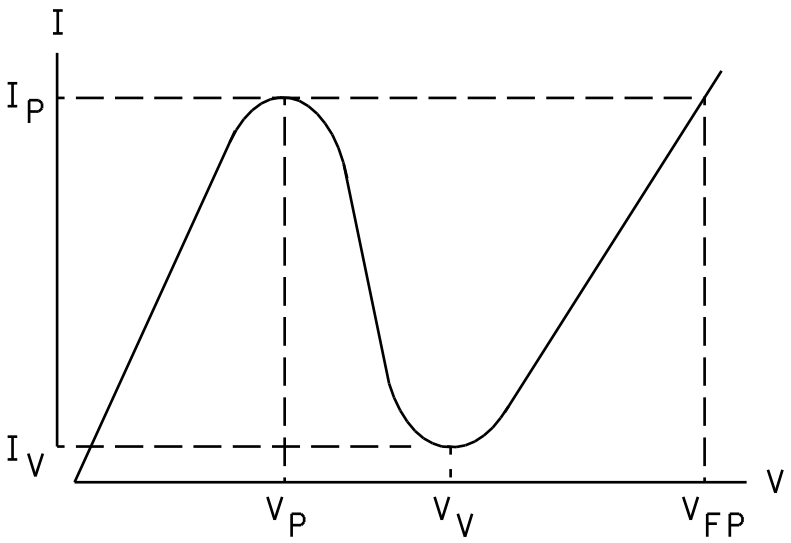

FIGURE 4306–3. Typical tunnel diode forward characteristic.

3. Procedure.

a. For the measurement of the static characteristics by point-by-point method, the circuit of figure 4306-1 shall be used. Resistor, R_2, is small to obtain low voltage and low impedance. Resistor R_3 is a current measuring resistor. Resistor R_1 is much larger than R_2. To obtain a plot in the negative resistance region R_1 shall be less than the magnitude of the incremental negative resistance of the tunnel diode.

b. For the measurement of the static forward characteristics of the device by oscillographic means, the circuit shown on figure 4306–2 shall be used. The magnitude of R_1 shall be less than the magnitude of the incremental negative resistance of the tunnel diode. Resistance R_3 is a current measuring resistor and should be chosen to give a suitable CRO deflection. Since the negative resistance is represented by the inverse slope of the I_V curve between the peak and valley voltage points, its approximate value can be estimated from the curve. For a more accurate method for the measurement of the negative resistance see test method 4321.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Resistors R_1, R_2, and R_3 (see 3.a and 3.b).

b. Signal frequency (see 3.b).

METHOD 4316

SERIES INDUCTANCE

1. Purpose. The purpose of this test is to measure the value of the small signal series inductance under the specified conditions.

2. Test circuit. See figure 4316–1.

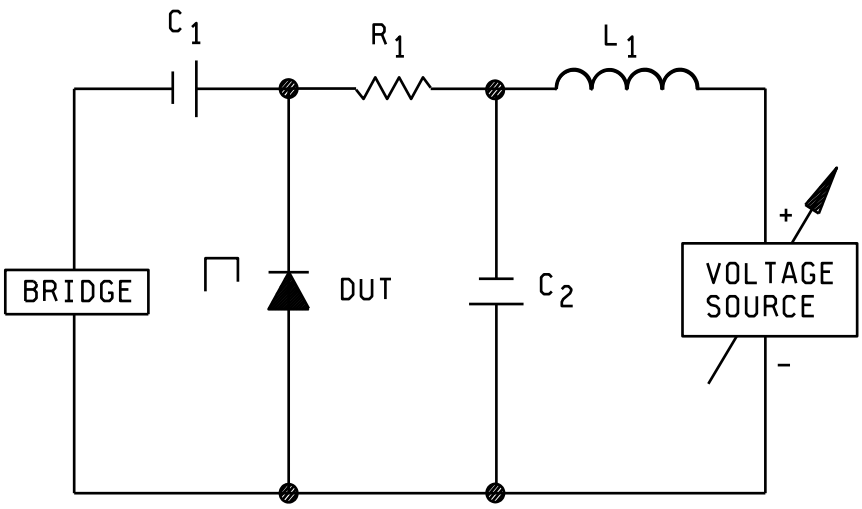

FIGURE 4316–1. Test circuit for series inductance.

3. Procedure. The device shall be reverse biased for the series inductance measurement. A sufficiently high frequency signal shall be employed to emphasize the inductive reactance, but not high enough to allow any capacitive parasitics to short-circuit the device, thus precluding the determination of L_S. A recommended frequency device is one approximately 25 percent of the self-resonant frequency of the DUT. Isolation of the dc power supply from the complex impedance is accomplished by the choke, L_1, in conjunction with C_1, R_1, C_2, branch (see figure 4316–1).

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Values for circuit elements, R_1, L_1, C_1, and C_2.

b. Signal frequency.

c. Reverse bias at which L_S is measured.

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METHOD 4321

NEGATIVE RESISTANCE

1. Purpose. The purpose of this test is to determine the magnitude of the negative resistance under the specified conditions.

2. Test circuit. See figures 4321–1 and 4321–2.

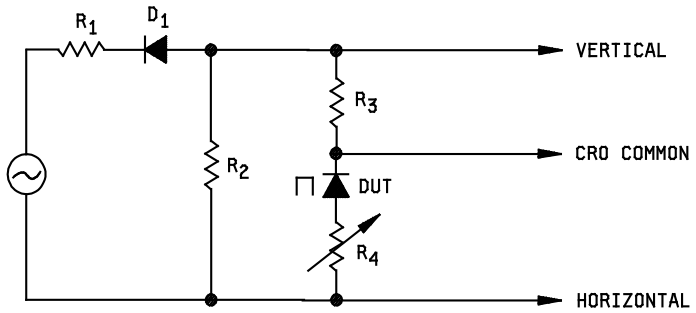

FIGURE 4321–1. Test circuit for negative resistance, short-circuit stable method.

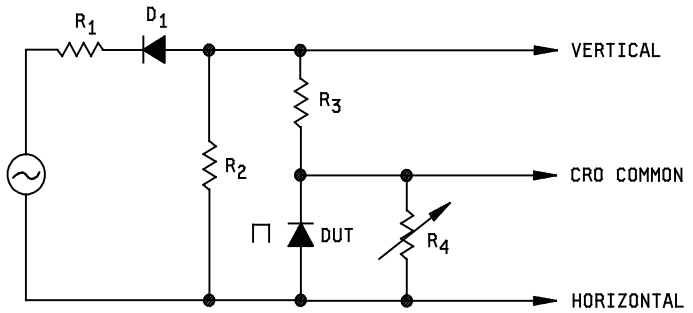

FIGURE 4321–2. Test circuit for negative resistance, open-circuit stable method.

3. Procedure. The magnitude of R_1 shall be less than the incremental negative resistance of the tunnel diode. Resistor R_3 is a current limiting resistor and should be chosen to give a suitable CRO deflection. Diode D_1 is a half wave rectifier.

3.1 Short-circuit stable method. Shunt the tunnel diode, with a variable resistor R_4 (see figure 4321–1). Vary R_4 until the slope of the negative resistance appears horizontal (zero slope) on the curve trace. The shunting resistance is now equal to the magnitude of the negative resistance, R_d. ($R_4 = R_d$.)

3.1.1 Open-circuit stable method. In series with the tunnel diode connect a variable resistor R_4 (see figure 4321–2). Vary R_4 until the slope in the negative resistance appears vertical (infinite slope) on the curve trace. The series resistance R_4 is now equal to the magnitude of the negative resistance ($R_4 = R_d$).

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Source impedance R_1.

b. Current sensing resistor, R_3.

c. Variable resistor, R_4.

METHOD 4326

SERIES RESISTANCE

1. Purpose. The purpose of this test is to determine the series resistance of the device under the specified conditions.

2. Test circuit. See figure 4326–1.

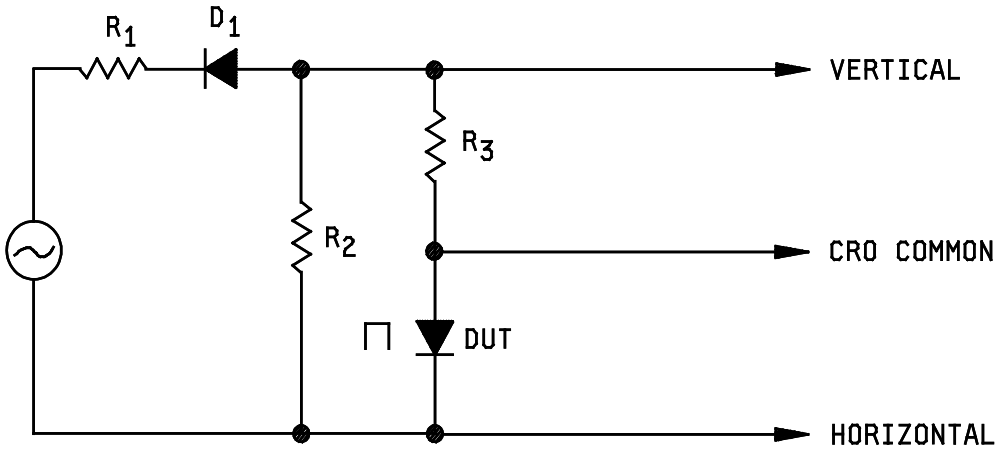

FIGURE 4326–1. Test circuit for series resistance.

3. Procedure. The measurement of the series resistance shall be accomplished for the device when biased in the reverse direction (see figure 4326–1). The linearity of the ohmic region shall be assured and the value of the power dissipation shall be such that no error is introduced as a result of excessive diode heating. The slope of the linear portion of the reverse biased tunnel diode shall be sealed within a specified accuracy in the direct determination of the series resistance of the device.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Current sensing resistor R_3.

b. Reverse bias at which R_3 is to be measured.

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METHOD 4331

SWITCHING TIME

1. Purpose. The purpose of this test method is to measure the switching time of the tunnel diode under the specified conditions.

2. Test circuit. See figure 4331–1.

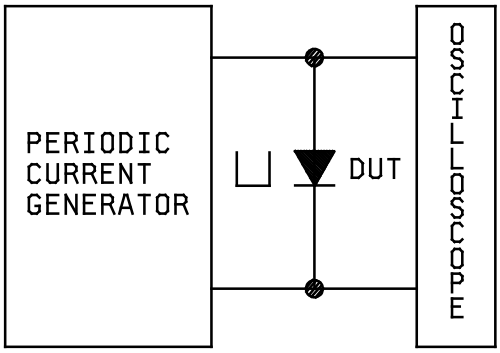

FIGURE 4331–1. Test circuit for switching time.

3. Procedure. A block diagram of the measuring circuit is shown on figure 4331–1. To perform the switching time measurement, it is necessary that the maximum generator current be greater than the diode peak current and that changes in generator current during measurement time be negligible compared to I_P. The oscilloscope input probe impedance shall be such that the current absorbed by the probe is at all times less than the peak current of the diode.

4. Summary. The following conditions shall be specified in the applicable performance specification sheet or acquisition document:

a. Generator current.

b. Repetition rate.

c. Rise time of oscilloscope.

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CONCLUDING MATERIAL

Custodians:
Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – AR, MI, SM
Navy – AS, CG, MC, SH
Air Force – 19, 99
Other – NRO

Preparing activity:
DLA – CC

Project: 5961–2014–087

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