The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 March 2017.

INCH–POUND

MIL–STD–750F
w/CHANGE 2
30 November 2016
SUPERSEDING
MIL–STD–750F
w/CHANGE 1
29 April 2013

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

TEST METHODS FOR SEMICONDUCTOR DEVICES

AMSC N/A

FSC 5961

FOREWORD

1. This test method standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This issue of MIL–STD–750 series establishes uniform test methods for testing the environmental, physical, and electrical characteristics semiconductor devices.

3. This entire test method standard has been revised. This revision has been issued in six parts; the basic test method standard (this document) and five numbered parts. This was done in order to provide flexibility in the use and the updating of the test methods. The six parts are listed as follows:

MIL–STD–750	–	Test Methods For Semiconductor Devices.
MIL–STD–750–1	–	Environmental Test Methods For Semiconductor Devices.
MIL–STD–750–2	–	Mechanical Test Methods For Semiconductor Devices.
MIL–STD–750–3	–	Electrical Characteristics Tests for Bipolar, MOSFET, and Gallium Arsenide Transistors.
MIL–STD–750–4	–	Electrical Characteristics Tests for Diodes, Microwave Diodes, Thyristors, and Tunnel Diodes.
MIL–STD–750–5	–	High Reliability Space Application Test Methods For Semiconductor Devices.

4. Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218–3990, or emailed to 750.TestMethods@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

SUMMARY OF CHANGE 2 MODIFICATIONS

1. Paragraph 3.1.2 has been added to separate symbols from acronyms used throughout the standard.

2. Paragraphs 3.1.3 through 3.1.3.5 have been added to define terms used throughout the standard.

3. Paragraph 4.2 has been modified to clarify the orientation requirements.

4. The title to 4.3.2.6 has been modified.

5. Figure 1 has been modified to add more views of the types of packages used in MIL–PRF–19500 specification sheets.

6. Figure 2 has been modified to reflect the arrow style used on figure 1.

Paragraph	Modification
3.1	Modified.
3.1.1	Modified.
3.1.2	New.
3.1.3	New.
3.1.3.1	New.
3.1.3.2	New.
3.1.3.3	New.
3.1.3.4	New.
3.1.3.5	New.
4.1.1	Modified.
4.1.5	Modified.
4.2	Modified.
4.3.2.5	Modified.
4.3.2.6	Modified.
4.4	Modified.
4.10	Modified.

Figure	Modification
Figure 1	Added subfigures 1b, 1c, 1d, 1e, and 1f.
Figure 2	Modified.

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1. SCOPE

1.1 Purpose. This standard establishes uniform methods and procedures for testing semiconductor devices suitable for use within Military and Aerospace electronic systems. The methods and procedures in the various parts of this standard cover basic environmental, physical, and electrical tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations. For the purpose of this standard, the term "devices" includes such items as transistors, diodes, voltage regulators, rectifiers, tunnel diodes, and other related parts. This standard is intended to apply only to semiconductor devices. The test methods and procedures described in the various parts of this multipart test method standard have been prepared to serve several purposes:

a. To specify suitable conditions obtainable in the laboratory that give test results equivalent to the actual service conditions existing in the field and to obtain reproducibility of the results of tests. The test methods described by this standard are not to be interpreted as an exact and conclusive representation of actual service operation in any one geographic location since it is known that the only true test for operation in a specific location is an actual service test at that point.

b. To describe, in a series of standards, all of the test methods of a similar character which now appear in the various joint-services semiconductor device specifications so that these test methods may be kept uniform and thus result in conservation of equipment, man-hours, and testing facilities. In achieving this objective, it is necessary to make each of the general test methods adaptable to a broad range of devices.

c. The test methods described by this standard for environmental, physical, and electrical testing of semiconductor devices shall also apply, when applicable, to parts not covered by an approved military sheet-form standard, specification sheet, or drawing.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system.

1.2.1 Classification of tests. The test methods are divided into five areas and are contained in five parts of this multipart test method standard. Test methods numbered 1000 to 1999 inclusive, cover environmental tests and are in MIL–STD–750–1. Test methods numbered 2000 to 2999 inclusive, cover mechanical- characteristics tests and are in MIL–STD–750–2. Electrical- characteristics tests are covered in two groups; 3000 to 3999 inclusive, cover test methods for transistors (see MIL–STD–750–3) and 4000 to 4999 inclusive, cover test methods for diodes (see MIL–STD–750–4). Test methods numbered 5000 to 5999 inclusive, are for high reliability space applications and are in MIL–STD–750–5.

1.2.2 Test method revisions. Test method revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, test method 1001.2 is the first revision of test method 1001.

1.3 Method of reference. Test methods contained in this multipart test method standard should be referenced, when applicable, in the individual specification, specification sheet, or procurement documents by specifying the test method number and the details required in the summary of the applicable method. The basic standard should be referenced and not the individual part or parts of this standard (see 5.3). To avoid the necessity for changing documents that refer to this standard, the revision number of a test method should not be used when referencing individual test methods. For example, use 1001 as a reference versus 1001.2.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this standard. This section does not include documents cited in other sections of this multipart standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, or 5 of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–19500	–	Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750–1	–	Environmental Test Methods For Semiconductor Devices.
MIL–STD–750–2	–	Mechanical Test Methods For Semiconductor Devices.
MIL–STD–750–3	–	Electrical Characteristics Test Methods for Bipolar, MOSFET, and Gallium Arsenide Transistor Semiconductor Devices.
MIL–STD–750–4	–	Electrical Characteristics Test Methods for Diodes, Microwave Diodes, Thyristors, and Tunnel Diode Semiconductor Devices.
MIL–STD–750–5	–	High Reliability Space Application Test Methods For Semiconductor Devices.
MIL–STD–1686	–	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).

DEPARTMENT OF DEFENSE HANDBOOKS

MIL–HDBK–263	–	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)(Metric).

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASME INTERNATIONAL (ASME)

ASME Y14.38	–	Abbreviations and Acronyms for Use on Drawings and Related Documents.

(Copies of these documents are available online at http://www.asme.org or from ASME International, Three Park Avenue, New York, NY 10016–5990.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540.3	–	Requirements for the Calibration of Measuring and Test Equipment.

(Copies of this document are available online at http://www.ncsli.org or can be obtained through NCSL International, 2995 Wilderness Place, Suite 107, Boulder, CO 80301–5404.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related applicable specification sheet, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Acronyms, symbols, and definitions. For the purposes of this standard, the acronyms, symbols, and definitions specified in MIL–PRF–19500, ASME Y14.38, NCSL Z540.3, and herein shall apply.

3.1.1 Acronyms used in this standard. Acronyms used in this standard are defined as follows:

a. BIST – Backward instability shock test.

b CFM – Cubic feet per minute.

c. DUT – Device under test.

d. ESD – Electrostatic discharge.

e. ESDS – Electrostatic discharge sensitivity.

f. FET – Field-effect transistor.

g. FIST – Forward instability shock test.

h. GaAs – Gallium Arsenide.

i. HTRB – High temperature reverse bias.

j. ICBO – Collector to base cutoff current.

k. IGBT – Insulated gate bipolar transistor.

l. LCC – Leadless chip carrier.

m. MOS – Metal oxide semiconductor.

n. MOSFET – Metal oxide semiconductor field-effect transistor.

o. NIST – National Institute of Standards and Technology.

p. NPN – The doping regions of a particular type of bipolar junction transistor.

q. PIND – Particle impact noise detection.

r. PNP – The doping regions of a particular type of bipolar junction transistor.

s. RH – Relative humidity.

t. SEM – Scanning electron microscope.

u. SOA – Safe operating area.

v. TSP – Temperature sensitive parameter.

w. UHF – Ultra high frequency.

x. V_{CB} – Forward voltage drop of the collector.

y. V_{EB} – Voltage drop of the emitter to base.

z. VSWR – Voltage standing wave ratio.

3.1.2 Symbols used in this standard. The symbols used in this standard are as follows:

a. Hz – Hertz.

b. µH – Microhenries.

c. ns – Nanosecond.

d. pF – Picofarad.

3.1.3 Definitions used in this standard. The definitions of terms used in this standard are as follows:

3.1.3.1 Accuracy. The quality of freedom from error. Accuracy is determined or assured by calibration, or reliance upon calibrated items.

3.1.3.2 Acquisition documents. Acquisition documents consist of the acquisition order or contract, device specification (e.g. specifications sheets, SCD's) or specifications as applicable.

3.1.3.3 Precision. The degree to which an instrument, device, assembly, test, measurement or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC). Term is used interchangeably with "repeatability".

3.1.3.4 Standard reference material (SRM). A device or artifact recognized and listed by NIST as having known stability and characterization. SRM's used in product testing provide traceability for technical specifications. SRM's do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

3.1.3.5 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

4. GENERAL REQUIREMENTS

4.1 Test conditions. Unless otherwise specified herein or in the individual specification sheet, all measurements and tests shall be made at thermal equilibrium at an ambient temperature of 25°C ±3°C and at ambient atmospheric pressure and relative humidity and the specified test condition (at environmentally elevated and reduced temperatures shall have a tolerance of ±3 percent, or +3°C, whichever is greater). Whenever these conditions must be closely controlled in order to obtain reproducible results, the referee conditions shall be as follows: Temperature 25°C ±1°C; relative humidity 50 ±5 percent; and atmospheric pressure from 650 to 800 millimeters of mercury. Unless otherwise specified in the detail test method, for mechanical test methods, (series 2000), the ambient temperature should be 25°C ±10°C.

4.1.1 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

a. Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within ±2°C or ±4 percent, whichever is greater.

   The controls for the chamber shall be such that the temperature of any single reference point within the working area shall not deviate more than ±2°C or ±4 percent, whichever is greater.

b. Space variation within working area: Chambers shall be so constructed that, at any given time, the temperature of any point within the working area shall not deviate more than ±3°C or ±3 percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.

c. Chambers with specified minimum temperatures (such as those used in burn-in, HTRB, and life tests): When test requirements involve a specified minimum test temperature, the controls and chamber construction shall be such that the temperature of any point within the working area shall not deviate more than +8°C, –0°C; or +8 percent, –0 percent, whichever is greater, from the specified minimum temperature, except for the immediate vicinity of the specimens generating heat.

4.1.2 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be 1,000 ±25 Hertz (Hz).

4.1.3 Sinusoidal pulse testing. For tests (e.g. test method 1040, condition A) which require a 60 Hz half wave sinusoidal input; a 50 Hz signal is acceptable for testing performed in European and Asian countries.

4.1.4 Accuracy. The specified limits are for absolute (true) values, obtained with the specified (nominal) test conditions. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the measured values, so that the true values of the device parameters (as they would be under nominal test conditions) are within the specified limits.

The following electrical test tolerances and precautions, unless otherwise specified in the applicable acquisition document, shall be maintained for all device measurements to which they apply (test methods series 3000, 4000 and other specified electrical measurements). Wherever test conditions are specified in the applicable acquisition document to a precision tighter than the tolerances indicated below, the specified conditions shall apply and take precedence over these general requirements.

a. Bias conditions shall be held to a tolerance of ±3 percent of the specified value, except for breakdown testing (see 4.1.4.c).

b. Such properties as input pulse characteristics, repetition rates, and frequencies shall be held to a tolerance of ±10 percent. Nominal values shall be chosen so that ±10 percent variation (or the actual test equipment variation, if less than 10 percent) does not affect the accuracy or validity of the measurement of the specified value.

c. Voltages and currents applied in breakdown testing shall be held to a tolerance of ±1 percent of the specified value(s).

d. Resistive loads shall be ±5 percent tolerance.

e. Capacitive loads shall be ±10 percent or ±1 picofarad (pF) tolerance, whichever is greater.

f. Inductive loads shall be ±10 percent or ±5 microhenries (µH) tolerance, whichever is greater.

g. Static parameters shall be measured to a tolerance of ±1 percent.

h. Switching parameters shall be measured to a tolerance of ±5 percent or ±1 nanosecond (ns), whichever is greater.

4.1.4.1 Control based on uncertainty. Test processes that have complex characteristics are best performed and controlled by the application of uncertainty analysis. The overall uncertainty in a test, or measurement process, shall be determined and impact of said uncertainty on the product parameter tolerance shall be taken into account. The methods used for determining uncertainty shall be defined and documented. The method selected shall use any, or all, combination of the following forms:

a. Arithmetic addition (linear): Normally produces an overly conservative estimate and reflects a highly improbable situation in which contributing errors are at their maximum limit at the same time and same direction.

b. Root sum square (RSS): Normally applied where errors tend to fit a normal distribution (Gaussian) and are from independent sources.

c. Partial derivatives: Used where complex relationships exist.

d. Monte Carlo simulation: Used in very complex situation where other methods are not easily applied or do not fit.

e. Standard reference material (or controlled correlation device) testing providing observable data.

NOTE: Observable data from a controlled device may be relied upon to provide feedback that confirms process performance is within statistical limits.

f. Analysis of systematic and random errors, applying corrections as applicable.

g. Any other recognized method of combining errors into an expression of uncertainty substantiated by an engineering analysis.

4.1.4.2 Test methods and circuits. Unless otherwise stated in the specific test method, the methods and circuits shown are given as the basic measurement method. The methods and circuits shown are not necessarily the only method or circuit which can be used, but the manufacturer shall demonstrate to the acquiring activity that alternate methods or circuits which they may desire to use are equivalent and give results within the desired accuracy of measurement (see 4.1.4).

4.1.5 Calibration requirements. Calibration and certification procedures shall be provided in accordance with NCSL Z540.3 for plant standards and instruments used to measure or control production processes and semiconductor devices under test. Calibrated items shall be controlled, stored, and used in a manner suitable to protect calibration integrity. Test equipment requiring calibration (single items or assemblies) shall be identified and labeled in accordance with NCSL Z540.3 or equivalent. For those measurements that are not traceable to the NIST, correlation samples shall be maintained and used as the basis of proving acceptability when such proof is required. In addition, the following requirements shall apply:

a. The accuracy of a calibrating instrument shall be at least four times greater than that of the item being calibrated, unless the item being calibrated is state of the art equipment, which may be near or equal in accuracy to the state of the art calibrating equipment, in which case the four times requirement does not apply. However, the instrument shall be calibrated to correlate with standards established by the NIST.

b. Except in those cases where the NIST recommends a longer period, and concurrence is obtained from the qualifying activity, calibration intervals for plant electrical standards shall not exceed one year and plant mechanical standards shall not exceed two years.

4.2 Identification of orientations, direction of forces applied and major plane for cross sectioning. For those test methods which involve observation (such as radiography) or the application of external forces which must be related to the orientation of the device, such orientation and direction of forces applied shall be identified in accordance with figures 1 and 2. For case or package configurations other than those shown on figures 1 and 2, the orientation of the device shall be as specified in the individual specification sheet or acquisition document. When the package is not shown on figures 1 and 2 and no orientation information is detailed in the individual specification sheet or acquisition document, the following shall apply:

a. X is the orientation of a device with the main axis of the device normal to the direction of the accelerating force, and the major cross section parallel to the direction of the accelerating force.

b. Y is the orientation of a device with the main axis of the device parallel to the direction of the accelerating force, and the principal base toward (Y_1), or away from (Y_2), the point of application of the accelerating force.

c. Z is the orientation of a device with the main axis and the major cross section of the device normal to the direction of the accelerating force. Z is 90 degrees of X.

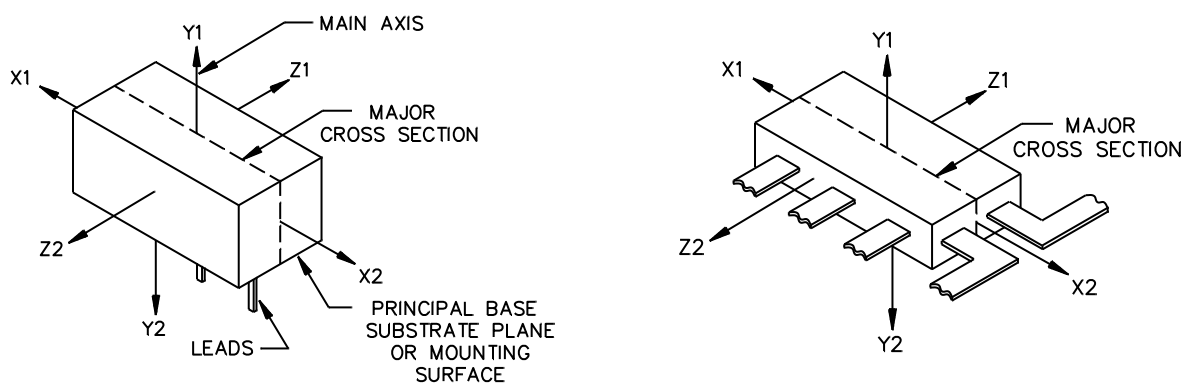

FIGURE 1a. Bottom lead type packages.

FIGURE 1b. Radial lead flat packages.

FIGURE 1. Orientation of non-cylindrical semiconductor devices.

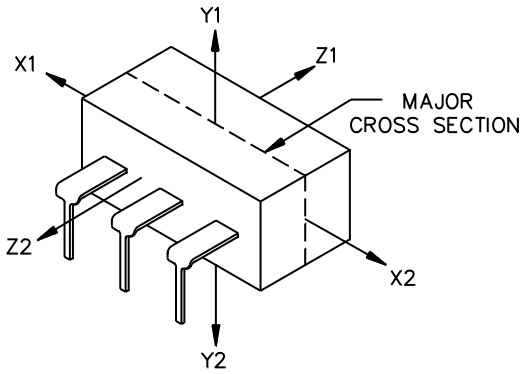

FIGURE 1c. Dual-in-line packages.

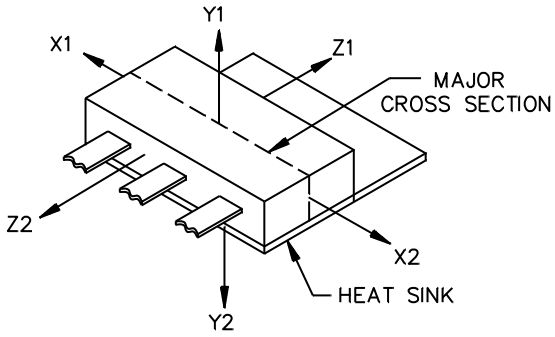

FIGURE 1d. Flange mount packages with radial leads from one side only and heatsink.

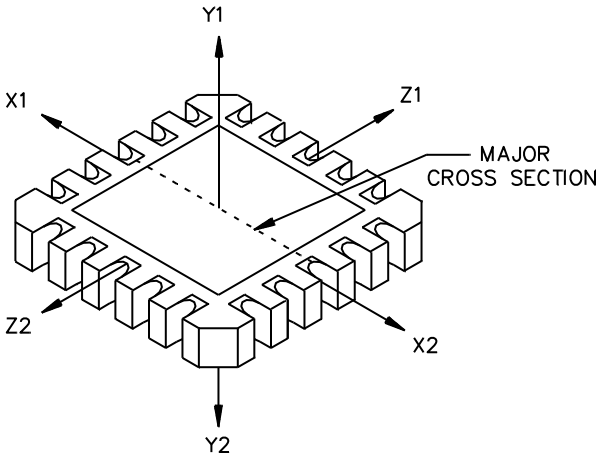

FIGURE 1e. Leadless chip carrier (top view).

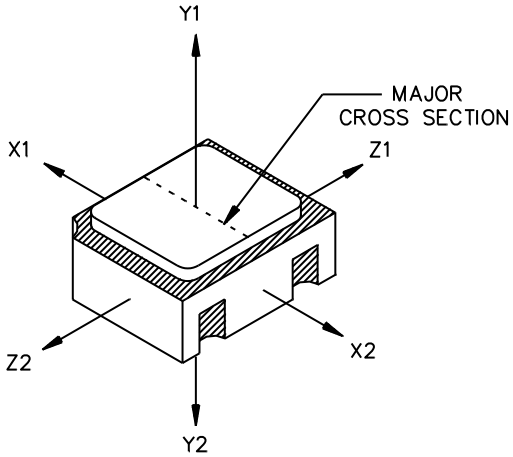

FIGURE 1f. Small leadless chip carrier (top view).

FIGURE 1. Orientation of non-cylindrical semiconductor devices – Continued.

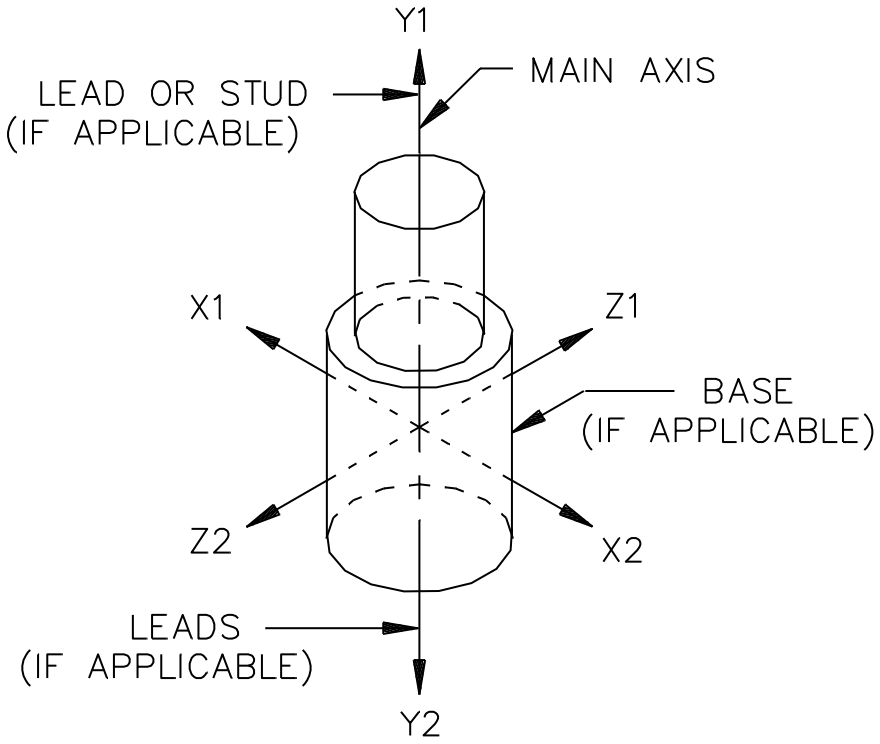

FIGURE 2. Orientation of cylindrical semiconductor device.

4.3 General precautions. The following precautions shall be observed in testing the devices.

4.3.1 Transients. Devices shall not be subjected to conditions in which transients cause the rating to be exceeded.

4.3.2 Test conditions for electrical measurements. Unless otherwise required for a specified test method, semiconductor devices should not be subjected to any condition that will cause any maximum rating of the device to be exceeded. The precautions should include limits on maximum instantaneous currents and applied voltages. High series resistances (constant current supplies) and low capacitances are usually required. If low cutoff or reverse current devices are to be measured; for example, nanoampere units, care should be taken to ensure that parasitic circuit currents, or external leakage currents are small compared with the cutoff or reverse current of the device to be measured.

4.3.2.1 Thermal resistance measurements (test method series 3100). For thermal resistance measurements, at least three temperature sensitive parameters (TSP) of the transistor can be used; the collector to base cutoff current, I_{CBO}; the forward voltage drop of the emitter to base diode, V_{EB}; and the forward voltage drop of the collector to base diode, V_{CB}. The methods described in this test method standard refer to the thermal resistance between specified reference points of the device. For this type of measurement, power is applied to the device at two values of case, ambient, or other reference point temperature, such that identical values of I_{CBO}, V_{EB}, or V_{CB} are read during the cooling portion of the measurement.

4.3.2.2 Low frequency tests (test method series 3200). Unless otherwise specified, the measurements shall be made at the electrical test frequency, 1,000 ±25 Hz. At 1,000 Hz, the reactive components may not be negligible.

4.3.2.3 High frequency tests (test method series 3300). Care shall be taken that, in designing the circuit and transistor mounting, adequate shielding and decoupling are provided and that series inductances in circuits are negligible.

4.3.2.4 Electrical characteristics tests for MOS field effect transistors (test method series 3400). Circuits are shown for n-channel field-effect transistors in one circuit configuration only. They may readily be adapted for p-channel devices and for other circuit configurations.

4.3.2.5 Steady-state dc measurements (test method series 4000). Unless otherwise specified, all steady-state dc parameters are defined using steady-state dc conditions. Automatic test equipment pulse conditions may be used for steady-state dc measurements only when correlation to between the pulsed and steady-state dc measurements has been established.

4.3.2.6 Pulse measurements (test method series 3000 and 4000). When device static or dynamic parameters are measured under pulsed conditions, in order to avoid measurement errors introduced by device heating during the measurement period, the following items should be covered in the performance specification sheet:

a. The statement "pulsed test" shall be placed by the test specified.

b. Unless otherwise specified, the pulse time (t_p) shall be ≤ 10 milliseconds and the duty cycle shall be a maximum of 2 percent; within this limit the pulse shall be long enough to be compatible with test equipment capability and the accuracy required, and short enough to avoid heating.

4.3.2.7 Electrical characteristics tests for microwave diodes (test method series 4100). When device static or dynamic parameters are measured under pulsed conditions, in order to avoid measurement errors introduced by device heating during the measurement period, the following items should be covered in the performance specification sheet:

a. Measurement of conversion loss, output noise ratio, and other microwave parameters shall be conducted with the device fitted in the holder. All fixed adjustments of the holder shall be made at a laboratory designated by the Government. In the test equipment, the impedance presented to the mixer by the local oscillator (and the signal generator, if used) shall be the characteristic impedance of the transmission line between the local oscillator and mixer (the maximum VSWR, looking toward the local oscillator, shall be 1.05 at the signal and image frequencies).

b. For qualification inspection of reversible UHF and microwave devices, the radio frequency measurements, excluding the post environmental test end points and high temperature life (non-operating) end points, shall be made, first, with the adapter on one end of the device, and then repeated with the adapter at the opposite end of the device; for the environmental and life tests, fifty percent of each sample shall be tested with the adapter on one end of the device and the remaining half of the sample shall be tested with the adapter on the opposite end of the device. End point measurements shall be made without moving the adapter. This procedure shall be repeated on at least one lot every 6 months.

c. For quality conformance inspection of reversible UHF and microwave devices, the electrical measurements, including the post environmental test end points, may be made with the adapter on either end of the device.

4.3.3 Test circuits. The circuits shown are given as examples which may be used for the measurements. They are not necessarily the only circuits which can be used; however the manufacturer shall demonstrate to the Government that other circuits which they may desire to use will give results within the desired accuracy of measurement. Circuits are shown for PNP transistors in one circuit configuration only. They may readily be adapted for NPN devices and for other circuit configurations.

4.3.3.1 Test method variation. Variation from the specified test methods used to verify the electrical parameters are allowed provided that it is demonstrated to the preparing activity, or their agent, that such variations in no way relax the requirements of this standard and that they are approved before testing is performed. For proposed test variations, a test method comparative error analysis shall be made available for checking by the preparing activity or their agent.

4.3.4 Soldering. Adequate precautions shall be taken to avoid damage to the device during soldering required for tests.

4.3.5 Order of connection of leads. Care should be taken when connecting a semiconductor device to a power source. The common terminal shall be connected first.

4.3.6 Radiation precautions. Due precautions shall be used in storing or testing semiconductor devices in substantial fields of X–rays, neutrons, or other energy particles.

4.3.7 Handling precautions.

4.3.7.1 UHF and microwave devices. Handling precautions for UHF and microwave devices shall be as follows:

a. Ground all equipment.

b. Make hand contact to the equipment while holding the base end and maintain hand contact with the equipment until the device is in place.

c. Where applicable, keep devices in metal shields until they are inserted in the equipment or until necessary to remove for test.

4.3.7.2 Electrostatic discharge sensitive devices. Handling precautions should be observed in accordance with MIL–HDBK–263 during testing of Electrostatic Discharge Sensitive (ESDS) devices. The area where ESDS device tests are performed shall meet the requirements of an ESD Protected Area of MIL–STD–1686.

4.4 Continuity verification of burn-in, HTRB, and life tests. The test set-up shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following shall be the minimum acceptable monitoring procedure:

a. Device sockets. Initially, and at least each 6 months thereafter, each test board or tray shall be checked to verify continuity to connector points to assure that the correct voltage bias will be applied. Except for this initial and periodic verification, each device, or device socket, does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the device under test (DUT).

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the system, and brought up to the specified operating conditions, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to ensure electrical continuity and the correct application of specified electrical stresses, or bias, for each connection or contact pair for the DUT used in the applicable test configuration. If the system (chamber) is opened for performing these tests, the system may be opened for a maximum of 10 minutes. Where possible, the test node points shall be accessible external to the oven chamber (HTRB) to avoid opening the door since that immediately reduces operating temperature. This can also influence leakage currents and bias to DUT with resistors in series for power supply protection.

c. At the conclusion of the test period, prior to removal of devices from temperature and bias conditions, the voltage and signal condition verification of 4.4.b shall be repeated.

d. For class S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified bias conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s) or by performing a socket verification on each socket prior to loading. An approved alternate procedure may be used.

4.4.1 Bias interruption. Where failures, or open contacts, occur which result in removal of the required bias stresses for any period of the required bias duration, the bias time shall be extended to ensure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias while the chamber is at temperature during the final 8 hours of burn-in shall require extension of the bias duration for an uninterrupted 8 hours (minimum) since the last interruption. Incidental, or momentary power interruptions less than or equal to 10 seconds can be ignored.

4.5 Requirements for high temperature reverse bias (HTRB) and burn-in.

a. The temperature of +20°C minimum is the ambient air temperature to which all devices should be exposed during power screening where room ambient is specified.

b. An increase in effective ambient temperature from cumulative induced power to DUT shall not result in device junction temperature exceeding maximum ratings.

c. For HTRB, the coolest ambient temperature shall be below the required minimum when measured in the various locations of convection currents (below or above) or upstream or downstream (fan air) of DUT.

d. Moving air greater than 30 CFM (natural convection) may be allowed for the purpose of temperature equalization within high device density burn-in racks.

e. Power up of burn-in racks may occur when ambient is less than specified. When thermal equilibrium has been reached, or 5 hours (maximum) has passed, the ambient shall be at the specified value. Time accrued prior to reaching the specified ambient shall not be counted for life test duration.

f. If the ambient, at or beyond the 5 hour point is not the specified value, a nonconformance exists and requires corrective action.

g. Time is not chargeable during the period when specified conditions are not maintained. If device maximum ratings are exceeded and the manufacturer intends to submit the lot affected, the product on test shall be evaluated by re-starting the burn-in or HTRB from zero hours at the specified temperature and verifying that the end-point failure rate is typical for this product type from a review of established records.

h. Chamber temperature for HTRB and burn-in shall be controlled to ±3 percent of the specified value (unless otherwise specified 4.1.1). This temperature shall be maintained within the chamber. Forced air may be used to equalize temperature within the chamber but shall not be used as a coolant to increase device power capability.

4.6 Bias requirements.

a. Bias errors at the power supply source caused by changing power supply loads during temperature transitions shall not exceed ±5 percent of that specified value.

b. Bias values at the source, during stabilized conditions, shall not exceed ±3 percent of the specified value.

c. Burn-in apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. Bias and burn-in circuitry tolerances should not vary test conditions to individual devices by more than ±5 percent of specified conditions.

d. Normal variation in individual device characteristics need not be compensated for by burn-in circuitry.

e. Burn-in equipment shall be arranged so that the existence of failed or abnormal devices in a group does not negate the effect of the test for other devices in the group. Periodic verification will assure that specified conditions are being maintained. Verification shall be performed, as a minimum, at the start and at the end of screening.

f. Lead, stud, or case mounted devices shall be mounted in their normal mounting configuration and the point of mechanical connection shall be maintained at no less than the specified ambient.

4.7 Destructive tests. Unless otherwise demonstrated, the following test methods are classified as destructive:

Test method number	Test
1017	Neutron irradiation
1019	Steady-state total dose irradiation
1020	ESDS classification
1021	Moisture resistance
1036, 1037	Intermittent operation life
1041	Salt atmosphere
1042 (condition D)	Burn-in/life test for power MOSFETs
1046	Salt spray
1056	Thermal shock (glass strain)
2017	Die shear test
2031	Soldering heat
2036	Terminal strength
2037	Post-seal bond strength
2075	Decap internal visual design verification
2077	SEM

All other mechanical or environmental tests (other than those listed in 4.8) shall be considered destructive initially, but may subsequently be considered non-destructive upon accumulation of sufficient data to indicate that the test is non-destructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without significant evidence of cumulative degradation in any device in the sample, is considered sufficient evidence that the test is non-destructive for the device of that manufacturer. Any test specified as a 100-percent screen shall be considered non-destructive for the stress level and duration or number of cycles applied as a screen.

4.8 Non–destructive tests. Unless otherwise demonstrated, the following test methods are classified as nondestructive:

Test method number	Test
1001	Barometric pressure
1022	Resistance to solvents
1026, 1027	Steady-state life
1031, 1032	High temperature life (non-operating)
1038, 1039, 1040	Burn-in screen
1042 (conditions A, B, and C)	Burn-in/life test for power MOSFETs
1051 (100 cycles or less)	Thermal shock (temperature cycling)
1071	Hermetic seal tests
2006	Constant acceleration
2016	Shock
2026	Solderability (if the original lead finish is unchanged and if the maximum allowable number of reworks is not exceeded.)
2052	PIND test
2056	Vibration, variable frequency
2066	Physical dimensions
2069, 2070, 2072, 2073, 2074	Internal visual (pre-cap)
2071	External visual
2076	Radiographic inspection
2081	FIST
2082	BIST
3101	Thermal impedance testing of diodes
3103	Thermal impedance measurements for IGBTs
3104	Thermal impedance measurements for GaAs
3051, 3052, 3053 (with limited supply voltage)	SOA (condition A for test method 3053)
3131	Thermal resistance (emitter to base forward voltage, emitter-only switching method)
4066	Surge current
4081	Thermal resistance of lead mounted diode (forward voltage, switching method)

NOTE: When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions, or approved accelerated screening, when it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and, in the case where it is allowed adequate sample testing, shall be performed to provide the proper reliability safeguards.

4.9 Laboratory suitability. Prior to processing any semiconductor devices intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written laboratory suitability status for each test method to be employed. Processing of any devices by any facility without laboratory suitability status for the test methods used shall render the processed devices nonconforming.

4.10 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life-cycle costs.

5. DETAILED REQUIREMENTS

5.1 Organization. This standard is comprised of six different parts, each of which is a separate publication with a unique identification number. This type of organization provides flexibility in referencing, and revising the test methods of the different parts of this standard. The complete standard consists of the basic standard and the five numbered parts.

5.2 Arrangement and contents. Each numbered part of this standard contains a series of test methods. Test methods covering similar tests are grouped together for ease of useability and referencing as follows:

a. Part 1 is identified as MIL–STD–750–1. This part contains all of the environmental test methods. These test methods are numbered 1005 through 1082.

b. Part 2 is identified as MIL–STD–750–2. This part contains all of the mechanical test methods. These test methods are numbered 2005 through 2103.

c. Part 3 is identified as MIL–STD–750–3. This part contains electrical characteristics test methods for bipolar, MOSFET, and Gallium Arsenide transistors. These test methods are numbered 3001 through 3575.

d. Part 4 is identified as MIL–STD–750–4. This part contains the electrical characteristics test methods for diodes, microwave diodes, thyristors, and tunnel diodes. These test methods are numbered 4000 through 4331.

e. Part 5 is identified as MIL–STD–750–5. This part contains the high reliability space application test methods. These test methods are numbered 5001 through 5010.

5.3 References to MIL–STD–750. All the requirements of this standard, its five associated parts, and the individual test methods in those parts are interchangeable with those standards identified as MIL–STD–750. Therefore, existing specifications, specification sheets or OEM documents referencing MIL–STD–750 do not need to be revised, updated, or changed to make reference to any of the different parts of this revision of MIL–STD–750.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing.

Accuracy
Bias requirements
Destructive tests
Electrical characteristics tests for microwave diodes
Electrical characteristics tests for MOS field effect transistors
High frequency tests
Laboratory suitability
Low frequency tests
Non–destructive tests

6.4 Changes from previous issue. The margins of this standard are marked with vertical bars to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – AR, MI, SM
Navy – AS, CG, MC, SH
Air Force – 19, 99
Other – NRO

Preparing activity:
DLA – CC

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.