The documentation and process conversion measures necessary to comply with this revision shall be completed by: 29 February 2016.

INCH–POUND

MIL–PRF–50884F
W/AMENDMENT 1
27 November 2015
SUPERSEDING
MIL–P–50884F
15 March 2014
(See 6.6)

PERFORMANCE SPECIFICATION

PRINTED WIRING BOARD, FLEXIBLE OR RIGID–FLEX, GENERAL SPECIFICATION FOR

Inactive for new design after 28 February 1999.
For new design use MIL–PRF–31032.

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43216–3990 or sent by electronic mailed to 5998.Documents@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the performance and qualification requirements for flexible and rigid-flex printed wiring boards with or without plated through holes (see 6.1). Verification is accomplished through the use of one of two methods of product assurance (appendix A or appendix B). Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use are specified in the applicable master drawing.

1.2 Classification. Printed wiring boards are classified by 1.2.1, 1.2.2, 1.2.3 and 1.2.6.

1.2.1 Printed wiring board type. The printed wiring boards covered by this specification are of the following types:

Type 1 – Singled–sided flexible printed wiring board (see 6.4.3.1) with or without shields or stiffeners.

Type 2 – Double–sided flexible printed wiring board (see 6.4.3.2) with or without shields or stiffeners with or without plated-through holes.

Type 3 – Multilayer flexible printed wiring board with plated holes (see 6.4.3.3) and with or without shields or stiffeners.

Type 4 – Multilayer rigid and flexible printed wiring board with plated-through holes (see 6.4.3.4).

Type 5 – Bonded rigid and/or flexible printed wiring board combinations without plated-through holes (see 6.4.3.5).

1.2.2 Installation use. The printed wiring boards covered by this specification are for the following installation uses:

Use A – Capable of withstanding flexing during installation (flex to install).

Use B – Capable of withstanding continuous flexing for the number of cycles specified (see 3.1.1).

1.2.3 Rework capability (see 6.6.1). The printed wiring boards covered by this specification are of the following rework capability grades:

Grade R – Flexible printed wiring that is capable of withstanding at least three solder and two unsolder operations without terminal area degradation.

Grade U – Flexible printed wiring that is capable of withstanding at least one solder operation without terminal area degradation. This grade can only be used in electrical or electronic assemblies that will not require an unsolder and re–solder capability.

If not specified on the applicable master drawing, the default rework capability is grade R.

1.2.4 Flexible base material. The printed wiring board flexible base material type should be identified by the base material designators of the applicable flexible base material specification as required by the master drawing (see 3.1.1).

1.2.5 Rigid base material (designs with stiffeners). The printed wiring board rigid base material type should be identified by the base material designators of the applicable base material specification as required by the master drawing (see 3.1.1).

1.2.6 Wrap plating (surface and knee continuous copper plating). The wrap plating grade designation is defined by the amount of plated-through hole surface and knee continuous copper plating thickness remaining after surface processing. The grades are as follows:

A – Printed boards of this grade have 80 percent or more of the specified wrap plating thickness after surface processing.

B – Printed boards of this grade have 50 percent or more of the specified wrap plating thickness after surface processing.

C – Printed boards of this grade have 20 percent or more of the specified wrap plating thickness after surface processing.

Unless otherwise specified, the default grade of wrap copper plating is grade A for printed board designs that will not undergo planarization and grade B for designs that require planarization.

1.3 Description of this specification. The main body contains general provisions and is supplemented by detailed appendices. Appendices A and B describe the two product assurance programs that can be implemented by the manufacturer. Appendix A contains the legacy QPL product assurance program. Appendix B is an optional quality management approach using a technical review board concept addressed in MIL–PRF–31032, to modify the performance and verification criteria provided in this specification. Appendix C provides statistical sampling, and basic test and inspection procedures. Appendix D can be used when producing printed wiring boards designed to superseded design standards (see 6.4.1 and D.4.2). Appendix D may also be used as a guide in developing a test plan for legacy or existing designs based on the tests and inspections of appendix A. Appendix E contains the qualification requirements. Appendices F and G contain illustrations of the acceptable and unacceptable conditions that are either externally or internally observable on printed wiring boards. Appendix H contains the requirements for quality control test circuitry and is mandatory for manufacturers qualified to the QPL product assurance level of this specification.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50 – Terms and Definitions for Interconnecting and Packaging Electronic Circuits. (DoD adopted).

(Copies of these documents are available online at http://www.ipc.org.)

(Non–Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General requirements. The manufacturer of printed wiring boards, in compliance with this specification, shall use, or have access to production and verification facilities, and product assurance procedures adequate to assure successful compliance with the provisions of this specification and the associated master drawing. Adequacy of a printed wiring board manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity (DLA Land and Maritime, code VQE). Only printed wiring boards which are verified and meet all the applicable performance requirements herein and the design, construction, and material requirements of the associated master drawing shall be certified as compliant and delivered.

3.1.1 Master drawing. Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing.

3.1.2 Conflicting requirements. In the event of conflict between the requirements of this specification and other requirements of the applicable master drawing, the precedence in which documents shall govern, in descending order, is as follows:

a. The applicable master drawing (see 3.1.1). Additional acquisition requirements (see 6.2) may be provided in the order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the qualifying activity, will result in the printed wiring board being deemed noncompliant with this specification.

b. This specification.

c. The applicable design standard (see 3.1.1, A.3.3 as applicable).

d. Specifications, standards, and other documents referenced in section 2.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC–T–50 and those contained herein (see 6.4, and appendices A, B, C, D, E, F, G, and H).

3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable Qualified Products List (QPL) at the time of award of contract (see A.4.5, B.4.1, E.3.1, and 6.3). The qualification requirements shall be in accordance with appendix E. Products qualified in accordance with appendix E are monitored and maintained through the manufacturer's Capability Verification Inspection program and do not require requalification to this specification.

3.3 Product assurance requirements. This document contains two different methods of product assurance for printed wiring board compliance. The two levels of printed wiring product assurance are QPL (see 3.3.1) and QML (see 3.3.2) as defined herein.

3.3.1 QPL product assurance. A product assurance program for QPL printed wiring boards furnished under this specification shall satisfy the requirements of appendix A. QPL product assurance system procedures shall be revised to address changes from the previous revision of this specification and made available to the qualifying activity no later than 6 months after the date of this specification in order for the manufacturer to be retained on Qualified Products Database 50884 (QPD–50884). The manufacturer shall ensure the product assurance procedures reflect the actual product assurance practices of the manufacturing location qualified. The qualifying activity shall be notified concurrently of any changes to these procedures.

3.3.2 QML product assurance. A product assurance program for QML printed wiring boards furnished under this specification shall satisfy the requirements of appendix B. QML product assurance procedures shall be revised to address changes from the previous revision of this specification and made available to the qualifying activity no later than 6 months after the date of this specification in order for the QML–31032 manufacturer to be retained on QPD–50884. The manufacturer shall ensure the product assurance procedures reflect the actual product assurance practices of the manufacturing location qualified. The qualifying activity shall be notified concurrently of any changes to these procedures.

3.4 Letters of interpretation and policy. Letters of interpretation and policy applicable to this document shall be approved in writing by the preparing activity. All letters of interpretation and policy applicable to MIL–PRF–50884 or MIL–P–50884written prior to the current date of this document are not applicable to this revision. All subsequent letters of interpretation and policy letters are valid only until the next document change action (amendment or revision).

3.5 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.6 Certification of conformance and acquisition traceability. Unless otherwise specified by the contract or order (see 6.2), a certificate of conformance for compliant printed wiring boards shall be forwarded to the acquiring activity (see 6.4.1). When a certificate of conformance for compliant printed wiring boards is supplied, it shall include the following information, as a minimum:

a. Manufacturer's name and address.

b. Customer's name and address.

c. Manufacturer's CAGE (Commercial and Government Entity) code (see 6.4.5).

d. Printed wiring board description, including classification (printed wiring board type, installation use, rework capability, and base materials), specification number with revision letter and amendment number when applicable, the applicable product assurance level (either QPL or QML), master drawing or other identification number, and the applicable design standard.

e. Lot date code.

f. Quantity of printed wiring boards in shipment from manufacturer.

g. Statement certifying printed wiring board conformance to this specification, the master drawing, and the contract or order.

h. The date of transaction.

i. A description or listing of the additional acquisition requirements (see A.6.2.2) not listed on the master drawing (see 3.1.1) that affects the design, test conditions, or acceptability requirements of the resulting printed boards.

j. The name of the company official approving the certificate of conformance. The manufacturer shall have a method for authenticating the approval of certificates of conformance for printed wiring boards compliant to this specification.

3.7 Qualifying activity on–site audit. Manufacturers listed on QPD–50884 will be required to undergo periodic on–site audits of their facilities by the qualifying activity. The manufacturer shall demonstrate to the qualifying activity that controls have been implemented to assure compliance to the requirements of this specification. The qualifying activity reserves the right to perform on–site audits of any other facilities, such as contracted services, that the manufacturer uses for producing printed wiring boards to this specification. The on-site audit shall verify that the manufacturer has an effective self-audit program for both itself and for all contract service operations used in the production of certified product.

3.8 Change effectivity. Unless otherwise specified by the preparing activity or the qualifying activity, all changes from the previous revision of MIL–P–50884 shall become effective within 180 days after the date of publication of this revision. If a qualified manufacturer is unable to implement the changes within the 180 day time period, additional time shall be requested from the qualifying activity. Manufacturers that are QPL listed and have concerns regarding possible changes to retention reporting requirements should contact the qualifying activity for clarification.

3.9 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see A.4.5 and appendix E, or B.4.1).

b. Inspection of product for delivery (see A.4.6 or B.4.3.a).

c. Periodic conformance inspection (see A.4.7 or B.4.3.b).

4.2 Printed wiring board performance verification.

4.2.1 QPL. The minimum requirements for printed wiring board performance verification to the QPL product assurance level shall consist of inspections on the production printed wiring boards and the quality conformance test circuitry or test coupons referenced in appendix A.

4.2.2 QML. The minimum requirements for printed wiring board performance verification to the QML product assurance level shall satisfy the guidelines of appendix B.

4.3 Qualification inspection. The minimum requirements for qualification shall be as specified in appendix E. Manufacturers qualified through appendix E may accept and certify orders to the QPL product assurance level of appendix A.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in–house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Flexible and rigid–flex printed wiring boards are intended primarily for use in ground support, airborne, and shipboard electronic equipment and electrical equipment to eliminate high density hand wiring, where space is limited and where compact packaging is desirable.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. The specific issue of individual documents referenced (see 2.2).

c. Packaging requirements (see 5.1).

d. Appropriate printed wiring board type (see 1.2.1), installation use (see 1.2.2), rework capability grade (see 1.2.3), and grade of copper wrap (see 1.2.6).

e. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see 3.1.1).

f. The specific issue of individual documents referenced (see 2 and A.2).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in QPD–50884 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, Ohio 43218–3990, or by e-mail to 5998.Qualifications@dla.mil, or at http://www.landandmaritime.dla.mil/programs/qmlqpl. An online listing of products qualified to this specification may be found in the Qualified Products Database at https://assist.dla.mil. Application procedures should conform to the guidelines of SD–6, "Provisions Governing Qualification" (see 6.3.3).

6.3.1 Transference of qualification. Manufacturers currently qualified to MIL–P–50884E with amendment 3 will have their qualification transferred to this document under the conditions described in 3.3.1 and 3.3.2. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements specification revision and amendment as listed on the approved Authorization to Test Form, DLA Land and Maritime Form 19W, available from the qualifying activity. New applications for qualification (after the date of this document) should be performed to the requirements of this revision.

6.3.2 Retention of qualification. Printed wiring boards verified and certified to MIL–P–50884C (with any amendment) or MIL–P–50884D (with any amendment) to any product assurance level contained herein may be used to meet retention of qualification production to this document (see A.4.5.1).

6.3.3 Legacy manufacturer certification program. The certification program of MIL–P–50884C (unamended) was not governed by the policies and procedures of the Defense Standardization Program as defined by DoD 4120.3–M and therefore does not exist within the QPL program of MIL–P–50884C with Amendment 1 and beyond. For additional information concerning this issue, see MIL–P–50884C, paragraph 60.1.

6.3.4 "Provisions Governing Qualification". Copies of SD–6, "Provisions Governing Qualification", may be downloaded at URL: http://assistdocs.com/search.

6.4 Terms and definitions.

6.4.1 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or sub-contractor to be its agent. When this organizational element of the Government has given specific written authorization to a contractor or sub-contractor to serve as agent, the agent will not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization, which is the preparing activity or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity will be an organization within the supplier's company that is independent of the group responsible for device design, process development, or screening, or may be an independent organization outside the supplier's company.

6.4.2 Design standard. A document that establishes the baseline parameters (default values), standard practices and guidelines for the design of printed wiring boards. Within this document, the term "design standard" is used to describe those documents that contains the design, construction, material, and test coupon requirements and guidelines used to produce panels of flexible printed wiring boards.

6.4.3 Printed wiring board type. The printed wiring board type should be as specified in IPC–2223. The legacy printed wiring board types of MIL–STD–2118 correspond to the types described in IPC–2223 and are listed herein.

6.4.3.1 Type 1. Type 1 flexible printed wiring boards have only one conductive layer (single sided conductor pattern) with coverlayer and no plating in the component holes. In addition, the design may contain shields or stiffeners. Type 1 flexible printed wiring boards are usually designed for installation use B (continuous flex) applications.

6.4.3.2 Type 2. Type 2 flexible printed wiring boards are printed wiring boards with conductor patterns on both sides of the printed wiring board (double sided). In addition, the design of the printed wiring board may require the following: (1) that the holes through the base material be plated through to connect the conductor patterns on both sides together, (2) with or without shields, and (3) with or without stiffeners. Type 2 flexible printed wiring boards are usually designed for installation use B (continuous flex) applications.

6.4.3.3 Type 3. Type 3 flexible printed wiring boards are multilayered (with three or more conductor layers) with plated-through holes. Type 3 printed wiring boards are usually designed for installation use A (flex to install) applications.

6.4.3.4 Type 4. Type 4 flex–rigid printed wiring boards are multilayered boards containing plated-through holes with rigid sections connected by flexible sections. Type 4 printed wiring boards are usually designed to be used in installation use A (flex to install) applications.

6.4.3.5 Type 5. Type 5 printed wiring boards are multilayer bonded rigid and flexible printed wiring board combinations without plated-through holes. Type 5 printed wiring boards are usually designed to be used in installation use A (flex to install) applications.

6.4.4 Product assurance. The method of complying with the two different levels of this document using either the QPL method or the QML method.

6.4.4.1 QPL. A transitional program that allows a manufacturer that is certified and qualified to the QML program of MIL–PRF–31032 to fabricate, test, and supply products to appendix A of this revision of this document.

6.4.4.2 QML. A list of manufacturers, by name and plant address, who have met the certification and qualification requirements stated in MIL–PRF–31032. A QML focuses on qualifying an envelope of materials and processes rather than individual products or designs. That envelope is qualified by carefully selecting representative worst case test vehicles or representative samples from production that contain all potential combinations of materials and processes that may be subsequently used during production. A QML is normally appropriate for items of supply that have very rapid technological advancement or a myriad of variations or custom designs that make individual product qualifications impractical or excessively expensive.

6.4.5 Commercial and Government Entity (CAGE) code. The Commercial and Government Entity Code, or CAGE Code, is a 5 digit identifier assigned to suppliers to the Federal Government of the United States of America in order to provide a standardized method of identifying a given facility or a specific location. Request for or an update to a CAGE code can be obtained at URL: http://www.dla.mil/CAGECodeRequestOrUpdate/CageCodeHome.aspx. CAGE was previously known as Federal Supply Code for Manufacturers (FSCM) and also the National Supply Code for Manufacturers (NSCM).

6.4.6 System for Award Management (SAM). The Central Contractor Registration (CCR) system was transitioned to the System for Award Management (SAM) in 2012. The SAM is the primary registrant database for the U.S. Federal Government. SAM collects, validates, stores and disseminates data in support of agency acquisition missions. Qualified manufacturers should be registered in the SAM prior to the award of a contract; basic agreement, basic ordering agreement or blanket purchase agreement. SAM information can be obtained at https://www.sam.gov.

6.4.7 Qualified Products Database (QPD). A QPD is an electronic version of a Qualified Products List (QPL) and Qualified Manufacturers List (QML) document. The QPD has replaced all of the information that used to contained on QPL–50884. As the data in a specific QPL or QML is converted to database format, the QPL or QML will be phased out and replaced by an equivalent Qualification Dataset (QDS) associated with the specification requiring qualification. For MIL–PRF–50884, a Qualified Products Database Supplemental Information Sheet containing the information once listed on QPD–50884 is available from the qualifying activity.

6.4.8 Qualified Products Database Supplemental Information Sheet (QPDSIS). The qualified capabilities for manufacturers may be found in the QPDSIS for any particular MIL–PRF–50884 listing. The QPDSIS is available at http://www.landandmaritime.dla.mil/programs/qmlqpl.

6.5 Compliant printed wiring boards. For a printed wiring board to be compliant with this document, it has to be produced by a manufacturer qualified for listing on QPD–50884 or reciprocal listing as described in appendix B, and come from a lot which was subjected to and passed all inspection of product for delivery verifications using the applicable product assurance program.

6.6 Supersession.

6.6.1 Superseded types and classes. Superseded types and classes are listed below:

a. Type A of MIL–P–50884B (the ability to withstand only one solder operation without degradation) was not addressed in previous revisions, but is addressed by rework capability grade U in this revision.

b. Type B of MIL–P–50884B (the ability to withstand five solder and unsoldering operation without degradation) was superseded by all printed wiring board types of MIL–P–50884C and MIL–P–50884D. It is addressed by rework capability grade R in this revision.

c. Class 1 of MIL–P–50884B was superseded by types 1, 2, and 5 of MIL–P–50884C and beyond.

d. Class 2 of MIL–P–50884B was superseded by types 3 and 4 of MIL–P–50884C and beyond.

6.6.2 Design, construction, and verification. Design, construction, and verification supersession information is included in appendix D of this document.

6.6.3 Reference to superseded specifications. All the requirements of this document can be interchangeable with those documents identified as MIL–P–50884. Therefore, existing documents (master drawings or OEM documents) referencing MIL–P–50884 need not be revised, updated, or changed to make reference to MIL–PRF–50884 in order for this document to be used.

6.7 Design standard. This document contains requirements and guidelines for the testing of printed wiring boards that were designed to and or make use of test coupons conforming to IPC–2221 and the flex and rigid-flex design details unique to IPC–2223. See appendix D for additional guidance regarding the verification of panels using different design standards.

6.8 Environmentally preferable material. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements of this specification. As of the dating of this document, the U.S. Environmental Protection Agency (EPA) is focusing efforts on reducing 31 priority chemicals. The list of chemicals and additional information is available on their website http://www.epa.gov/osw/hazard/wastemin/priority.htm. Included in the list of 31 priority chemicals are cadmium, lead, and mercury. Use of these materials should be minimized or eliminated unless needed to meet the requirements specified herein (see section 3).

6.9 Automatic update notification. An electronic mail notification option is available to registered ASSIST users. If you do not receive an electronic mail message that an amendment or revision of this document has been completed, information pertaining to how to make use of this option within ASSIST may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, Ohio 43218–3990, or by email to 5998.Qualifications@dla.mil, or at website http://www.landandmaritime.dla.mil/Offices/Sourcing_and_Qualification/resource.aspx.

6.10 Subject term (key word) listing.

Design standard
Master drawing
Qualified Manufacturer List (QML)
Qualified Product List (QPL)
Test coupon
Product assurance program

6.11 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

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PRODUCT ASSURANCE (PERFORMANCE AND VERIFICATION) REQUIREMENTS FOR QUALIFIED PRODUCTS LIST LEVEL

A.1 SCOPE

A.1.1 Scope. This appendix contains the requirements and procedures for manufacturers using the traditional Qualified Products List (QPL) method of product assurance (performance and verification inspection) for printed wiring boards covered by this specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3 and A.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections A.3 and A.4 of this specification, whether or not they are listed.

A.2.2 Government documents. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of this document are available online at http://quicksearch.dla.mil.)

A.2.3 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM B567 – Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568 – Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.

(Copies of these documents are available online at http://www.astm.org.)

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–2221 – Generic Standard on Printed Board Design.
IPC–2223 – Sectional Design Standard for Flexible Printed Boards.
IPC–A–600 – Acceptability of Printed Boards.
IPC–OI–645 – Standard for Visual Optical Inspection Aids.
IPC–TM–650 – Test Methods Manual.
IPC–7095 – Design and Assembly Process Implementation for BGAs.
IPC–9252 – Requirements for Electrical Testing of Unpopulated Printed Boards.
J–STD–003 – Solderability Tests for Printed Boards.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

A.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 General. The performance requirements contained in this section, although sometimes determined by examination of sampled printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.1.1 Master drawing (see A.6.2.1.d). Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing. For the purposes of this appendix, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable master drawing. If individual design details are not specified on the applicable master drawing, then the baseline design parameters shall be as detailed in the design standard that was used to design the printed wiring board (see A.3.3).

A.3.2 Qualification. Printed wiring boards furnished under this appendix shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see A.4.5 and A.6.3).

A.3.3 Design (see A.6.2.1.e). Printed wiring boards shall be of the design as specified. Unless otherwise specified (see A.3.1.1), if individual design details are not specified on the applicable master drawing, then the baseline design parameters to be used for acceptability of finished product requirements shall be as detailed in the design standard that was used to design the printed wiring board. If no design standard is specified on the master drawing or the appropriate design standard cannot be determined, then the default design shall be performance class 3 of IPC–2221 and IPC–2223.

A.3.3.1 Test coupons. Test coupon design shall be in accordance with the applicable design standard specified (see A.3.1.1) and herein. Test coupon placement and quantity on a production panel shall be in accordance with the requirements of appendix H. Test coupon selection and usage shall be determined by the manufacturer in order to meet the in-process, groups A, B, and C inspection requirements herein. NOTE: Test coupon design shall be as specified in the applicable design standard or herein, and shall reflect worst case design conditions of the printed wiring board(s) they represent.

A.3.4 Materials. The printed wiring boards shall be constructed of materials as specified (see A.3.1.1). When a definite material is not specified on the applicable master drawing, a material shall be used that will enable the printed wiring board to meet the performance requirements of this specification. Acceptance or approval of any material shall not be construed as a guaranty of the acceptance of the finished printed wiring board.

A.3.4.1 Pure tin. Unless otherwise specified (see A.3.1.1), the use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of printed wiring board finishes and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of three percent lead, by mass (see A.6.8).

A.3.4.2 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.5 External visual and dimensional requirements. When examined in accordance with A.4.8.1, the finished printed wiring board shall meet the dimensional requirements specified in A.3.5.1 through A.3.5.8. Unless otherwise specified (see A.3.1.1), design related dimensional requirements specified in A.3.3, such as cutouts, overall thickness, periphery, and other features specified, shall be examined in accordance with A.4.8.1. Scratches, dents, and tool marks shall not bridge or expose signal conductors, expose base metal, expose or disrupt reinforcement fibers, reduce dielectric properties, and reduce spacing below the minimum requirements herein. Appendix F contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions of printed wiring board test specimens.

A.3.5.1 Base material (flexible and rigid).

A.3.5.1.1 Edges of base materials. Base material edges include the external edge of the printed board, the edges of cutouts, and the edges of non–plated–through holes. Loose metallic burrs shall not be acceptable. The minimum edge spacing (the spacing between the edge of the printed wiring board base material and conductors) shall be as specified.

A.3.5.1.1.1 Edges of flexible sections. Defects such as burrs, nicks, tears, or delamination, along the trimmed edges of flexible sections of printed wiring boards shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1). Discoloration or resin recession along the trimmed edges of the flexible sections following the solderability or resistance to soldering heat test is acceptable providing the discoloration or resin recession dimension does not exceed the thickness of the adhesive material in the bonding area (when applicable) or reduce the edge spacing below the requirements of the master drawing.

A.3.5.1.1.2 Edges of rigid sections (types 4 and 5). Defects such as burrs, crazing, and nicks, along the edges of printed wiring boards, including edges of cutouts and edges of non-plated-though holes, shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1) or .10 inch (2.5 mm), whichever is smaller. If no requirement for edge spacing is specified (see A.3.1.1), these types of penetrations shall not exceed .10 inch (2.5 mm). For haloing, the distance between the penetration and the nearest conductive feature shall not be less than the minimum lateral conductor spacing, or .004 inch (0.1 mm) if not specified. Inspection panels that are scored or partially routed with breakaway tabs for printed wiring board or test coupon removal shall meet the de-panelization requirements specified (see A.3.1.1).

A.3.5.1.1.3 Edges between flexible and rigid sections (see figure F–1). The edge of the rigid portion of a flexible to rigid junction shall define the transition between flexible and rigid portions of a printed wiring board. Unless otherwise specified (see A.3.1.1), the inspection range for a flexible to rigid junction shall be limited to .060 inch (1.52 mm) on either side of the transition. Imperfections along the flexible to rigid transition such as adhesive squeeze out, localized deformation of dielectric and conductors, protruding dielectric materials, crazing, or haloing not extending past the inspection range shall be acceptable.

A.3.5.1.2 Surface imperfections. Imperfections in the surface of the base material such as blistering, burrs, cuts, dents, foreign materials, gouges, nicks, pits, resin scorched areas, resin starved areas, scratches, tool marks, variations in color such as white spots or black spots, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

a. The imperfection does not bridge between conductors (weave texture may bridge conductors).

b. The dielectric spacing between the imperfection and conductors does not reduce conductor spacing below the specified minimum requirements (see A.3.1.1).

A.3.5.1.2.1 Exposed or disrupted fibers. Exposed or disrupted reinforcement fibers on the horizontal surface of the printed board shall not bridge conductors and shall not reduce the conductor spacing below the minimum conductor spacing requirements. Unless otherwise specified, weave texture (reinforcement texture) or weave exposure (exposed reinforcement material fibers) by mechanical fabrication operations shall be acceptable provided they meet the exposed or disrupted reinforcement fiber requirements.

A.3.5.1.2.2 Surface pits and voids. Surface pits and voids in the base material shall be acceptable providing the following conditions are met:

a. Surface pits or voids are no bigger than .031 inch (0.8 mm) in the longest dimension.

b. The surface pits or voids do not bridge conductors.

c. The total area of all surface pits or voids does not exceed five percent of the total printed board area.

d. The surface pit or void does not affect the performance of the base material.

A.3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

a. The imperfection is translucent.

b. The imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.

c. The imperfection does not reduce conductor spacing between adjacent conductors below the minimum requirements specified (see A.3.1.1).

d. The imperfection does not propagate as a result of testing (such as rework simulation, resistance to soldering heat, or thermal shock).

e. Color variations or mottled appearance in bond enhancement treatments shall be acceptable. Random areas of missing bond enhancement treatment shall not exceed 10 percent of the total conductor surface area of the affected layer.

A.3.5.1.3.1 Foreign inclusions. Foreign inclusions shall be acceptable provided they comply with the following:

a. The inclusion is trapped within the flexible portion of the printed wiring board.

b. The inclusion does not reduce the spacing between conductors below the minimum conductor spacing specified (see A.3.1.1). If not specified, the inclusion shall not reduce the conductor spacing by more than 20 percent.

c. The inclusions longest dimension is no greater than .032 inch (0.81 mm) in circuitry areas. Inclusions in non-circuitry areas have no maximum dimension requirement.

d. When the base material specification allows for more or larger inclusions, those inclusions are allowed in the finished printed wiring board, up to the size and quantity defined by the base material specification provided that the inclusion does not violate the conductor spacing requirements of A.3.5.1.3.c.

A.3.5.1.3.2 Foreign inclusions between printed board surface and stiffener (types 1, 2, and 3 only). Translucent foreign inclusions located between the printed board surface and stiffener shall be acceptable provided they comply with the following:

a. Any bulge caused by the inclusion is no larger than .004 inch (0.1 mm).

b. Any inclusions shall not be larger than 5 percent of the bonding area of the stiffener.

c. There shall be no contact of the inclusion with a component hole or the printed board periphery. Any thread-like inclusion shall not protrude more than .04 inch (1.0 mm) from the printed board periphery

d. There shall be no inclusions that reduce the spacing between adjacent access openings below the minimum spacing specified in A.3.5.2.4.

A.3.5.1.3.3 Subsurface spots. Subsurface spots shall be acceptable provided they meet any of the following:

a. The spots are translucent.

b. The spots are known to be weave texture other than delamination or disbonding.

c. The spots are isolated white spots that do not propagate as a result of any soldering operation (gelation particles are acceptable regardless of location).

A.3.5.1.3.4 Adhesive voids (for metal clad flexible base materials only). Adhesive voids that are no greater than .020 inch (0.51 mm) or 25 percent of spacing shall be acceptable.

A.3.5.1.3.5 Measling and crazing. Measling and crazing shall not exceed the class 3 acceptable requirements specified in IPC–A–600, for bare printed wiring boards.

A.3.5.1.3.6 Exposed or disrupted reinforcement fibers. Exposed or disrupted reinforcement fibers shall be acceptable provided they do not bridge conductors and do not reduce the conductor spacing below the specified minimum.

A.3.5.2 Conductor pattern.

A.3.5.2.1 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of any conductor pattern or land from the base material. The completed printed board shall not exhibit any lifted land. (NOTE: See A.3.6.2.5 for allowances for the acceptable lifting of lands, i.e. lifted lands, following rework simulation, resistance to soldering heat, and thermal shock testing.)

A.3.5.2.2 Conductor finish. The conductor finish shall be as specified. Unless otherwise specified, the following requirements shall apply.

A.3.5.2.2.1 Coverage. The conductor finish plating or coating shall cover the basis metal of the conductive pattern. Coverage of a conductor by solder does not apply to the vertical conductor edges. There shall be no evidence of any lifting or separation of conductor finish plating or coating from the surface of the conductive pattern.

A.3.5.2.2.1.1 Dewetting. For tin alloys, reflowed tin–lead, or solder coated surfaces, a maximum of five percent of dewetting is permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes not used for solder connections shall meet the requirements of J–STD–003.

A.3.5.2.2.1.2 Nonwetting. For tin alloys, reflowed tin–lead, or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

A.3.5.2.2.2 Conductor finish plating and coating voids in plated-through holes. The conductor finish plating and coating shall not have voids in plated-through holes that exceed the following limits:

a. No more than one final finish void in any plated-through hole.

b. Not more than 5 percent of the plated-through holes shall have conductor finish voids.

c. Any conductor finish void present is not more than 5 percent of the plated-through holes length.

d. Any conductor finish void present is less than 90 degrees of the circumference of the plated-through hole.

A.3.5.2.2.3 Edge board contacts. Unless otherwise specified, these requirements apply to the critical contact area. The critical contact area for edge board contacts shall be as specified.

a. Defects or surface imperfections in the edge board contact finish shall not expose base metal in critical contact area.

b. There shall be no nodules or metal bumps in the edge board contact finish in the critical contact area.

c. Pits, dents, or depressions in the edge board contact finish shall not exceed .0059 inch (0.15 mm) in their longest dimension. There shall be no more than three occurrences for each edge board contact, and no more than 30 percent of the contacts shall be affected.

A.3.5.2.2.4 Plating junctions (typical of edge board contacts). There shall be no exposed copper in the junction of metallic platings or coatings. An overlap of metallic platings or coatings shall be acceptable if less than .032 inch (0.8 mm) in length. When both solder coating and gold plating are present at a plating junction, a discolored or gray-black area at that plating overlap zone shall be acceptable.

A.3.5.2.2.5 Solder mask. For designs using solder mask over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder mask and the basis metal conductor finish.

A.3.5.2.2.6 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductive pattern.

A.3.5.2.3 Conductor pattern imperfections (see figures F–2 and F–3). The conductor pattern shall contain no cracks, splits or tears. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce non-critical conductors width by more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent width reductions greater than .50 inch (12.70 mm) or 10 percent of a signal conductor length, whichever is less.

A.3.5.2.3.1 Cuts and scratches. A cut or scratch of any length or width is permissible on ground or voltage planes, provided the dielectric is not exposed. Cuts and scratches on non-critical conductors may be of any length, but no deeper than 20 percent of the total conductor thickness.

A.3.5.2.3.2 Dents. A dent of any length or width on ground planes shall be acceptable provided the clad surface is not torn. Dents on conductive patterns may be of any length, but no deeper than .0005 inch (0.013 mm).

A.3.5.2.3.3 Pinholes. Pinholes in ground or voltage planes in non-critical areas shall be acceptable provided they have no single diameter greater than .040 inch (1.0 mm) and do not exceed four for each 1.0 inch (25.4 mm) diameter. Pinholes in a conductive pattern shall be acceptable, provided they do not reduce the width of a conductive pattern by 10 percent and do not exceed one for each 1.0 inch (25.4 mm) of a conductor length.

A.3.5.2.3.4 Pits. Pits in ground or voltage planes shall be acceptable provided they do not exceed 25 percent of the surface area. Any pit in the conductive pattern is acceptable provided the outline dimension does not exceed 10 percent of the conductor width, and there is no more than one pit for each 1.0 inch (25.4 mm) of the conductor length.

A.3.5.2.3.5 Superfluous metal. Unless otherwise specified, small particles of metal, such as residual copper or subsequent plating after etching, which remain affixed to areas that are intended to be free of conductive material shall be acceptable providing the following conditions are met:

a. The superfluous metal is no closer than .25 inch (6.4 mm) to any conductor.

b. The superfluous metal is smaller than .005 inch (0.13 mm) at their greatest diameter.

A.3.5.2.4 Conductor spacing and width.

A.3.5.2.4.1 Conductor spacing. The conductor spacing shall be as specified (see A.3.1.1). The minimum edge spacing (the spacing between the edge of the printed wiring board and conductors) shall be as specified. Unless otherwise specified, if no conductor spacing tolerance is specified, a reduction in the conductor spacing of 10 percent above the specified spacing, due to isolated defects or misregistration, shall be considered acceptable.

A.3.5.2.4.2 Conductor width. The conductor width(s) shall be as specified (see A.3.1.1). Allowable reduction in the conductor width, due to isolated defects or misregistration, shall be in accordance with A.3.5.2.3.

A.3.5.2.5 Lands for component mounting. The lands to be used for component mounting shall be as specified. Imperfections on component hole lands, surface mount lands, or wire bond pads shall be acceptable provided they do not exceed the defect allowance requirements specified herein.

A.3.5.2.5.1 Component hole lands (external annular ring (see figures F–4 and F–5). The minimum external annular ring shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum external annular ring shall not be less than the value specified in the IPC's 2220 series of documents for the design of flexible or rigid-flex printed wiring boards. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the minimum external annular ring specified, due to defects such as access hole (coverlayer or stiffener) misregistration, dents, pinholes, pits, nicks, and extruded adhesive onto the land. No more than 20 percent of the annular ring circumference (72 degrees) may be affected. Unless otherwise specified, plated-through holes identified as vias can have a maximum of 90 degrees of hole breakout if the breakout does not occur at the conductor to land intersection.

A.3.5.2.5.2 Rectangular surface mount lands (see figure F–6). Rectangular surface mount lands shall not contain defects such as nicks, dents, and pin holes along the external edge of the land that exceed 20 percent of either the length or width of the land and shall not encroach the pristine area, which is defined by the central 80 percent of the land width by 80 percent of the land length as shown on figure F–6. Defects internal to the land shall not exceed 10 percent of the length or width of the land and shall remain outside of the pristine area of the surface mount land. Electrical test probe 'witness'' marks shall be acceptable when within the pristine area.

A.3.5.2.5.3 Round surface mount lands and Ball Grid Array pads (see figure F–7). Round surface mount lands and Ball Grid Array (BGA) pads shall not contain defects such as nick, dents and pin holes along the edge of the land that radially extend towards the center of the land by more than 10 percent of the diameter of the land. In addition, defects shall not extend more than 20 percent of the circumference of the land as shown on figure F–7. There shall be no defects within the pristine area which is defined by the central 80 percent of the land diameter. Electrical test probe 'witness' marks shall be acceptable when within the pristine area.

A.3.5.2.5.4 Wire bond pads. The maximum conductor finish roughness (surface roughness) for pads or areas designated for wire bonding shall be no greater than 32 micro inches (0.8 micrometers). Unless otherwise specified, the wire bond pad bonding area shall be defined as the pristine area as shown on figure F–6 for rectangular pads or figure F–7 for round pads. There shall be no pits, nodules, scratches, electrical test probe 'witness' marks, or other defects in the pristine area that exceed the surface roughness limits.

A.3.5.2.6 Holes for interlayer connections. The external annular ring of holes used for interlayer connections shall be as specified. Unless otherwise specified, the external annular ring may have in isolated areas a 20 percent reduction of the specified minimum external annular ring due to defects such as dents, pinholes, pits, or nicks.

A.3.5.2.7 Registration, external (method I).

A.3.5.2.7.1 Component hole lands Misregistration of component hole lands shall not reduce the minimum external annular ring below the limits specified (see A.3.1.1).

A.3.5.2.7.2 Rectangular surface mount lands. The registration of rectangular surface mount lands shall be as specified (see A.3.1.1).

A.3.5.2.7.3 Round surface mount lands. Round surface mount lands, such as Ball Grid Array (BGA) lands, using copper–defined lands, solder mask-defined lands, or solder dam designs shall comply with IPC–7095.

A.3.5.3 Coverlayer (including coverfilm and cover coat). Unless otherwise specified, the requirements specified in A.3.5.3.1 through A.3.5.3.6 shall apply to coverlayers, coverfilms, and cover coats. When the term coverlayer is used herein, it also applies to both coverfilms and cover coats.

A.3.5.3.1 Coverage. Coverlayer coverage imperfections (such as blisters, pits, skips, and voids) shall be acceptable providing the imperfection complies with the following:

a. The coverlayer imperfection shall not bridge by blisters or expose isolated conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the coverlayer imperfection shall not expose isolated conductors whose spacing is less than .020 inch (0.5 mm) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor shall not be bare copper.

d. The coverlayer imperfection does not expose plated holes or via holes that are to be tented or filled by coverlayer.

e. Blisters in the coverlayer shall not exceed the following: Two for each side, maximum size .010 inch (0.25 mm) in longest dimension, does not reduce electrical spacing between conductors by more than 25 percent.

f. Pits and voids in non-conductor areas shall be acceptable provided they have adherent edges and do not exhibit lifting or blisters in excess of that allowed in A.3.5.3.1.e.

g. The coverlayer may tent or plug via holes as specified (see A.3.1.1). Coverage between closely spaced surface mount lands shall be as specified.

h. The coverlayer does not need to be flush with the surface of the land.

A.3.5.3.2 Delamination (see figure F–8). The coverlayer shall be uniform and free of delaminations, such as creases, soda strawing, and wrinkles. Coverlayer delamination or non–lamination shall be acceptable, providing such imperfections do not violate A.3.5.1.3.1 and the following conditions are met:

a. At random locations away from conductors if each delamination is no larger than .01 square inch (6.45 square mm) and is not within .040 inch (1.0 mm) of the printed wiring board edge or coverlayer access hole or opening. The total number of the above delaminations shall not exceed three in any 1 square inch (645 square mm) of coverlayer surface area.

b. Along conductor edges, the total delamination does not exceed either .02 inch (0.51 mm) in width or 20 percent of the spacing between adjacent conductors, whichever is smaller.

c. When design requires coverage to the edge of flexible sections; chipping, delamination, lifting, or separation of the coverlayer along the edge of flexible sections shall not penetrate more than .05 inch (1.3 mm) or 50 percent of the distance to the closest conductor, whichever is less.

d. There shall be no coverlayer delamination along the outer edges of the coverlayer or openings of the coverlayer that reduces the seal below minimum edge to conductor spacing (see A.3.5.1.1).

e. There shall be not more than 3 coverlayer delaminations that exceeds 1.0 square inch (25.4 square mm) in surface area.

A.3.5.3.2.1 Wrinkles or creases. Wrinkles or creases in the coverlayer shall be acceptable provided the requirements of A.3.5.3.2 are met.

A.3.5.3.2.2 Continuous flex designs (installation use B). After exposure to the flexibility endurance test (see A.3.7.4.7 and A.4.8.4.7), there shall be no propagation of any coverlayer separation or delamination in the continuous flex area for installation use B designs.

A.3.5.3.3 Cover coat cure. The cured cover coat shall not exhibit tackiness and blistering or delamination shall not be in excess of that allowed in A.3.5.3.1 or A.3.5.3.2.

A.3.5.3.4 Registration (access holes) (see figure F–9). The coverlayer shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1) and herein. If a clearance is specified, no encroachment of the coverlayer on the land is allowed, except at the conductor attachment. The misregistration of a coverlayer defined feature shall not expose adjacent isolated conductors or lands. If no registration requirements are specified, the following shall apply:

a. For plated-through holes and vias, the following shall apply:

   (1) Coverlayer misregistration (including squeeze-out or ooze-out) onto plated-through component hole lands shall not reduce the external annular ring below the specified minimum requirements. The requirements of A.3.5.3.1.a and A.3.5.3.1.b shall also be met.

   (2) Coverlayer shall not encroach into plated-through hole barrels or onto lands of unsupported holes to which solder connections will be made.

   (3) Unless specified to be solder filled, coverlayer is permitted in plated holes or vias in which no lead is to be soldered.

b. For surface mount lands with no plated-through holes, the following shall apply:

   (1) For lands with a pitch of .050 inch (1.27 mm) or greater, coverlayer encroachment is on one side of land only and does not exceed .002 inch (0.050 mm).

   (2) For lands with a pitch less than .050 inch (1.27 mm), coverlayer encroachment shall not exceed .001 inch (0.025 mm). The encroachment can occur on adjacent sides, but not on opposite sides of the land.

c. For ball grid array lands, the following shall apply:

   (1) If the BGA land is coverlayer (or solder mask) defined, allowable misregistration of the coverlayer causes breakout of the land of not more than 90 degrees.

   (2) If the BGA land is copper defined, the coverlayer shall not encroach onto the land. Coverlayer on the land-to-via connecting conductor shall be acceptable.

   (3) If the BGA land is connected to a via and a coverlayer dam is specified, the dam shall remain in place and be continuous over the conductor to the via (no cracked, peeling, or missing coverlayer).

d. Edge-board contacts and test points which are intended for assembly testing shall be free of coverlayer unless a partial coverage allowance is specified.

e. Coverlayer shall not encroach into plated-through hole barrels or onto other surface features such as connector fingers, test points, or lands of unsupported holes to which solder connections will be made.

f. Covercoat need not be flush with the surface of the land. Misregistration of a covercoat-defined feature shall not expose adjacent isolated lands or conductors.

A.3.5.3.5 Thickness. The coverlayer thickness shall be as specified (see A.3.1.1).

A.3.5.3.6 Wicking of metallic conductor surface finish materials (plated metals or solder) (see figure F–10). The wicking of plating metals or solder shall not extend into a bend or flex transition area and shall meet the conductor spacing requirements. When wicking under coverlayers is present in non-bend or flex transition areas, the penetration of metallic conductor surface finish materials (plated metals or solder) not exceed .012 inch (0.3 mm).

A.3.5.4 Dimensions of features (interface and physical dimensions). The finished printed wiring boards shall meet the interface and physical dimensions specified (see A.3.1.1). The dimensional requirements includes items such as cutouts, overall thickness, periphery, and other design features as specified. In the event that a dimensional characteristics is not specified, the applicable class 3 of IPC–2221 design default for that characteristic shall apply.

A.3.5.4.1 Conductor pattern feature accuracy. Conductor pattern feature accuracy shall be as specified.

A.3.5.4.2 Hole pattern accuracy. The accuracy of the hole pattern (size and location) on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.4.3 Hole size. The hole size and tolerance shall be as specified. Unless otherwise specified, hole size tolerance shall be applied after plating. Nodules or rough plating in plated–through holes shall not reduce the hole diameter below the minimum limits specified.

A.3.5.4.4 Edge board contacts edge condition. The end or beveled edge of edge board contacts shall be smooth with no burrs, roughness, or lifted plating. There shall be no separation of the edge board contacts from the base material or any loose reinforcement fibers on the beveled edge. Exposed copper on the end or beveled edge of the edge board contact shall be acceptable. Conductor finish plating or coating shall comply with the requirements of A.3.5.2.5.

A.3.5.5 Solder mask (when applicable). The cured solder mask shall not exhibit any chalking, crazing, peeling, skipping, softening, swelling, wicking, or wrinkles in excess of the limits specified herein. Unless otherwise specified (see A.3.1.1), the solder mask requirements specified in A.3.5.5.1 through A.3.5.5.7 shall apply.

A.3.5.5.1 BGA lands. BGA lands using solder mask–defined lands or solder dam designs shall comply with the class 3 acceptable conditions of IPC–A–600.

A.3.5.5.2 Coverage. Solder mask coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the imperfection meets all of the following:

a. The solder mask imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the solder mask imperfection shall not expose two isolated conductors whose spacing is less than .020 inch (0.5 mm) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor shall not be bare copper.

d. The solder mask imperfection does not expose via holes that are required to be tented.

e. Bubbles, pits or voids in non-conductor areas shall be acceptable if they have adherent edges and do not exhibit blistering or lifting in excess of that allowed in A.3.7.4.4.

A.3.5.5.3 Discoloration. Discoloration of metallic surfaces under the cured solder mask is acceptable.

A.3.5.5.4 Registration (see figures F–11 and F–12). The solder mask shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If no requirements are specified, the following apply:

a. For plated-through holes and vias, the following shall apply:

(1) Solder mask misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.

(2) Solder mask shall not encroach into plated-through hole barrels or onto other surface features (such as edge board contacts, or lands of unsupported holes) to which solder connections will be made.

(3) Solder mask is permitted in plated holes or vias in which no lead is to be soldered.

b. For surface mount lands with no plated-through holes, the following shall apply:

(1) For lands with a pitch of .050 inch (1.27 mm) or greater, solder mask encroachment is on one side of land only and does not exceed .002 inch (0.050 mm).

(2) For lands with a pitch less than .050 inch (1.27 mm), solder mask encroachment is on one side of land only and does not exceed .001 inch (0.025 mm).

c. For ball grid array lands, the following shall apply:

(1) If the land is solder mask defined, allowable misregistration of the solder mask causes breakout of the land of not more than 90 degrees.

(2) If the land is copper defined, the solder mask shall not encroach onto the land. Solder mask on the land-to-via connecting conductor shall be acceptable.

(3) If solder mask dam is specified, the dam remains in place with the conductor to the via covered.

d. Edge-board contacts and test points which are intended for assembly testing shall be free of solder mask unless a partial coverage allowance is specified.

A.3.5.5.5 Soda straw voids. There shall be no visible soda straw voids between the solder mask and the printed board base material surface and the edges of the conductor patterns.

A.3.5.5.6 Solder mask cure. The cured solder mask coating shall not exhibit tackiness, blistering, or delamination.

A.3.5.5.7 Thickness. The solder mask thickness shall be as specified (see A.3.1.1).

A.3.5.6 Stiffeners.

A.3.5.6.1 Acceptability, design, and placement. The design, placement, and acceptability requirements for stiffeners shall be as specified. Adhesive squeeze-out shall not reduce the annular ring below the minimum solderable annular ring requirements.

A.3.5.6.2 Bonding. Complete bonding of the stiffener to the flexible portion of the printed wiring board is not required (see A.6.13). Unless otherwise specified (see A.3.1.1), the bonding of the stiffener to the flexible portion of the printed wiring board shall be 50 percent minimum.

A.3.5.6.3 Foreign material between the stiffener and printed wiring board surface. Foreign material determined to be located between stiffener and printed wiring board surface shall be acceptable provided the bulge of non-conductive foreign material is no larger than .004 inch (0.1 mm). The foreign material shall not be larger than 5 percent of the bonding area of the stiffener. The foreign material shall not encroach onto the land of any component hole.

A.3.5.6.4 Stiffener access hole registration. Stiffener access hole registration shall be such that the size or diameter of the access hole shall not reduce the component land area or minimum annular ring below the limits specified (see A.3.5.2.1).

A.3.5.7 Via protection.

A.3.5.7.1 Filled via, cap plating (see figure F–13). When the design requires the copper cap plating of filled vias (see A.3.1.1), all vias required to be protected shall be completely covered by the cap plating. The plated copper surface shall be planar with no indication of the filled via underneath. Visually discernable protrusions (bumps) and depressions (dimples) in the copper plating over filled vias shall be acceptable providing they meet the requirements of A.3.6.6. Voids in the copper cap plating over the filled portion of the via shall not be acceptable.

A.3.5.7.2 Unfilled via, solder mask tenting (see figure F–14). When the design requires the tenting of solder mask over unfilled vias (see A.3.1.1), all vias required to be protected shall be completely covered by solder mask. Voids in the solder mask over the via exposing the hole shall not be acceptable.

A.3.5.8 Wicking of metallic conductor surface finish materials (see figure F–10). Wicking of metallic conductor surface finish materials (coatings, platings, or solder) extending .010 inch (0.25 mm) or less into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1). Wicking of metallic conductor surface finish materials (coatings, platings, or solder) extending .012 inch (0.3 mm) or less under coverlayers in non-bend or flex transition areas shall be acceptable.

A.3.6 Plated hole structural requirements. When examined by microsection, the plated hole structures (which includes plated-through holes, blind vias, buried vias, low aspect ratio blind vias, and microvias) of the microsectioned test specimen shall meet the requirements of A.3.6.1 through A.3.6.9. If not specified on the applicable master drawing (see A.3.1.1) or herein, the requirements of A.3.3 shall be met. Barrel cracks, butt plating joints, circumferential separations, corner cracks, and cracked copper plating shall not be acceptable. Appendix G contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. The thermal zones of plated hole structures are shown on figures G–1 and G–2.

A.3.6.1 Base material. Base materials shall be used that enable the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified (see A.3.1.1), the following base material condition requirements listed in A.3.6.1.1 through A.3.6.1.8 shall apply.

A.3.6.1.1 Adhesive voids (for metal clad flexible base materials only) (see figure G–1).

A.3.6.1.1.1 Non-stressed specimens (as received condition). Adhesive voids with the longest dimension of .020 inch (0.51 mm) or less shall be acceptable. Multiple adhesive voids in the same plane between adjacent plated holes shall not have a combined length which exceeds .020 inch (0.51 mm).

A.3.6.1.1.2 Stressed specimens (after rework simulation, resistance to soldering heat, or thermal shock). After undergoing rework simulation, resistance to soldering heat, or thermal shock testing (see A.3.7.4.8, A.3.7.6.2, and A.3.7.6.3), adhesive voids are not evaluated in zone A. Adhesive voids in zone B with the longest dimension of .020 inch (0.51 mm) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements specified (see A.3.1.1).

A.3.6.1.2 Base material cracks and voids (see figure G–1).

A.3.6.1.2.1 Non-stressed specimens (as received condition). Laminate voids with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable.

A.3.6.1.2.2 Stressed specimens (after rework simulation, resistance to soldering heat, or thermal shock). After undergoing rework simulation, resistance to soldering heat, or thermal shock testing (see A.3.7.4.8, A.3.7.6.2, and A.3.7.6.3), laminate cracks and voids are not evaluated in zone A. Laminate cracks located wholly in zone A shall be acceptable. Laminate cracks and voids that originate in zone A and encroach into zone B shall not exceed a length of .003 inch (0.08 mm). Laminate cracks and voids in zone B shall not exceed a length of .003 inch (0.08 mm), shall not bridge adjacent uncommon conductors, and shall not reduce dielectric spacing, either laterally or vertically, below the minimum specified spacing. Multiple laminate cracks and voids located between two adjacent plated-through holes shall not have a combined length in excess of .003 inch (0.08 mm), shall not bridge adjacent uncommon conductors, and shall not reduce dielectric spacing, either laterally or vertically, below the minimum specified spacing.

A.3.6.1.3 Coverlayer thickness. Unless otherwise specified (see A.3.1.1), the thickness of the coverlayer shall not be measured.

A.3.6.1.4 Delamination. Printed wiring boards shall have no delaminations in excess of that allowed in A.3.5.1.3.

A.3.6.1.5 Dielectric layer thickness (see figure G–3). The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum dielectric spacing for rigid, or rigid and flex base materials, should not be less than the value specified in the IPC's 2220 series of documents for the design of flexible or rigid-flex printed wiring boards. On the date of publication of this document, the minimum dielectric spacing dimension for rigid base materials was listed as .0035 inch (0.089 mm), and when the dielectric material between conductor layers is composed of both rigid and flexible base materials, the minimum dielectric was listed as .0015 inch (0.038 mm).

A.3.6.1.6 Metal plane hole fill insulation material (see figures G–4 and G–5). Radial cracks, lateral spacing, wicking, or voids in the dielectric material used to insulate the heat sink plane or metal core from circuitry and plated through holes shall not reduce by 75 percent the specified lateral spacing between adjacent conductive surfaces. Unless otherwise specified (see A.3.1.1), the minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands, or plated-through hole and the heat sink plane shall be .004 inch (0.102 mm) or 50 percent of the specified spacing, whichever is less.

A.3.6.1.7 Hole wall to dielectric separation (resin recession) (see figure G–1).

A.3.6.1.7.1 Non-stressed specimens (as received condition). Any separation between the vertical edge of the dielectric material and the outer surface of the plated hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (0.08 mm) and the dielectric separation on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

A.3.6.1.7.2 Stressed specimens (after rework simulation, resistance to soldering heat, or thermal shock). After undergoing rework simulation, resistance to soldering heat, or thermal shock testing (see A.3.7.4.8, A.3.7.6.2, and A.3.7.6.3), resin recession at the outer surface of the plated hole barrel shall be permitted and is not cause for rejection.

A.3.6.1.8 Via fill of blind and buried vias. Unless otherwise specified (see A.3.1.1), blind vias shall be at least 75 percent filled with the via fill material (laminating resin or similar via filling material). Unless otherwise specified, buried vias shall be at least 95 percent filled with the via fill material.

A.3.6.2 Conductor pattern.

A.3.6.2.1 Conductor finish. A conductor finish plating or coating material shall be used that enables the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified (see A.3.1.1), the following conductor finish condition requirements shall apply.

A.3.6.2.1.1 Dewetting. For tin alloys, reflowed tin-lead, or solder coated surfaces, a maximum of 5 percent of dewetting is permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes not used for solder connections shall meet the requirements of J–STD–003.

A.3.6.2.1.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

A.3.6.2.1.3 Outgrowth and overhang. There shall be no outgrowth on the conductor edges when finished with fused tin-lead or solder coating. The maximum permissible outgrowth on conductor edges finished with surface finish metals other than tin-lead or solder shall be .001 inch (0.025 mm).

A.3.6.2.1.4 Protective finishes for internal metal cores or metal backing. The plating, coating, or surface treatment type and thickness of internal metal cores and metal backing materials shall be as specified (see A.3.1.1).

A.3.6.2.1.5 Thickness (plating or coating). The conductor finish plating or coating thickness shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum conductor finish plating or coating thickness should not be less than the values specified in the IPC's 2220 series of documents for the design of flexible or rigid-flex printed wiring boards. On the date of publication of this document, those values are reproduced in table A–I. (Also see A.3.5.2.5).

TABLE A–I. Conductor surface finish plating and coating thickness.

Material		Thickness, in inches (mm)
Gold (electroplated) for edge-board contacts and areas not to be soldered		.00005 (0.0013 mm) minimum
Gold (electroplated) for areas to be soldered		.000018 (0.00046 mm) maximum
Gold (electroplated) for areas to be wire bonded, ultrasonic		.000002 (0.00005 mm) minimum
Gold (electroplated) for areas to be wire bonded, thermosonic		.00003 (0.0008 mm) minimum
Nickel (electroplated); under gold areas to be wire bonded		.00012 (0.003 mm) minimum
Nickel (electroplated); edge-board contacts		.00008 (0.002 mm) minimum
Nickel (electroplated); barrier to prevent formation of Cu-Sn compounds		.00005 (0.0013 mm) minimum
Organic solderability preservative (OSP)		Solderable
Immersion silver		Solderable
Electrodeposited tin-lead, fused or solder coat		Coverage and solderable
Electrodeposited tin-lead, unfused		.0003 (0.008 mm) minimum
Solder coat over base copper		Coverage and solderable
ENIG	Electroless nickel	.00012 (0.003 mm) minimum
	Immersion gold (areas not to be soldered)	.000002 (0.00005 mm) minimum
	Immersion gold (areas to be soldered)	Solderable

A.3.6.2.2 Conductor thickness. The conductor thickness shall be as specified (see A.3.1.1).

A.3.6.2.2.1 Conductors with copper plating (after processing). When a conductor thickness is specified, the conductor thickness (metal foil and copper plating) shall be equal to or greater than the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (metal foil and copper plating) shall be within the specified tolerance for the specified thickness. If only a starting metal foil weight requirement is specified, the thickness limits for conductors with plating shall meet the requirements of table A–II. If only final metal foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity. Unless otherwise specified, the final conductor thickness of planarized layers will be less than the values in table A–II due to the reduction allowance of A.3.6.4.2.

NOTE: Conductors with copper plating are typical of external layers of multilayer designs and internal layers of sequential laminated multilayer designs.

TABLE A–II. Thickness of conductors with copper plating after processing (not planarized).

Starting copper foil weight 1/	Processing reduction allowance 2/	Minimum conductor thickness after processing		
		Type 2	Types 3 and 4 ≤ .060 (1.5 mm)	Type 3 and 4 > .060 (1.5 mm)
	inches (µm)	inches (µm)	inches (µm)	inches (µm)
1/8	.00006 (1.5)	.00052 (13.2)	.00091 (23.1)	.00130 (33.0)
1/4	.00006 (1.5)	.00064 (16.3)	.00103 (26.2)	.00143 (36.3)
3/8	.00006 (1.5)	.00076 (19.3)	.00115 (29.2)	.00156 (39.6)
1/2	.00008 (2.0)	.00092 (23.4)	.00132 (33.5)	.00171 (43.4)
1	.00012 (3.0)	.00150 (38.1)	.00189 (48.0)	.00228 (57.9)
2	.00012 (3.0)	.00270 (68.6)	.00309 (78.5)	.00349 (88.6)
3	.00016 (4.0)	.00388 (98.6)	.00428 (108.6)	.00467 (118.6)
4	.00016 (4.0)	.00510 (129.5)	.00549 (139.4)	.00589 (149.6)

1/ The starting copper foil weight is as specified on the master drawing.
2/ The processing reduction allowance does not factor in any rework processing for copper foil weights below 1/2. For weights of 1/2 and above, the processing reduction allowance accounts for one rework process.

A.3.6.2.2.2 Conductors without copper plating (after processing). When a minimum conductor thickness is specified, the conductor thickness (metal foil only) shall be equal to, or greater than, the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (metal foil only) shall be within the specified tolerance for the specified thickness. For wrought or rolled metal foil types, if only a starting metal foil weight requirement is specified, a reduction in thickness up to 5 percent below the minimum allowable foil thickness specified by the applicable material specification shall be considered acceptable in order to accommodate a processing allowance for cleaning either by chemical or mechanical means. For deposited metal foil types, if only a starting metal foil weight requirement is specified, the limits for minimum internal layer foil thickness after processing shall be in accordance with table A–III. If only final metal foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity.

TABLE A–III. Thickness of conductors without copper plating (after processing).

Starting copper foil weight	Processing reduction allowance		Minimum surface conductor thickness (after processing)	
	inches	(µm)	inches	(µm)
1/8	.00006	(1.5)	.00012	(3.048)
1/4	.00006	(1.5)	.00024	(6.096)
3/8	.00006	(1.5)	.00037	(9.398)
1/2	.00016	(4.0)	.00045	(11.43)
1	.00024	(6.0)	.00098	(24.892)
2	.00024	(6.0)	.00219	(55.6)
3	.00024	(6.0)	.00341	(86.6)
4	.00024	(6.0)	.00463	(117.6))

A.3.6.2.3 Conductor width. The conductor width shall be as specified (see A.3.1.1).

A.3.6.2.4 Annular ring, internal (see figure G–6). The minimum annular ring for functional internal lands on types 3 and 4 printed wiring boards shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum internal annular ring should not be less than the values specified in the IPC's 2220 series of documents for the design of flexible or rigid-flex printed wiring boards.

A.3.6.2.5 Bonding of conductor to base material and lifted lands (see figure G–7).

A.3.6.2.5.1 Non-stressed specimens (as received condition). There shall be no lifted lands, or evidence of lifted lands on the non-stressed microsectioned test specimen. When inspected in accordance with A.4.8.2 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with A.4.8.1 for separation of the lands from the base material.

A.3.6.2.5.2 Stressed specimens (after rework simulation, resistance to soldering heat, or thermal shock). After undergoing rework simulation, resistance to soldering heat, or thermal shock testing (see A.3.7.4.8, A.3.7.6.2, and A.3.7.6.3), the maximum allowed distance from the base material surface to the bottom of the edge of the land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and copper plating on that land.

A.3.6.2.6 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.6.3 Hole preparation prior to metallization. The presence of both flexible and rigid base materials in type 4 designs will cause varying degrees of etchback amongst the various base materials in the finished plated-through hole. In addition, all designs that make use of adhesiveless flexible base material will typically exhibit minimal etchback at the flexible dielectric to copper conductor interface.

A.3.6.3.1 Desmear (hole cleaning) (see figure G–8). When etchback is not specified on the applicable master drawing, the vertical faces of the internal conductors of holes that will be plated shall be cleaned to be free of resin smear. Lateral removal of base material from the hole wall shall not exceed .001 inch (0.03 mm). When desmear is used for hole preparation, a negative etchback of .0005 inch (0.013 mm) maximum shall be acceptable.

A.3.6.3.2 Etchback (when specified, see A.3.1.1) (see figures G–9 and G–10). When specified (see A.3.1.1), holes that will be plated shall be processed for the lateral removal of resin and reinforcement material (woven glass or other media) from the internal conductors prior to plating. Unless otherwise specified (see A.3.1.1), etchback shall be a minimum of .0001 inch (0.0025 mm) and no greater than the specified minimum internal annular ring or .002 inch (0.05 mm), whichever is less, with a preferred depth of .0005 inch (0.013 mm) when measured at the internal copper contact area protrusion (see figure G–9). The etchback shall be effective on at least the top or bottom (or both) surface of each internal conductor to provide at least a two (2) point contact with the subsequent hole plating (see figure G–10). Negative etchback is not acceptable when etchback is specified. Wicking shall meet the requirements of A.3.6.6.

A.3.6.4 Plated-through hole plating. Unless otherwise specified (see A.3.1.1), copper plating thickness applies to the hole wall, the hole knee, and the surface land of the plated-through hole (see figures G–11, G–12 and G–13).

A.3.6.4.1 Copper plating thickness (when applicable) (see figures G–11, G–12 and G–13). The copper plating thickness (on the surface, in plated-through holes, in blind and buried vias) shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum copper plating thickness should not be less than the values specified in the IPC's 2220 series of documents for the design of flexible or rigid-flex printed wiring boards. On the date of publication of this document, those values are reproduced in table A–IV for plated through holes and table A–V for blind and buried vias.

A.3.6.4.2 Wrap copper plating (see figures G–12 and G–13). Unless otherwise specified, the wrap plating (plated–through hole surface and knee continuous copper plating) thickness shall be as specified (see 1.2.6). The wrap plating shall not be reduced by more than 20 percent for grade A, 50 percent for grade B, and 80 percent for grade C of the specified wrap copper plating thickness due to planarization or other processing.

TABLE A–IV. Plated-through hole copper plating thickness.

Printed board design characteristic	Minimum average		Thin areas		Minimum wrap	
	inch	(mm)	inch	(mm)	inch	(mm)
Type 2	.0005	(0.013)	.0004	(0.010)	.0005	(0.013)
Types 3 and 4 1/	.001	(0.025)	.0008	(0.020)	.0005	(0.013)
Types 3 and 4 2/	.0014	(0.035)	.0012	(0.030)	.0005	(0.013)

1/ For designs in which the printed board is constructed of base materials of T_G equal to or greater than 110ºC in areas with plated through holes.
2/ For designs in which the board thickness is greater than .60 inch (1.5 mm) and is constructed of base materials of T_G less than 110ºC in areas with plated through holes.

A.3.6.4.3 Copper plating defects (see figures G–13 and G–14). Unless otherwise specified (see A.3.1.1), a 20 percent reduction of the specified copper plating thickness shall be acceptable if it is non-continuous (isolated; not more than 10 percent of the composite board thickness). Any copper plating less than 80 percent of the specified thickness shall be treated as a copper plating void.

TABLE A–V. Blind and buried via copper plating thickness.

Via design characteristic	Minimum average		Thin area		Minimum wrap	
	inch	(mm)	inch	(mm)	inch	(mm)
Blind vias	.001	(0.025)	.0008	(0.020)	.0003	(0.008)
Microvias, blind and buried	.0005	(0.013)	.0004	(0.010)	.00025	(0.006)
Buried vias, two layer core	.0006	(0.015)	.0005	(0.013)	.0003	(0.008)
Buried vias, core greater than 2 layers thick	.001	(0.025)	.0008	(0.020)	.0005	(0.013)

A.3.6.4.4 Copper plating voids (see figure G–15). The copper plating in the plated-through holes shall not exhibit any void in excess of the following:

a. There shall be no more than one plating void for each panel, regardless of length or size.

b. There shall be no plating void in excess of 5 percent of the total printed wiring board thickness.

c. There shall be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated-through hole exhibiting this condition shall be counted as having one void for panel acceptance purposes.

A.3.6.4.5 Wicking of copper plating (see figure G–16). When measured from the edge of the drilled hole, the wicking of copper plating into the base material shall not extend past the calculated allowable wicking limit provided this limit does not reduce the conductor spacing below the minimum clearance spacing requirements specified. The maximum allowable wicking limit is calculated by adding the hole cleaning dielectric removal value (desmear or ecthback) plus the .003 inch (0.08 mm) allowance for wicking. See A.3.6.3.1 for dielectric removal value for desmear, or if applicable, A.3.1.1 and A.3.6.3.2 for the specified etchback value. The combination of wicking, hole cleaning dielectric removal value, and any non-contiguous tears or drill gouges caused by hole formation shall not exceed the calculated allowable wicking limit.

A.3.6.5 Conductive interfaces and separations. The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, nonmetallic conductive coatings, or vacuum deposited copper, and electrolytic copper, whether panel or pattern plated) shall also be considered a conductive interface.

A.3.6.5.1 Copper to copper interfaces (see figure G–17). Except along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall copper conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable.

A.3.6.5.2 Dissimilar metal interfaces. For printed wiring board designs containing metal cores with dissimilar metals (such as copper-invar-copper), contamination or separation at the conductive interface shall not exceed 20 percent of the thickness of the dissimilar metal.

A.3.6.6 Via cap plating (see figures G–18 and G–19).

A.3.6.6.1 Thickness. For designs that specify copper plating for via protection, the minimum via cap plating thickness over filled vias shall be as specified (see A.3.1.1). If not specified, the minimum via cap copper plating thickness over filled vias shall be in accordance with the minimum wrap copper plating thickness specified in table A–IV.

A.3.6.6.2 Cap plating imperfections. When cap plating of a filled via is specified, voids in the plating over the via fill shall not be acceptable. Separation of the via cap plating to via fill material shall be acceptable. Separation of the via cap plating to underlying plating shall not be acceptable. Depressions (dimples) below the surface of the land shall be no greater than .003 inch (0.08 mm). Protrusions (bumps) of the cap plating above the surface of the land shall be no greater than .002 inch (0.051 mm).

A.3.6.7 Hole wall deficiencies (see figures G–20 and G–21). Nodules, plating folds, or plated glass fibers that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below the limits specified (see A.3.1.1). Isolated areas of reduced copper thickness due to glass fiber protrusions shall meet the minimum thickness requirements specified, when measured from the end of the protrusion to the edge of the hole plating.

A.3.6.8 Metallic cracks (see figure G–22). There shall be no cracks in the internal layer conductive foils, platings, or coatings. Cracks in outer layer metal foil shall be acceptable if they do not propagate into the plated copper. Cracks shall not be acceptable in the copper plating.

A.3.6.9 Nail-heading. Nail-heading of conductors shall not exceed 1.5 times the copper foil thickness.

A.3.7 Inspection requirements. The detailed requirements contained in this section, although determined by examination of sample printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.7.1 External visual and dimensional acceptability (of printed wiring boards). When examined as specified in A.4.8.1, the printed wiring boards shall be in accordance with the requirements specified in A.3.1.1 (master drawing), A.3.4 (material), A.3.5 (visual and dimensional), A.3.8 (marking), A.3.10 (repair), and A.3.12 (workmanship).

A.3.7.2 Destructive physical analysis (DPA) by metallographic evaluation of printed wiring board test specimens. When printed wiring board test specimens (finished printed wiring boards, supporting test coupons, or qualification test specimens) are microsectioned and examined as specified in A.4.8.2, the requirements specified in A.3.1.1, A.3.3, and A.3.6 shall be met.

A.3.7.2.1 Non-stressed specimens (as received condition). After meeting the requirements of A.3.8 and A.3.12 when inspected in accordance with A.4.8.1, the non-stressed (as received) printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and the requirements of A.3.1.1, A.3.3, and A.3.6 shall be met.

A.3.7.2.2 Registration, internal.

A.3.7.2.2.1 By microsection (method II). Unless otherwise specified (see A.3.1.1), when inspected as specified in A.4.8.2.2, the layer-to-layer pattern misregistration shall not reduce the minimum annular ring below the limits specified (see A.3.1.1).

A.3.7.2.2.2 By registration test coupons (method III) (optional). Registration test coupons may have been designed into the printed wiring board by the design activity, or may be added to the panel by the manufacturer to enhance testability (see A.4.8.2.4.2 and appendix H). To be usable for acceptance purposes, registration test coupons shall relate the actual grid location of each circuitry layer to all other circuitry layers and to the hole pattern accuracy required (see A.3.5.4) in each printed wiring board.

A.3.7.3 Chemical requirements.

A.3.7.3.1 Ionic contamination (cleanliness). When printed wiring boards are tested in accordance with A.4.8.3.1, the levels of ionic contamination shall be in accordance with the requirements of A.3.7.3.1.1 or A.3.7.3.1.2, as applicable. The sodium chloride salt equivalent ionic contamination test equipment specified in A.6.4.2 can be used in lieu of the method specified in A.4.8.3.1. When printed wiring boards are tested using the sodium chloride salt equivalent ionic contamination test equipment specified in A.6.4.2, the final value shall be less than equivalents of sodium chloride specified for the printed wiring board surface area tested.

A.3.7.3.1.1 Prior to the application of solder mask (see A.6.4). Unless otherwise specified (see A.3.1.1), the level of ionic contamination shall not exceed 10.06 micrograms/square inch (1.56 micrograms/square centimeter) prior to the application of solder mask.

A.3.7.3.1.2 Completed inner layer prior to lamination (when specified, see A.3.1.1 and A.6.2.2.g). The levels of ionic contamination for completed inner layers prior to lamination shall be as specified (see A.3.1.1).

A.3.7.3.1.3 Completed printed wiring boards (when specified, see A.3.1.1 and A.6.2.2.g). The levels of ionic contamination for completed printed wiring boards shall be as specified (see A.3.1.1).

A.3.7.3.2 Resistance to solvents (inks or paints). After ink or paint based markings or legends are tested in accordance with A.4.8.3.2, any specified markings or legends which are missing in whole or in part, faded, smeared, of shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

A.3.7.4 Physical requirements.

A.3.7.4.1 Adhesion, coverlayer (including coverfilm and cover coat). When tested as specified in A.4.8.4.1, the maximum percentage of cured coverlayer lifted from the conductors, lands, or surface of the printed wiring board test specimen shall be in accordance with the following:

a. Bare copper or base material: Maximum percentage of lifting 0 percent.

b. Gold or nickel plating: Maximum percentage of lifting 5 percent.

c. Melting metals (tin-lead plating, solder coating, indium, bismuth, and others): Maximum percentage of lifting 10 percent.

A.3.7.4.2 Adhesion, legend and marking. After legends or marking are tested in accordance with A.4.8.4.2, any specified legend or markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it is no longer legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

A.3.7.4.3 Adhesion, plating. When tested as specified in A.4.8.4.3, there shall be no plating particles or conductor patterns removed from the printed wiring board test specimen except for outgrowth.

A.3.7.4.4 Adhesion, solder mask. When tested as specified in A.4.8.4.4, the maximum percentage of cured solder mask lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall be in accordance with the following:

a. Bare copper or base material: Maximum percentage of lifting 0 percent.

b. Gold or nickel plating: Maximum percentage of lifting 5 percent.

c. Melting metals (tin-lead plating, solder coating, indium, bismuth, and others): Maximum percentage of lifting 10 percent.

A.3.7.4.5 Bow and twist (stiffener sections). When tested as specified in A.4.8.4.5, the maximum allowable bow and twist for rigid or stiffener sections of the printed wiring board shall be, unless otherwise specified (see A.3.1.1), 0.75 percent for designs that use surface mount components and 1.5 percent for all other designs.

A.3.7.4.6 Flexibility endurance (installation use B only). When tested as specified in A.4.8.4.6, printed wiring board test specimen shall be capable of withstanding the specified conditions of A.3.7.4.6.1 or A.3.7.4.6.2, as applicable, without any evidence of damage, degradation or rejectable delamination. After the test, the requirements specified in A.3.5.3.2 and A.3.7.5.1 shall be met.

A.3.7.4.6.1 Qualification and periodic testing. Printed wiring board test specimen shall be capable of withstanding the specified number of cycles without any evidence of damage, degradation, or rejectable delamination.

A.3.7.4.6.2 User specified (see A.3.1.1 and A.6.2.2). The number of flexing cycles, flexing rate, and points of application of the flexing, travel of loop (if other than 1.0 inch (25.4 mm) minimum), and diameter of mandrel (when applicable) shall be specified (see A.3.1.1). If no parameters are specified, use the qualification and lot acceptance test default values of A.4.8.4.6.

A.3.7.4.7 Folding flexibility (installation use A only). When tested as specified in A.4.8.4.7, printed wiring board test specimen shall be capable of withstanding the specified conditions of A.3.7.4.7.1 or A.3.7.4.7.2, as applicable, without any evidence of damage, degradation, or rejectable delamination. After the test, the electrical requirements specified in A.3.7.5.1 and A.3.7.5.2 shall be met.

A.3.7.4.7.1 Qualification and periodic testing. The number of fold cycles shall be 25 cycles in both directions. The point of application shall be the center of the printed wiring board test specimen, orthogonal to the longest length. The mandrel size for types 1 and 2 shall be 12 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel size for types 3, 4, and 5 shall be 24 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel shall not be less than .125 inch (3.18 mm).

A.3.7.4.7.2 User specified (see A.3.1.1 and A.6.2.2). The folding flexibility test parameters shall be as specified (see A.3.1.1). The minimum parameters specified on the master drawing shall be as follows:

a. Direction of bend.

b. Degree of bend.

c. Number of fold cycles.

d. Diameter of mandrel.

e. Points of application.

A.3.7.4.8 Rework simulation. Rework simulation is not applicable for printed wiring board designs that do not use any plated through-holes for component attachment.

A.3.7.4.8.1 Grade R, types 1 and 5 with unsupported holes (bond strength). After undergoing the test specified in A.4.8.4.8.1, the unsupported land shall withstand 5 pounds (2.27 Kg) pull or 500 lb/in (3.4 MPa), whichever is less.

A.3.7.4.8.2 Grade R, types 2, 3 and 4 with plated-through holes. After undergoing the test specified in A.4.8.4.8.2, the type 2, 3 or 4 printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of blistering or delamination in excess of that allowed in A.3.5.

b. Internal visual and dimensional inspection: The printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and the requirements specified in A.3.6 shall be met.

A.3.7.4.8.3 Grade U. Printed wiring boards designs requiring grade U rework simulation shall be subjected to only the first solder cycle of the test routines specified in A.3.7.4.8.1 or A.3.7.4.8.2, as applicable.

A.3.7.4.9 Solderability. Solderability testing is applicable only on printed wiring board designs that require soldering during circuit card assembly processes. Unless otherwise specified (see A.3.1.1), printed wiring board designs that use compliant pin technology only for component attachment do not require solderability testing. Unless otherwise specified, printed wiring board designs that use surface mount components only shall be tested for surface solderability.

A.3.7.4.9.1 Hole (plated-through hole) solderability. After undergoing the test specified in A.4.8.4.9.1, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting) specified in J–STD–003 class 3 or the solderability test methods described in appendix G of MIL–PRF–31032, as applicable.

A.3.7.4.9.2 Surface (or surface mount land) solderability. After undergoing the test specified in A.4.8.4.9.2, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting) specified in J–STD–003 class 3 or the solderability test methods described in appendix G of MIL–PRF–31032, as applicable.

A.3.7.4.10 Solder mask cure. When tested as specified in A.4.8.4.10, the cured solder mask coating shall not exhibit tackiness, blistering, or delamination.

A.3.7.4.11 Surface peel strength (types 3 and 4 foil laminated printed wiring boards). When tested as specified in A.4.8.4.11, the surface conductor shall withstand a minimum peel strength greater than or equal to the "after thermal stress" values for the corresponding copper foil profile as specified by either the applicable base material specification or the master drawing. If no value for peel strength is listed in the base material specification or on the master drawing for the copper foil used (as is the case with many low and very low profile or rolled-annealed foils), then a value that is 50 percent of the standard profile copper foil shall be used. Unless otherwise specified (see A.3.1.1), the peel strength values for base material thicknesses over .0197 inch (0.500 mm) specified by the base material specification shall be used. This requirement is only applicable to foil laminated types 3 and 4 printed wiring boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

A.3.7.5 Electrical requirements.

A.3.7.5.1 Circuit continuity and shorts. When specified (see A.3.1.1) that it is acceptable, verification of circuit continuity and shorts by indirect testing by signature comparison may be used for production screening.

A.3.7.5.1.1 Circuit continuity. When tested as specified in A.4.8.5.1, the resistance between the endpoints of conductor patterns within a network of conductors shall be as specified (see A.3.1.1). For qualification inspection there shall be no circuits whose resistance exceeds 20 ohms. Unless otherwise specified (see A.3.1.1), for production printed wiring boards, there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum for each inch of circuit length shall apply. Conductor patterns that consist of long runs of narrow conductors or short runs of very wide conductors may increase or decrease the resistance. The acceptability of these type of circuits, of controlled impedance nets, or of embedded resistive patterns shall be specified.

A.3.7.5.1.2 Circuit shorts (isolation resistance). When tested as specified in A.4.8.5.1, the insulation resistance between mutually isolated conductors shall be as specified (see A.3.1.1) Unless otherwise specified (see A.3.1.1), for production printed wiring boards, the insulation resistance shall be greater than 10 megohms.

A.3.7.5.2 Circuit or plated-through hole short to metal core substrate. When printed wiring board designs with metal cores are tested in accordance with A.4.8.5.2, the dielectric material used to insulate the heat-sinking plane from circuitry and plated through holes shall provide an insulation resistance greater than 2 megohms. Electrical access to the metal core substrate shall be provided in the design when this test is to be performed.

A.3.7.5.3 Dielectric withstanding voltage (DWV). When inspected as specified in A.4.8.5.3, there shall be no flashover, sparkover, or breakdown between isolated conductors.

A.3.7.5.4 Impedance testing (when specified). When impedance resistance values are specified, all printed wiring boards shall be electrically testing tested as specified in A.4.8.5.4.

A.3.7.6 Environmental requirements.

A.3.7.6.1 Moisture and insulation resistance (MIR). When tested as specified in A.4.8.6.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.2 Resistance to soldering heat.

A.3.7.6.2.1 Solder float thermal stress (single side, single cycle, component holes).

A.3.7.6.2.1.1 Types 1 and 5. After undergoing the test specified in A.4.8.6.2, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and shall not exhibit any cracking or separation of plating and conductors, blistering or delamination of base materials shall not exceed the limits allowed in A.3.5.1.3, and lands shall not lift in excess of that allowed in A.3.5.2.1.

A.3.7.6.2.1.2 Types 2, 3, and 4. After undergoing the test specified in A.4.8.6.2, the printed wiring board test specimen shall be examined in accordance with A.4.8.1 and shall exhibit no blistering or delamination in excess of that allowed in A.3.5.1.3. After meeting the visual and dimensional requirements of A.3.5, the printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and the requirements of A.3.6 shall be met.

A.3.7.6.3 Thermal shock. While undergoing the test specified in A.4.8.6.3, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, the printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection (all types): When inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.

b. Internal visual and dimensional inspection (types 3 and 4): When the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.8 Marking.

A.3.8.1 Product identification and test vehicle traceability codes. Unless otherwise specified (see A.6.2), each production printed wiring board, each qualification test specimen, and each set of quality conformance test circuit strips (as opposed to each individual test coupon) shall be marked as specified (see A.3.1.1) and herein. As a minimum, each production printed wiring board, qualification test specimen, or quality conformance test circuit strip shall be marked with the printed wiring board manufacturers' CAGE code (see 6.4.5), lot date code (see A.3.8.5), and traceability code (see A.7.15). Additional marking on the printed wiring boards is allowed provided it does not interfere with the required marking.

A.3.8.2 Legend. Legends on printed wiring boards shall be as specified (see A.3.1.1).

A.3.8.3 Methods of producing legend and marking. Legend and marking shall be produced by one of the following methods: the same process used in producing the conductive pattern; or the use of a fungistatic ink or paint applied to the printed wiring board; or on a label which is applied to the printed wiring board; or by a mechanical pencil, mechanical machining, or laser machining on a metallic area provided for marking purposes. Conductive legends or marking shall be no closer to the conductive pattern of the printed wiring board than the spacing requirements specified (see A.3.1.1).

A.3.8.4 Marking legibility. All marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards, shall remain legible after all tests, and in no manner affect printed wiring board performance. After any or all tests, product identification or traceability marking shall comply with the class 3, acceptable conditions specified in IPC–A–600.

A.3.8.5 Lot date code. The lot date code is a unique code to identify the period during which the printed wiring boards were manufactured. Unless otherwise specified by the acquiring activity (see A.3.1.1), the first two numbers in the lot date code shall be two digits of the number of the year, and the third and fourth number shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be proceeded by a zero reading from left to right or from top to bottom, the code number shall designate the year and week, in that order.

A.3.9 Traceability. Traceability shall be available for review by the qualifying or contracting activity for a minimum of 3 years after delivery of the printed wiring boards. Unless otherwise specified (see A.6.2.1), supporting test data, test coupons, and microsection mounts shall be retained by the manufacturer. Lost or inadequate quality records, supporting data, and test coupons (including microsection mounts and untested test coupons) may result in loss of qualification.

A.3.9.1 Quality–conformance test circuitry, test coupons, and microsection mounts. Each quality–conformance test circuitry (QCTC) shall be identifiable with those corresponding production printed wiring boards produced on the same inspection panel that also produced the QCTC. Unless otherwise specified (see A.3.1.1), each QCTC shall be traceable to its originating position on the panel. All individual test coupons (including those in microsection mounts) separated from its QCTC, or qualification test specimen, shall have its traceability maintained back to the inspection panel, QCTC, or qualification test specimen from where the test coupons originated. When a QCTC or test coupon is representative of more than one printed wiring board design (multiple designs on each panel), it shall be traceable to those printed wiring boards fabricated on that inspection panel. When a microsection mount contains more than one specimen, an orientation mark or other identification marking shall identify layer one of the first specimen. Unless otherwise listed on the multiple specimen microsection mount, traceability identifying all specimens contained in a mount shall be maintained.

A.3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified (see A.3.1.1) or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

A.3.9.3 Serialization. When the contract requires the printed wiring boards to be serialized, each printed wiring board or qualification test specimen shall be marked with a unique serial number assigned consecutively within the inspection lot, allowing traceability of the printed wiring board and its test results.

A.3.9.4 Quality records. A system shall be in place to track all quality records, including but not limited to, the results of all qualification tests, the results of all inspection of product for delivery tests (binary or variables data), any required failure analysis, and contract services records. The retention period for each type of quality records shall be a minimum of 3 years.

A.3.10 Rework and repair.

A.3.10.1 Rework. The touch-up of surface imperfections in the base material, removal of residual plating materials or extraneous copper shall be permitted when such action does not affect the functional integrity of the printed wiring board.

A.3.10.2 Repair. When inspected in accordance with A.4.8.1, printed wiring boards shall not be repaired or reveal any evidence of repair.

A.3.11 Recycled, recovered, or environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.12 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free of defects in excess of those allowed in this appendix that could affect life or serviceability.

A.4 VERIFICATION

A.4.1 Classification of inspections. The inspections requirements specified herein are classified as follows:

a. Qualification inspection (see A.4.5).

b. Inspection of product for delivery (see A.4.6).

c. Periodic conformance inspection (see A.4.7).

A.4.2 Test and measuring equipment. Measuring and test equipment of sufficient accuracy, quality, and quantity to permit performance of the required inspection shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with section C.5 of appendix C, or equivalent.

A.4.3 Inspection conditions. Unless otherwise specified in the applicable test method or procedure, inspections and tests shall be performed in accordance with test method number 1.3 of IPC–TM–650.

A.4.4 Printed wiring board performance verification. Printed wiring board performance verification shall consist of inspections on the production printed wiring boards and the QCTC or test coupons referenced in tables herein for in-process, groups A, B, and C inspections. Selection of test coupons for testing shall be in accordance with the applicable inspection table. Each production printed wiring board or panel of printed wiring boards shall include sufficient test coupons to complete the applicable verification requirements specified. The design of test coupons shall be as specified on the applicable master drawing (see A.3.1.1). The minimum number of test coupons on the production panel and the requirements for positioning the test coupons on the inspection panel shall be in accordance with the requirements of appendix H.

A.4.5 Qualification inspection (see A.6.3). Qualification inspection shall be performed at the manufacturing location and a laboratory acceptable to the Government on sample qualification test specimens produced with material, equipment, processes, and procedures normally used in production. The requirements for qualification to the QPL product assurance level shall be in accordance with appendix E.

A.4.5.1 Retention of qualification. To retain qualification, the manufacturer shall make available to the qualifying activity data concerning production of qualified product at 12 month intervals. The qualifying activity shall establish the initial reporting date. The retention of qualification data shall consist of:

a. A summary of the results of the tests performed for inspection of product delivery (in-process and group A) indicating as a minimum the number of lots that have passed and the number of lots that have failed. The results of tests of all reworked lots shall be identified and accounted for.

b. A summary of the results of tests performed for groups B inspection performed and completed during the 12 month period. Group B shall be performed only for those months in which production occurred.

c. The actual test data for groups A and B or all shall be supplied to the qualifying activity upon request.

d. The extent of qualification specified in E.4 shall apply.

e. In the event that no production occurred during the 12-month period, the manufacturer shall certify that it still has the capabilities and facilities necessary to produce and test the qualified product.

A.4.5.2 Failure to submit retention data. Failure to communicate with the qualifying activity within 60 calendar days after the end of the 12 month period may result in loss of qualification. In addition, the manufacturer shall notify the qualifying activity within 3 business days if at any time during the 12 month period that the results of periodic inspection indicates failure of the qualified product to meet the performance requirements of this appendix.

A.4.5.3 Non-production during reporting period. In the event that there is no production of any compliant printed wiring boards during the 12 month reporting period, the manufacturer shall certify that it retains the capabilities and facilities necessary to produce and test the qualified product. If during two consecutive reporting periods there has been no production of the qualified product, the manufacturer may be required, at the discretion of the qualifying activity, to submit a representative product to partial or full re-qualification testing. For the case when the manufacturer is listed for more than one flexible base material type on the QPL and there has been no production of the qualified product of one or all qualified base material types, the manufacturer may be required, at the discretion of the qualifying activity, to submit a representative product of those base material types to testing.

A.4.5.4 Requalification. Requalification is not required as long as the manufacturer maintains its QPL qualification or a listing for an equivalent technology to be supplied to this appendix on QPD–31032.

A.4.6 Inspection of product for delivery. Inspection of product for delivery shall consist of in-process and group A inspection. Except as specified in A.4.7.1.4, delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of the periodic inspection. Anomalies or defects noted on sample printed wiring boards or test coupons (or both) defined herein shall be recorded and the proper corrective action shall be initiated. Manufacturers that are qualified to use sub-contract services are still responsible for in-process and group A inspections and shall be subject to loss of qualification if the results of in-process and group A inspections indicate failure of the product to meet the applicable requirements.

A.4.6.1 In–process inspection. Each inspection lot of printed wiring boards or panels, as applicable, shall be inspected in accordance with table A–VI. When permanent solder mask is specified (see A.3.1.1), the in-process inspections specified in subgroups 1, 2 and 3 of table A–VI shall be performed prior to solder mask application. Prior to lamination of type 3 or 4 printed wiring boards, the in-process inspections specified in subgroup 2 of table A–VI shall be performed.

A.4.6.1.1 Inspection lot.

A.4.6.1.1.1 Subgroup 1. An inspection lot shall correspond to each production lot or each change of shift of work force, whichever occurs first. Production lots may be grouped based on same materials, same type or types of interfacial connections and terminations, and same processing requirements.

A.4.6.1.1.2 Subgroup 2. An inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.1.2 Sample size. The number of printed wiring boards or panels to be selected from each inspection lot for examination shall be in accordance with table A–VI. All samples shall be chosen randomly.

A.4.6.1.3 Rejected lots. If an inspection lot is rejected as a result of a failure to pass the subgroup 1 tests specified, the manufacturer shall withdraw the lot, take corrective action in connection with the cleaning materials and procedures, reclean the lot and resubmit the lot for reinspection. Printed wiring boards shall not be acceptable if the permanent solder mask coating has been applied to a contaminated surface. If an inspection lot is rejected for subgroup 2 or 3 tests, the manufacturer may screen (100 percent inspection) out the defective units (printed wiring boards or panels). Defective printed wiring boards shall not be shipped.

TABLE A–VI. In–process inspection.

Inspection	Requirement paragraph	Method paragraph	Sample size 1/	Notes
Subgroup 1				
Material	A.3.4	A.4.8.1.8	See A.4.8.1.8	
Ionic contamination (cleanliness)	A.3.7.3.1	A.4.8.3.1	Plan BN or TL	2/
Subgroup 2				
Conductor spacing	A.3.5.2.2	A.4.8.1	Plan BH	2/ 3/
Conductor width	A.3.5.2.3	A.4.8.1	Plan BH	2/ 3/
Conductor pattern imperfections	A.3.5.2.4	A.4.8.1	Plan BH	2/ 3/

1/ See appendix C, table C–I for C = 0 sampling plans.
2/ The verification shall be performed prior to solder mask or coverlayer application.
3/ The verification shall be performed prior to lamination on each production lot.

A.4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in table A–VII. The qualified manufacturer shall be responsible for completion of all group A inspections and shall be subject to loss of qualification for failure not to complete or to have completed all group A test and inspections.

A.4.6.2.1 Inspection lot. A group A inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.2.2 Sampling procedures. Statistical sampling and inspection shall be in accordance with appendix C. For 100 percent inspection, all rejected units (printed wiring boards or panels of printed wiring boards) shall not be supplied on the contract. All sample units shall be chosen randomly. The following details on panel/test coupon sampling shall apply:

a. Non-stressed specimen (as received condition) microsection evaluations (see A.3.7.2.1):

(1) Types 2 and 5: The test specimen shall be test coupon "A". The number of sample units to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series L. The samples for the as-received condition and resistance to soldering heat testing shall be selected from different panels.

(2) Types 3 and 4: One "A" or "AB-R" test coupon for each panel shall be microsectioned and inspected (see A.4.6.2.2.d.2). The orientation of the as-received condition microsection shall be orthogonal to the resistance to soldering heat microsection.

b. Solderability (see A.3.7.4.9):

(1) For Sequential Electrochemical Reduction Analysis (SERA), samples shall be selected in accordance with appendix G of MIL–PRF–31032.

(2) For J–STD–003 or the solderability test methods of appendix G of MIL–PRF–31032: When test coupon "S" is the test specimen, the number of sample units to be tested shall be based on a statistical sample of the number of panels in the lot in accordance with appendix C, table C–I, series L. When test coupon "A" is the test specimen, the number of sample units to be tested shall be based on the same statistical sample of test coupon "S", but a multiple of 4 shall be applied to the resulting sample size.

c. Resistance to soldering heat (solder float thermal stress) (see A.3.7.6.2).

(1) Types 1 and 5: The test specimen shall be test coupon "B". The number of sample units to be tested and inspected shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series L. The samples for as-received condition and resistance to soldering heat testing shall be selected from different panels.

(2) Type 2: The test specimen shall be test coupon "B". The number of sample units to be tested and microsection inspected shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series L.

(3) Types 3 and 4: The test specimen shall be test coupon "B" or "AB-R". A minimum of one test specimen for each panel shall be tested and microsection inspected. Additional sample units shall be microsectioned based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series J. For designs with blind or buried vias, at least one additional test coupon "B" for each panel shall be subjected to the resistance to soldering heat test in accordance with A.4.8.6.2 and inspected to the requirements of A.3.7.2 for each additional copper plating process used (see A.6.12 for additional guidance).

d. Registration.

(1) Method I (types 1, 2, and 5 only): When method I is used, registration shall be evaluated using any combination of "A" test coupons taken from diagonal corners of the inspection panel.

(2) Method II (types 3 or 4 only): When method II is used, registration shall be evaluated using any combination of two microsectioned test specimens taken from diagonal corners of the inspection panel. Both sample units shall have been microsectioned in the vertical plane with one sample unit representing the panel's length (X) direction and the other representing the panel's width (Y) direction. Test coupons from the as-received condition (see A.3.7.2.1), resistance to soldering heat (see A.3.7.6.2) or when available, hole solderability (see A.3.7.4.9.1) verifications may be used.

(3) Method III: When method III is to be used, the number of sample units needed for verifying registration shall be documented in the qualifying activity approved alternate test plan (see C.5.2.2).

e. Copper plating voids (see A.3.6.4.4). When a single plating void that is within the acceptable limits of A.3.6.4.4 is present in a microsection or set of microsections representing an inspection panel, a referee sample unit from that panel shall be microsectioned and inspected for copper plating voids. The referee microsection shall be performed using an "A" or "B" test coupon from the opposite corner of the suspect panel. If the referee microsection has no plating voids, then that panel is acceptable, however, if a plating void is present in the referee microsection, that panel of printed wiring boards shall be rejected. Any plated-through hole in the microsection failing the plating void criteria specified in A.3.6.4.4 subparagraphs a, b, or c, shall be cause for the entire inspection panel of printed wiring boards associated with the microsection to be rejected.

TABLE A–VII. Group A inspection.

Inspection	Requirement paragraph	Method paragraph	Test specimen 1/					Sample plans 2/
			T1	T2	T3	T4	T5	
Visual and dimensional								
External visual and dimensional acceptability	A.3.7.1	A.4.8.1	PWB	PWB	PWB	PWB	PWB	Plan BH 3/ 4/
Registration (method I)	A.3.5.2.7	A.4.8.1.3	5/	5/			5/	Plan BJ/TJ see 6/
DPA by microsection								
Non-stressed specimens	A.3.7.2.1	A.4.8.2	6/	6/	6/	6/	6/	See 6/
Registration (method II)	A.3.7.2.2	A.4.8.2.4			6/	6/		See 6/ and 7/
Chemical								
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	8/	8/	8/	8/	8/	See 8/
Physical								
Adhesion, coverlayer	A.3.7.4.1	A.4.8.4.1	9/	9/	9/	9/	9/	Plan BN/TN 9/
Adhesion, legend	A.3.7.4.2	A.4.8.4.2	10/	10/	10/	10/	10/	Plan BN/TN 10/
Adhesion, plating	A.3.7.4.3	A.4.8.4.3	11/	11/	11/	11/	11/	Plan BH/TJ 3/
Adhesion, solder mask	A.3.7.4.4	A.4.8.4.4	G	G	G	G	G	Plan TJ 12/
Bow and twist	A.3.7.4.5	A.4.8.4.5	PWB	PWB	PWB	PWB	PWB	Plan BH 13/
Solderability								
Hole	A.3.7.4.9.1	A.4.8.4.9.1		14/	14/	14/		See 6/ 14/
Surface	A.3.7.4.9.2	A.4.8.4.9.2	15/	15/	15/	15/	14/	Plan BH/TJ 6/ 15/
Solder mask cure	A.3.7.4.10	A.4.8.4.10				16/		Plan TJ 16/
Electrical								
Circuit continuity	A.3.7.5.1.1	A.4.8.5.1.1			PWB	PWB		100 percent 17/
Circuit shorts	A.3.7.5.1.2	A.4.8.5.1.1			PWB	PWB		100 percent 17/
Environmental								
Resistance to soldering heat	A.3.7.6.2.1	A.4.8.6.2.1	6/	6/	6/	6/	6/	See 6/

1/ T1 designates a type 1 design; T2 designates a type 2 design; T3 designates a types 3 design; T4 designates a type 4 design, and T5 designates a type 5 design; PWB means inspect the entire production printed wiring board, whereas an individual test coupon designation means inspect the specified test coupon. See appendix D herein for test coupon identification (name) translation to the applicable design standard.
2/ See appendix C, table C–I for C = 0 sampling plans and C.4.5 for examples.
3/ Some attributes may need to be inspected prior to lamination or solder mask application.
4/ The solder mask thickness test can be performed on either a test coupon at a sampling of TJ or production printed wiring board at a sampling of BH, manufacturer's option.
5/ Test coupon "A" or a production printed wiring board shall be used at the manufacturer's option.
6/ See A.4.6.2.2 for test specimen description and sample size. Type 1 test specimens do not require a DPA by microsection evaluation.
7/ An optional method of verifying registration using test coupons (method III) is available. See A.4.8.2.4.2 for details.
8/ See A.4.8.3.2.1 for test specimen description and sample size.
9/ See A.4.8.4.1 for test specimen description.
10/ See A.4.8.4.2 for test specimen description.
11/ Test coupons "C", "M", or a production printed wiring board shall be used at the manufacturer's option. Applicable to platings only. This inspection does not need to be performed on solder or organic coatings.

TABLE A–VII. Group A inspection – Continued.

12/ For printed wiring board designs using permanent solder mask on the production board. If the design does not require solder mask, then the test does not need to be performed.
13/ Rigidized sections or stiffener portions only.
14/ Test coupon "A" or "S" shall be used at the manufacturer's option.
15/ PWB, or test coupon "C" or "M", manufacturer's option. For printed wiring boards using only surface mount lands for component attachment, the surface solderability test can be used in lieu of the hole solderability test.
16/ Test coupon "G" or "T" shall be used at the manufacturer's option.
17/ Types 3 and 4 printed wiring boards only. NOTE: It is assumed that both continuity and circuit shorts can be visually verified for types 1, 2, and 5. If continuity and circuit shorts cannot be verified using visual inspection, then the production printed wiring boards shall be tested using a sample size in accordance with appendix C, table C–I, series H.

A.4.6.2.3 Alternative to sampling inspection (first piece produced design inspection see A.7.18). In lieu of performing sample inspections of all characteristics or parameters detailed on the master drawing, manufacturers may use first piece produced design inspection. This type of inspection is only applicable to the criteria described in A.4.6.2.3.1 and A.4.6.2.3.2. First item produced design inspection can be performed on the first printed wiring board that is representative of all printed wiring boards in the production lot of the design. The use of automated inspection technology shall be acceptable.

A.4.6.2.3.1 Board and conductor pattern features. Unless otherwise specified, the accuracy of board and conductor pattern features may be verified by performing first piece produced design inspection on a representative first production run part or by sampling the printed boards in the lot.

A.4.6.2.3.2 Hole pattern accuracy. Unless otherwise specified, only the holes that are specifically dimensioned on the master drawing shall be inspected for hole pattern accuracy to meet the board dimensional requirements specified. Unless otherwise specified, the accuracy of the hole pattern may be verified by performing first piece produced design inspection on a representative first production run part or by sampling the printed boards in the lot. Unless otherwise specified, the hole pattern accuracy of nonspecifically dimensioned holes, such as plated through holes and vias, do not need to be checked as their locations are set by the design activity supplied database and are controlled by external and internal annular ring requirements.

A.4.6.2.4 Rejected lots. If an inspection lot is rejected, the manufacturer may rework it to correct the defects and resubmit the lot for reinspection, or screen out the defective units (if possible). Resubmitted lots shall be inspected using tightened inspection (see appendix C). Such lots (reworked or screened) shall be clearly identified as reinspected lots. Products which have failed any group A inspection and have not been reworked and have not passed reinspection (as specified in this appendix) may not be delivered as compliant printed wiring boards.

A.4.6.2.5 Disposition of sample units. Sample printed wiring boards which have passed all of group A inspection may be delivered if the inspection lot is accepted.

A.4.7 Periodic conformance inspection. Periodic conformance inspection shall consist of groups B and C inspection. Except where these inspections show noncompliance with the applicable requirements (see A.4.7.1.4 and A.4.7.2.4), delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of these periodic inspections. Periodic inspections shall be performed at a certified suitable laboratory (see A.6.5). Because of the performance nature of this document, the design details of the printed wiring boards represented by the sample units need to be made available to the testing facility (see A.6.7 and C.6.1). Because of the performance nature of this document, the design details of the printed wiring boards represented by the sample units will need to be supplied to the testing facility (see A.6.7).

A.4.7.1 Group B inspection. Group B inspection shall consist of the inspections specified in table A–VIII.

A.4.7.1.1 Inspection lot. The sample units (printed wiring board test specimens) shall be randomly selected from the most complex printed wiring board (see A.7.2) inspection lot or lots that has passed all in-process and group A inspections during that production month (i.e., the group B reporting period). The most complex printed wiring boards shall be as determined by the manufacturer using its definition of complex (see A.7.2), subject to approval by the qualifying activity.

A.4.7.1.2 Sampling procedures. Sample units for each extent of qualification base material type family (see E.4.1.4) produced during that reporting period shall be subjected to group B inspection.

A.4.7.1.2.1 Sample unit selection. Except for the case of a 1 panel inspection lot, the sample units shall be selected from different panels. Unless otherwise specified in A.4.8.3.2 (resistance to solvents) or A.4.8.4.11 (surface peel strength), the following criteria shall be used in selecting samples for group B testing:

a. The sample units shall be from the most complex (see A.7.2) printed wiring board design produced that calendar month that allow for each test to be performed.

b. The sample units shall be randomly selected from panels which have passed group A inspection during that calendar month.

c. The sample units can be either:

(1) Two sets of quality conformance test circuitry, or

(2) Two test coupons for each test to be performed.

Eight foil lamination peel strength specimens shall be selected from two different production lots; four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is produced in a calendar month, then only the test coupons from that lot shall be submitted.

A.4.7.1.3 Frequency. The frequency of selecting sample units and performing group B testing shall be on a monthly basis. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

A.4.7.1.4 Failures. If one or more sample units fail to pass group B inspection, the sample shall be considered to have failed. The qualifying activity shall be notified of any group B failure within 3 business days. Group B inspection shall be repeated on additional sample units (either all group B inspections or just the group B inspection which the original sample failed, at the discretion of the qualifying activity) from the next most complex (see A.7.2) inspection lot from the same month that the failure occurred. Group A inspection and shipment of the product represented by the failed group B sample shall be discontinued.

A.4.7.1.4.1 Corrective actions. Corrective actions shall be taken on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, and equipment), and which are considered subject to the same failure.

A.4.7.1.4.2 Noncompliance. If the lot or lots directly represented by the group B failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group B sample are considered noncompliant until a sample from the next most complex (see A.7.2) inspection lot passes group B inspection.

A.4.7.1.4.3 Reinstitution of group A inspection. After successful completion of group B reinspection, group A inspection of product represented by the group B failure may be reinstituted.

A.4.7.1.5 Disposition of sample units. Sample units which have been subjected to group B shall be retained as specified in A.3.9.

TABLE A–VIII. Group B inspection.

Inspection	Requirement Paragraph	Method Paragraph	Test coupon by type 1/		Notes
			Types 1, 2 ,3, and 5	Type 4	
Subgroup 1					
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	2/	2/	2/
Rework simulation	A.3.7.4.8	A.4.8.4.8	3/	3/	3/
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1	E	E	
Dielectric withstanding voltage	A.3.7.5.3	A.4.8.5.3	E	E	4/
Subgroup 2					
Surface peel strength	A.3.7.4.11	A.4.8.4.11		P	5/

1/ See 1.2, 6.4.3, and A.3.1.1 herein.
2/ See A.4.8.3.2.1 for test specimen description and number of samples required.
3/ The holes to be tested and inspected shall represent component holes used for through–hole mounting. The test specimens shall be either test coupon "A" or holes from a production printed wiring board.
4/ Dielectric withstanding voltage shall be performed after the moisture and insulation resistance test on the same test coupon subjected to the moisture and insulation resistance test.
5/ Test coupon "P" is detailed in appendix H. See A.4.7.1.2.1 for the number of samples required.

A.4.7.2 Group C inspection. Group C inspection shall consist of the inspections specified in table A–IX for installation use A and B.

A.4.7.2.1 Inspection lot. The sample units (test coupons or production printed wiring boards) shall be randomly selected from the inspection lot that have passed all in-process and group A inspections during that reporting period.

A.4.7.2.2 Sampling procedures. Samples for each flexibility class (see 1.2.2) and each extent of qualification grouping based on the flexible base material type produced during that reporting period shall be subjected to group C inspection. If no printed wiring boards were produced during the reporting period, then group C inspection does not need to be performed.

Example: If both installation use A and B printed wiring boards were produced of adhesive flexible metal clad base material family and only class A printed wiring boards were produced using adhesiveless flexible metal clad base material family, then testing would be as follows:

a. Adhesive family: Both installation use A and use B verification tests (folding flexibility and flex endurance) would need to be performed.

b. Adhesiveless family: Only installation use A verification test (folding flexibility) would need to be performed.

A.4.7.2.2.1 Sample unit selection. Unless otherwise specified, the following criteria shall be used in selecting samples for group C testing:

a. The sample units shall be for each class of product produced during that reporting period. NOTE: If only use A printed wiring boards were produced during the reporting period, then only use A needs to be tested.

b. The sample units shall be randomly selected from panels which have passed in-process and group A inspection during that inspection period.

c. The sample units can be either:

(1) Two test coupons or sets of quality conformance test circuitry, or

(2) Two printed wiring boards for each test to be performed.

A.4.7.2.3 Frequency. The frequency of group C testing shall be every 24 months. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

TABLE A–IX. Group C inspection.

Inspection	Requirement paragraph	Method paragraph	Test specimen 1/
Subgroup 1	A.3.7.4.6	A.4.8.4.6	PWB or 2/
Flexibility endurance (use B)			
Folding flexibility (use A)	A.3.7.4.7	A.4.8.4.7	PWB or 3/
Subgroup 2			
Thermal shock	A.3.7.6.3	A.4.8.6.3	PWB or 3/

1/ See 1.2, 6.4.2, and A.3.1.1 herein.
2/ A suitable single–sided portion of a type 3, 4, or 5 production printed wiring board or the test specimen described in the applicable test method.
3/ A suitable portion of a production printed wiring board or the test coupon described in appendix H.

A.4.7.2.4 Noncompliance. If one or more sample units fail to pass group C inspection, the manufacturer shall notify the qualifying activity of such failure within 3 business days. The manufacturer shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, and equipment) and which are considered subject to the same failure. If the lot or lots directly represented by the group C failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group C sample are considered noncompliant until a sample passes group C inspection. Group A inspection and shipment of the product shall be discontinued until corrective action, acceptable to the qualifying activity, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections, or the inspection which the original sample failed, at the discretion of the qualifying activity). Group A inspection may be reinstituted; however, final acceptance and shipment shall be withheld until the group C inspection has shown that the corrective action was successful.

A.4.7.2.5 Disposition of sample units. Sample units which have been subjected to group C shall be retained as specified in A.3.9.

A.4.8 Methods of inspection. The following verification tests and test methods assure printed wiring board integrity within typical operating conditions and applications. Alternate methods are allowed with prior approval by the qualifying activity. The test methods described herein are the preferred methods and shall be the referee method in case of dispute when alternate test methods result in differing or conflicting results.

A.4.8.1 Visual and dimensional inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using either test method number 2.2.1 or 2.2.2 of IPC–TM–650, as applicable. Unless otherwise specified, the magnifications in table A–X shall be used for the conductor width or land diameter/width of features under inspection. Referee inspection needed to confirm a suspected defect of the specimen features shall be accomplished at a magnification of up to 40X, as applicable to confirm the suspected defect. Characteristics not observable through solder mask shall be evaluated prior to its application to the surface of the printed wiring board (see A.4.6.1). Verification of printed wiring board dimensional parameters using automated inspection technology (AOI and AXI) shall be acceptable.

TABLE A–X. Inspection magnification.

Conductor width or land diameter/width	Magnification 1/		IPC–OI–645 grade
	Standard inspection	Referee inspection	
Greater than .04 inches (1.0 mm)	1.75 x	4x	IV & V
From .02 to .04 inches (0.5 to 1.0 mm)	4x	10x	V & VI
From .001 to .02 inches (0.025 to 0.5 mm)	10x	20x	VI & VII
Less than .001 inches (0.025 mm)	20x	40x	VII & VIII

1/ Referee conditions are used to verify printed wiring boards rejected at the standard inspection magnification power. For printed wiring board designs with mixed conductor and land diameters and widths, the greater magnification power may be used for the inspection of the entire printed wiring board.

A.4.8.1.1 Annular ring, external (see A.3.5.2.5.1). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board. See figures F–4 and F–5 for illustration.

A.4.8.1.2 Overall printed wiring board thickness (see A.3.5.4). Unless otherwise specified, the overall printed wiring board thickness measurement shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.1.2.1 With edge-board contacts. Unless otherwise specified, printed wiring boards with edge-board contacts shall have the overall thickness measured from top to bottom of the printed wiring board on the final finish plated surfaces of opposite contacts.

A.4.8.1.2.2 Without edge-board contacts. Unless otherwise specified, printed wiring boards without edge-board contacts shall have the overall thickness measured across the board from plated copper surface to plated copper surface not including the final finish plating.

A.4.8.1.3 Registration, external (method I) (types 1 and 2) (see A.3.5.2.7). Registration of type 1 and type 2 printed wiring boards shall be satisfied if the outer layers meet the external annular ring (see A.3.1.1 and A.3.5.2.5) and hole pattern accuracy (see A.3.1.1 and A.3.5.4) requirements.

A.4.8.1.4 Solder mask thickness (see A.3.5.5.7). The measurement of the solder mask thickness shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.1.5 Product identification (marking and traceability). The printed wiring board specimen shall be inspected in accordance with test method number 2.1.8 of IPC–TM–650, except that the magnification shall be 1.75X (3 diopters), minimum.

A.4.8.1.6 Alternate plating and coating measurement techniques. When a conductor surface finish plating or coating thickness is less than .00005 inch (0.00125 mm), the verification of thickness shall be performed in accordance with one of the following test methods:

a. ASTM B567, measurement of thickness by the beta backscatter method.

b. ASTM B568, measurement of thickness by X-ray spectrometry.

A.4.8.1.7 Wire bond pad surface roughness. The printed wiring board specimen shall be inspected in accordance with test method number 2.4.15 of IPC–TM–650. Only the pristine area of the terminal shall be evaluated.

A.4.8.1.8 Hole size. The finished hole size and tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of hole size measurements needed for each hole size shall be determined by the manufacturer. The number of holes to be sampled for each hole size present on the printed wiring board shall be determined based on the number of holes within the population. The sampling plan used shall be documented by the manufacturer in its product assurance plan.

A.4.8.1.9 Materials inspection. Prior to any fabrication, materials inspection shall consist of certification supported by verification data, which verifies that the materials specified (see A.3.1.1) used in fabricating the printed wiring boards are in accordance with the applicable referenced specifications or requirements specified. Unless otherwise specified, verifying data does not need to be submitted to the qualifying activity or acquiring activity, but shall be made available upon request.

A.4.8.1.10 Workmanship. The printed wiring board specimen shall be inspected in accordance with test method number 2.1.8 of IPC–TM–650, except that the magnification shall be 1.75X (3 diopters), minimum.

A.4.8.2 Microsection inspection. Microsection inspections (to evaluate characteristics such as plated hole structures, plating thickness, or foil thickness) shall be accomplished by using the following preparation and inspection methods.

A.4.8.2.1 Microsection preparation. Microsection preparation shall be accomplished by using methods in accordance with either test method numbers 2.1.1 of IPC–TM–650. Automatic microsectioning techniques may be used in lieu of test methods 2.1.1 of IPC–TM–650. The following details shall apply:

a. Number of plated hole structures for each specimen. A minimum of three plated hole structures cross sectioned vertically shall be made for each printed wiring board test specimen required.

b. Accuracy.

(1) Through holes. All three plated hole structures of each printed wiring board test specimen shall be sectioned, ground, and polished to within ±10 percent of the center of the drilled diameter of the hole.

(2) Microvias. For non-copper filled microvias, at least three microvias of each printed wiring board test specimen shall the be sectioned, ground, and polished to within ±10 percent of their center. For copper filled microvias, the grinding and polishing accuracy shall be sufficient to evaluate contact dimension.

c. Pre–microetch evaluations. The three plated hole structures of the printed wiring board test specimens shall be evaluated for plating separations, superfluous copper, and wicking prior to microetching (see A.6.11).

d. When more than two printed wiring board test specimens are contained in a mount (coupon–stacking or gang mounting), the following shall apply:

(1) The printed wiring board test specimens shall not be in direct contact with any other printed wiring board test specimen in the mount. The recommended minimum distance between printed wiring board test specimens in a mount is .010 inch (0.25 mm).

(2) The traceability requirements of A.3.9.1 shall apply.

A.4.8.2.2 Microsection examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number 2.2.5 of IPC–TM–650 to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, and other characteristics, in plated holes. If more than three plated hole structures are on a printed wiring board test specimen cross section (as with test coupon "AB–R"), all plated hole structures of the same size shall be evaluated. Each side of the three plated hole structures shall be viewed independently. The following details shall apply:

a. Magnifications. The printed wiring board test specimens shall be inspected at the magnifications specified in test method number 2.2.5 of IPC–TM–650.

b. Evaluations. Pre– and post–microetch evaluations for the criteria of A.3.6 shall be accomplished at magnifications specified above. The printed wiring board test specimens shall be evaluated for plating separations, superfluous copper, and wicking both prior to and after microetching.

c. Measurements. Specified thickness measurements shall be averaged from at least three determinations for each side of each plated hole of each test specimen. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in A.3.6.4.4.

EXAMPLE: The copper plating thickness of the plated hole wall shall be determined from the average of three measurements, approximately equally spaced, taken on each side of the plated-through hole. Conductor thickness shall be determined by an average of three measurements on each layer and each side of the hole.

d. Final finish plating and coatings that are less than .00005 inch (0.00125 mm) in thickness shall not be measured using metallographic techniques. The plating and coating thickness shall be evaluated using the alternate measurement techniques of A.4.8.1.6.

A.4.8.2.3 Evaluation of plated hole features by DPA (see A.3.6). When external and internal features and structures of printed wiring board test specimens are inspected in accordance with A.4.8.2.2, the following details shall apply:

a. Dielectric layer thickness (see A.3.6.1.5). The dielectric layer thickness shall be inspected between all conductor layers present in the printed wiring board test specimen.

b. Thermal planes (see A.3.6.1.6). The lateral dielectric spacing between the heat sinking planes and adjacent conducting surfaces (nonfunctional lands) or plated-through holes shall be measured at the closest point between these surfaces or the plated-through hole.

c. Plating and coating thickness (see A.3.6.2.1.5 and A.3.6.4). Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured for compliance with the requirements of A.3.6.4.3.

d. Copper plating voids (see A.3.6.4.4). When a single plating void that is within the acceptable limits of A.3.6.4.4 is present in a microsection, the sampling procedures of A.4.6.2.2.e shall apply for group A verifications. Any plated hole structure in the microsection failing the plating void criteria specified in A.3.6.4.4 subparagraphs a, b or c, shall be cause for the entire panel of printed wiring boards associated with the microsection to be rejected. For group B inspections, see A.4.7.1.4.

e. Annular ring, internal (see A.3.6.2.4). This measurement shall apply to all internal lands for all plated hole structures in the cross section.

A.4.8.2.4 Registration (types 3 and 4). Layer-to-layer registration of multilayered printed wiring boards shall be determined by either evaluating microsectioned test coupons (method II, see A.4.8.2.4.1) or by evaluating of special registration coupons when provided (method III, see A.4.8.2.4.2).

A.4.8.2.4.1 By microsection (method II). Method II registration of printed wiring boards shall be satisfied if all layers meet the annular ring and hole pattern accuracy requirements specified (see A.3.1.1). Registration shall be evaluated using any combination of the non-stressed specimens (as received) (see A.3.7.2.1) and or the resistance to soldering heat (see A.3.7.6.2) microsectioned printed wiring board test specimens taken from diagonal corners of the panel. Both printed wiring board test specimens shall have been microsectioned in the vertical plane with one printed wiring board test specimen representing the panel's length (X) direction and the other representing the panel's width (Y) direction.

A.4.8.2.4.2 By registration test coupons (method III) (optional). Registration test coupons and techniques, when provided by the printed wiring board fabricator, shall be evaluated in accordance with methods approved by the qualifying activity and when applicable, the acquiring activity. Unapproved methods of measurement using registration test coupons shall be backed up by method II of A.4.8.2.4.1 using the appropriate test coupons (see table A–VIII) from the same panel.

A.4.8.3 Chemical inspection.

A.4.8.3.1 Ionic contamination (by resistivity of solvent extract) (see A.3.7.3.1 and A.6.4). The printed wiring board shall be inspected for ionic contamination in accordance with test method number 2.3.25 of IPC–TM–650.

A.4.8.3.2 Resistance to solvents (marking ink or paint) (see A.3.7.3.2). Marking ink or paint resistance to solvents shall be inspected in accordance with test method number 2.3.4 of IPC–TM–650. The following details apply:

a. The marked portion of the printed wiring board test specimen shall be brushed.

b. After the test, the printed wiring board test specimen shall be visually inspected in accordance with A.4.8.1 for legibility of marking.

A.4.8.3.2.1 Sampling procedures and test specimens. The resistance to solvents test shall be performed either during group A (every lot) or during group B (monthly). The minimum number of sample units tested shall be at least one sample unit for each solution specified by the applicable test method (i.e., one sample unit for each solution required). The printed wiring board test specimen shall be as described in appendix H.

A.4.8.4 Physical inspections.

A.4.8.4.1 Adhesion, cover material (see A.3.7.4.1). The adhesion and permanency of cured cover materials on printed wiring board test specimens shall be determined in accordance with test method number 2.4.28.1 of IPC–TM–650, with the following details and exceptions. The printed wiring board test specimen shall be as described in appendix H when samples are taken from production panels or table A–VI when taken from qualification test specimens.

A.4.8.4.2 Adhesion, legend and marking (see A.3.7.4.2). The printed wiring board test specimen shall be inspected in accordance with test method number 2.4.1.1 of IPC–TM–650. The printed wiring board test specimen shall be as described in appendix H.

A.4.8.4.3 Adhesion, plating (see A.3.7.4.3). The printed wiring board test specimen shall be inspected in accordance with test method number 2.4.1 of IPC–TM–650, with the following details and exceptions. When edge board contacts are part of the conductor pattern, at least one pull shall be on the contacts. Fresh tape shall be used for each pull. If overhang metal (slivers) breaks off and adheres to the tape, it is evidence of outgrowth, but not a plating adhesion failure.

A.4.8.4.4 Adhesion, solder mask (see A.3.7.4.4). The printed wiring board test specimen shall be inspected for permanency and adhesion of cured solder mask in accordance with test method number 2.4.28.1 of IPC–TM–650.

A.4.8.4.5 Bow and twist (see A.3.7.4.5). The printed wiring board test specimen shall be inspected for bow and twist in accordance with test method number 2.4.22 of IPC–TM–650.

A.4.8.4.6 Flexibility endurance (see A.3.7.4.6). The printed wiring board test specimen shall be inspected for flexibility endurance in accordance with test method number 2.4.3 of IPC–TM–650 with the following exceptions:

a. The number of test specimens to test shall be as required by A.4.7.2.2.1.

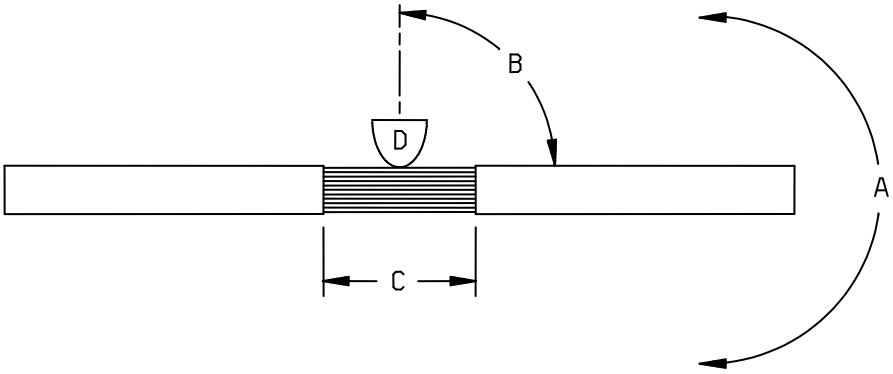
b. The test specimen shall be subjected to a minimum of 100,000 cycles.

The flexibility endurance test may also be performed using an alternate test-to-failure method specified in A.6.6.1.

A.4.8.4.6.1 Test specimens. The printed wiring board test specimens shall be as described in appendix H.

A.4.8.4.7 Folding flexibility (see A.3.7.4.7). The folding flexibility test shall be performed by subjecting the printed wiring board test specimen to fold cycles as described below and as depicted on figure A–1. The specified number of fold cycles shall be performed with the mandrel placed in contact with the printed wiring board test specimen on one side and then again with the mandrel placed in contact with the printed wiring board test specimen on the opposite side. After completion of the specified number of fold cycles, both directions, the printed wiring board test specimen shall be tested for electrical defects in accordance with A.3.7.5.1.

A.4.8.4.7.1 Test specimens. The printed wiring board test specimen shall be as described in appendix H.



NOTES:
a. Direction of bend (detail A).
b. Degree of bend (detail B).
c. Points of application (detail C).
d. Diameter of mandrel (detail D).

FIGURE A–1. Folding flexibility.

A.4.8.4.8 Rework simulation.

A.4.8.4.8.1 Unsupported hole (see A.3.7.4.8.1). The printed wiring board test specimen shall be inspected in accordance with test method number 2.4.21 of IPC–TM–650 with the following details and exceptions. Three holes for each printed wiring board test specimen shall be tested. Insert wires in holes in selected lands and solder to lands by machine or hand, as applicable. The insert wire lead shall have a diameter so that the diameter of the hole will be at a maximum of .020 inch (0.51 mm) greater than the diameter of the inserted wire lead. The wires shall not be clinched. It shall be considered a failure when a land around an unsupported hole is loosened.

A.4.8.4.8.2 Plated-through hole (see A.3.7.4.8.2). Rework simulation of plated-through holes shall be tested in accordance with test method number 2.4.36 of IPC–TM–650. The following details shall apply:

a. Unless otherwise specified, method A shall be used initially.

b. For designs with an overall printed wiring board thickness greater than .120 inch (3.0 mm), one row of plated-through holes shall be used to assure that the pre-designated method to be used for the soldering and de–soldering operation will produce satisfactory solder connections for the printed wiring board test specimen design being tested. A satisfactory solder connection is when the wire is wetted through the entire plated hole within the soldering time limit specified in the test method. An unsatisfactory solder connection is when an insufficient solder connection is produced or the soldering time exceeds the limit specified in the test method.

c. In case of an unsatisfactory solder connection, another plated-through hole on the row shall be soldered using the soldering temperature of the next higher method (for example, method B if method A is insufficient, or method C if method B does not suffice) until a satisfactory solder connection is made. If the temperatures of method C still yields unsatisfactory solder connections, consult the qualifying activity for additional guidance before proceeding further with the testing.

d. Once a method that produces satisfactory solder connections has been determined, the soldering and de-soldering operation shall proceed using a different row of plated-through holes which will be evaluated to the acceptance criteria of A.3.7.4.8 herein. The final test method used shall be noted in the test report.

A.4.8.4.9 Solderability (see A.3.7.4.9). Unless otherwise specified (see A.3.1.1), the tests that used Sn-Pb solders (A, B, C, or D) of J–STD–003 shall be used. The default category of coating durability of J–STD–003 is category 2. When specified (see A.3.1.1), accelerated conditioning for coating durability shall be in accordance with J–STD–003. For printed wiring boards using only surface mount components, the surface solderability test can be used in lieu of the hole solderability test. For mixed component designs (both surface mount and through hole attachment), unless otherwise specified, only the hole solderability test shall be performed.

A.4.8.4.9.1 Hole (plated-through hole) (see A.3.7.4.9.1). The printed wiring board test specimens shall be inspected in accordance with J–STD–003 or the solderability test methods test described in appendix G of MIL–PRF–31032.

A.4.8.4.9.2 Surface or surface mount land (see A.3.7.4.9.2). The printed wiring board test specimens shall be inspected in accordance with J–STD–003 or the solderability test methods described in appendix G of MIL–PRF–31032.

A.4.8.4.10 Solder mask cure (see A.3.7.4.10). The printed wiring board test specimens shall be inspected for cured of solder mask in accordance A.4.8.1.

A.4.8.4.11 Surface peel strength (types 3 and 4 using foil lamination) (see A.3.7.4.11). The printed wiring board test specimen shall be tested and inspected in accordance condition A of test method number 2.4.8 of IPC–TM–650. Conditions B and C (after resistance to soldering heat and after exposure to processing chemicals) shall not be performed. All surface finish plating or coatings (for example, plated tin-lead, solder coating, ENIG, OSP, and others) shall be chemically removed prior to test or shall be prevented from being deposited during manufacturing. The printed wiring board test specimen shall not be coated with any organic coating for test. No individual value in the calculation of the average peel strength shall be less than 1.5 pounds (0.68 Kg) of the specified minimum value for each inch (0.26 N/mm) of width.

A.4.8.4.11.1 Test specimens. The printed wiring board test specimen shall be as described in appendix H.

A.4.8.5 Electrical inspection.

A.4.8.5.1 Continuity and circuit shorts.

A.4.8.5.1.1 Production screening. Printed wiring boards shall be electrically tested using either automatic or manual equipment capable of verifying the test level C requirements of IPC–9252 for 100 percent continuity and isolation.

A.4.8.5.1.2 Qualification and referee testing.

A.4.8.5.1.2.1 Circuit continuity (see A.3.7.5.1.1). A current shall be passed through each net by applying electrodes on the terminals at each end of the net. The current passed through the net shall not exceed those specified in the applicable design standard (see A.3.1.1 and appendix D) for the smallest conductor in the circuit. For manual testing during qualification, the current shall be 1.0 amp minimum and shall be applied for a minimum of 5 seconds.

A.4.8.5.1.2.2 Circuit shorts (isolation resistance) (see A.3.7.5.1.2). A test voltage shall be applied between each net and all other nets that are adjacent to the net under test. The voltage shall be applied between nets of each layer and the electrically isolated net of each adjacent layer. For manual testing the voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be as specified on the applicable master drawing. If a test voltage of the printed wiring board is not specified on the applicable master drawing, the test voltage shall be the maximum rated voltage of the net being tested. If no maximum rated voltage is specified, or it is less than 40 volts, then the minimum test voltage shall be 40 volts minimum.

A.4.8.5.2 Circuit or plated-through hole short to metal core substrate (see A.3.7.5.2). A polarizing voltage of 500 volts shall be applied between conductors and or lands and the metal core substrate in a manner such that each conductor and or land is tested to the conditions of A.4.8.5.1.2.2.

A.4.8.5.3 Dielectric withstanding voltage (see A.3.7.5.3). The printed wiring board test specimen shall be tested in accordance with test condition B of test method number 2.5.7 of IPC–TM–650. The following details and exceptions apply:

a. Test specimen: The printed wiring board test specimen shall be as identified in table A–VIII.

b. Magnitude of test voltage: Condition B (1,000 V dc +25 V dc, –0 V dc).

c. Duration of application of test voltage: 30 seconds +3, –0 seconds.

d. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.8.5.4 Impedance testing (see A.3.7.5.4). Impedance testing shall address the parameters required by the level C requirements of IPC–9252.

A.4.8.6 Environmental inspection.

A.4.8.6.1 Moisture and insulation resistance (see A.3.7.6.1). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3 of IPC–TM–650, class 3, using test specimen preparation method A. The initial and final resistance measurements shall be taken at 500 V dc, +25 V dc, –0 V dc).

A.4.8.6.2 Resistance to soldering heat.

A.4.8.6.2.1 Solder float thermal stress (single side, single cycle, component holes) (see A.3.7.6.2). The printed wiring board test specimen shall be inspected for solder float thermal stress in accordance with appendix F of MIL–PRF–31032. The following details shall apply. Printed wiring board test specimens constructed of adhesiveless metal-clad flexible base materials shall be subjected to test condition A. Printed wiring board test specimens constructed of adhesive flexible metal-clad base materials shall be subjected to test condition B. Printed wiring board test specimens constructed of both adhesive and adhesiveless metal-clad flexible base materials shall be subjected to test condition B.

A.4.8.6.3 Thermal shock (see A.3.7.6.3). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.7.2 of IPC–TM–650, test condition D.

A.5 PACKAGING

A.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see A.6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

A.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. This appendix is intended to be used by manufacturers certified to the QML printed board specification, MIL–PRF–31032 to supply product to legacy drawings.

A.6.2 Acquisition requirements.

A.6.2.1 Primary acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. Packaging requirements (see A.5.1).

c. Appropriate printed wiring board type (see 1.2.1), installation use (see 1.2.2), and rework capability grade (see 1.2.3).

d. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see A.3.1.1).

e. Title, number, revision letter (with any notice number when applicable), and date of the applicable design standard (see A.3.3).

f. Part identification (if applicable), and marking instructions including size, location, and application method (see A.3.1.1 and A.3.8).

g. Whether microsectioned printed wiring board test specimens, sample units or photographs are required to be delivered with the order.

A.6.2.2 Additional acquisition requirements. Acquisition documents should also specify the following data, if applicable:

a. Verification Conformance Inspection option (if other than option 4) (see appendix D).

b. Design related, if different than the applicable design standard (see appendix D).

(1) Minimum annular ring (external or internal) (see A.3.1.1), if different than the applicable design standard.

(2) Minimum conductor width (see A.3.1.1), if different than the applicable design standard.

(3) Minimum conductor spacing (see A.3.1.1), if different than the applicable design standard.

(4) Minimum dielectric thickness (see A.3.1.1), if different than the applicable design standard.

(5) Minimum edge spacing requirement (see A.3.1.1), if different than the applicable design standard.

(6) Copper plating thickness (see A.3.1.1), if different than the applicable design standard.

(7) Conductor finish plating (see A.3.1.1), if other than solder coating or tin-lead.

c. Level of ionic contamination (see A.3.7.3.1).

d. Electrical test requirements (see A.3.7.5.1 and A.3.7.5.4).

e. Surface peel strength (foil lamination), if applicable (see A.3.7.4.11).

f. Non-delivery of sample units which have not been subjected to electrical testing (continuity and circuit shorts tests) and have passed all other tests to groups A and B inspection.

g. Contamination (organic) (see A.3.7.3.1 and A.6.4).

h. If special, or other identification, marking is required (see A.3.8).

A.6.3 Qualification.

A.6.3.1 Transference of qualification. Manufacturers currently qualified to MIL–P–50884D will have their qualification transferred to this document. Qualifications in process (before the date of this document) will be performed to the specification revision and amendment listed on the approved DLA Land and Maritime Form 19W. New applications for qualification (after the date of this document) will be performed to the requirements of this revision.

A.6.3.2 Qualification expiration and Qualified Products Database (QPD) 50884. Qualification listings within QPD–50884 for manufacturers qualified under past revisions of this document includes the qualification expiration date as the last six digits of the test reference number. This date, formatted as (month/day/year), was used to represent the qualification expiration date for that listing. In past revisions of this document, that date was used to signify that the company is no longer qualified whether or not that individual listing has been removed the QPD. That date is not applicable to this issue.

A.6.4 Ionic contamination testing (surface cleanliness). The values of ionic contamination specified in this document were established in the late 1970's by the U.S. Navy with the issuance of the Naval Air Center Materials Research Report No. 3–78. The values used in the report were eventually used in the canceled specification MIL–P–28809 as a baseline needed for completed assemblies. The chemistries of the fluxes and cleaning solutions used in the 1970's were very different than what is used currently. The levels of ionic contamination needed for today's circuit card assemblies may be well below that threshold established in Naval Air Center Materials Research Report No. 3–78 or allowed by this specification.

A.6.4.1 Flux removal. Selection of procedures for flux removal is at the manufacturer's discretion. A procedure should be chosen which will enable the printed wiring board fabricator to produce results enabling compliance with this document. Both polar and nonpolar solvents may be required to effect adequate flux removal.

A.6.4.2 Alternate methods and equipment. The following methods of determining the cleanliness of printed wiring boards have been shown to be equivalent to the sodium chloride equivalent ionic contamination test method:

a. The Kenco Alloy and Chemical Company, Incorporated, "Omega Meter™, Model 200" (see http://www.scscoatings.com).

b. Alpha Metals Incorporated, "Ionograph™" (see http://www.scscoatings.com).

c. Zero Systems, Incorporated, "Zero Ion™, Model ZI–100."

d. Westek, "ICOM 5000™."

Table A–XII list the equivalence factors for these methods in terms of micrograms equivalents of sodium chloride for each unit area.

TABLE A–XI. Equivalence factors.

Method	Equivalence factors	Equivalents of sodium chloride		Related IPC–TM–650 test method
		Micrograms per square inch	Micrograms per square cm	
Resistivity of solvent extract	1.00	10.06	1.56	2.3.25
Omega Meter™	1.39	14.00	2.20	2.3.25
Ionograph™	2.01	20.00	3.10	2.3.25
Zero Ion™	3.68	37.00	5.80	N/A
ICOM 5000™	2.20	22.00	3.40	N/A

A.6.5 Certified suitable laboratories (acceptable to the Government). Government accepted test laboratories are those facilities that have demonstrated their ability to perform the verification test required by this document. Levels of acceptance include group A, group B, group C, and qualification testing.

A.6.6 Alternate test methods (see C.5.2.2). Other test methods may be substituted for those specified herein provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this appendix.

A.6.6.1 Flexibility endurance (see A.4.8.4.6). The flexibility endurance test may be performed using the alternate test procedure detailed in test method number 2.4.3.1 of IPC–TM–650. The mandrel size for printed wiring board types 1 and 2 shall be 12 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel shall not be less than .125 inch (3.18 mm). The number of cycles until failure shall be reported.

A.6.7 Group B sample critical design details. Past versions of this document contained default design details that were assumed to apply to all test coupons subjected to group B inspection, regardless of the master drawing design requirements. With the issuance of revision D of this document, the design details which were universally used to determine acceptance or failure of the group B samples, are no longer considered universally applicable to the group B test coupons. The printed wiring board design details (plating thickness, dielectric separation, external annular ring, internal annular ring, and other design criteria) or the default design standard that applies to the test coupons, should be submitted along with test coupons so that a proper group B evaluation of the design can be completed.

EXAMPLE: The master drawing of the most complex design selected for group B testing requires .003 inch (0.08 mm) of copper plating thickness, .006 inch (0.15 mm) of dielectric spacing, and .005 inch (0.13 mm) internal annular ring. These design details are considerably different than the baseline design parameters found in either IPC–2223 or IPC–2221. If on these same samples, the group B test laboratory found that the samples exhibited .002 inch (0.05 mm) of copper plating thickness, .005 inch (0.13 mm) of dielectric spacing and .004 inch (0.10 mm) internal annular ring, the test laboratory could not claim, state, or certify that the results of group B testing or the samples met the specification requirement.

A.6.8 Tin finishes (see A.3.4.1). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Tin whisker growth could adversely affect the operation of electronic equipment systems. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM B545.

A.6.9 DLA Land and Maritime Form 19W. Copies of DLA Land and Maritime Form 19W, "PWB–QPL Application/Authorization to Test" may be obtained at URL http://www.landandmaritime.dla.mil/Offices/Sourcing_and_Qualification/ or upon application to DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43216–5000.

A.6.10 Alternate microsection preparation procedure guidelines. IPC–MS–810 "Guidelines for High Volume Microsection" contains many recommendations and suggestions that can be helpful in preparing microsection mounts containing multiple printed wiring board test specimens.

A.6.11 Microsection mount microetch caution. Prior to microetching, if lines are visible in the areas of inner layer to hole wall interfaces, care should be taken to not over-etch the mount so that the various plating layers will still be visible in the etched mount. This will enable accurate determination as to whether the line is separation or a polishing artifact.

A.6.12 Blind, buried, and through vias. This specification includes provisions for verifying the performance of rigid printed wiring boards containing blind vias, buried vias, controlled depth drilled vias, laser drilled vias, low aspect ratio blind vias, microvias, semi-blind vias, semi-buried vias, and through vias.

A.6.13 Stiffener adhesion test and requirement. This document does not include the stiffener adhesion test or requirement contained in MIL–P–50884C. All stiffeners are viewed as a mechanical support and total bonding of the stiffener to the printed wiring board is not required for compliance with this document.

A.6.14 Referenced IPC–TM–650 test methods. The following test method numbers are referenced in this document:

2.1.1 – Microsectioning.
2.1.8 – Workmanship.
2.2.1 – Mechanical Dimensional Verification.
2.2.2 – Optical Dimensional Verification.
2.2.5 – Dimensional Inspections Using Mircosections.
2.3.4 – Chemical Resistance, Marking Paints and Inks.
2.3.25 – Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract.
2.4.1 – Adhesion, Tape Testing.
2.4.1.1 – Adhesion, Marking Paints and Inks.
2.4.3 – Flexural Fatigue, Flexible Printed Wiring Materials.
2.4.3.1 – Flexural Fatigue and Ductility, Flexible Printed Wiring.
2.4.8 – Peel Strength of Metallic Clad Laminates.
2.4.15 – Surface Finish, Metal Foil.
2.4.21 – Land Bond Strength, Unsupported Component Hole.
2.4.22 – Bow and Twist (Percentage).
2.4.28.1 – Adhesion, Solder Resist (Mask), Tape Test Method.
2.4.36 – Rework Simulation, Plated-Through Holes for Leaded Components.
2.5.7 – Dielectric Withstanding Voltage, PWB.
2.6.3 – Moisture and Insulation Resistance, Printed Boards.
2.6.7.2 – Thermal Shock, Continuity and Microsection, Printed Board.

A.7 DEFINITIONS

A.7.1 Base material types. Qualification of a particular flexible base material types will be extended to cover all flexible base material types of that same family.

a. Adhesiveless family includes all base materials that use other techniques to hold the basis metal to one or both sides of the dielectric.

b. Adhesive family include all base materials that rely/use an adhesive to hold the metal to both sides of the dielectric. Note "cast" materials are considered adhesiveless.

A.7.2 Complex (as related to group B testing). Complexity of printed wiring boards will usually depend on the base materials used; dielectric layer thickness; overall printed wiring board thickness; number of conductor layers; conductor widths and spacings; intricacy of patterns; size, quantity, aspect ratio and positioning of plated holes; tolerancing of any or all of the above; the presence of internal thermal planes or heat sinks, and all combinations of the above with respect to their manufacturing difficulty, and their effects upon the consistent ability of the printed wiring boards to meet the requirements of the periodic testing, unless otherwise specified by the contracting activity.

A.7.3 Conductive interfaces. The term conductive interfaces is used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of metal foil. The interface between platings and coating (electroless copper, direct metallization copper, vapor deposited copper, non-electroless electroless copper substitutes, and electrolytic copper, whether panel or pattern plated), are also considered a conductive interface.

A.7.3.1 External conductive interfaces. An external conductive interface is considered to be the junction between the surface copper foil and the deposited or plated copper.

A.7.3.2 Internal conductive interfaces. An internal conductive interface is considered to be the junction between the internal layers (copper foil posts or internal layers) and the deposited or plated copper.

A.7.4 Contract services. Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include verification testing including electrical function tests.

A.7.4.1 Mass lamination. Manufacturers requesting to use contract services lamination (mass lamination) are required to be qualified to type 4 of the same base material type requested. The qualification test specimens and sample sizes should be specified in the qualification test plan.

A.7.5 Cover material. Cover materials are thin dielectric materials used to encapsulate circuitry.

A.7.5.1 Covercoat. Covercoats are materials that are deposited as a liquid onto the circuitry that subsequently becomes a permanent dielectric coating.

A.7.5.2 Coverfilm. Coverfilms consist of one of the following:

a. A homogeneous single component.

b. Separate layers of generically similar chemistries.

c. A composite blend of constituents.

A.7.5.3 Coverlay. Coverlay are film and adhesive made from separate layers of generically different chemistries.

A.7.6 Inspection panel. A production panel which includes a sufficient quantity of quality-conformance test circuitry necessary to complete all qualification inspections or group A and group B verifications, as applicable. Inspection panels may have been wholly or partially processed as a larger production panel. Separation of a production panel into multiple inspection panels is acceptable if each of the smaller sub-panels contain a sufficient quantity of quality-conformance test circuitry necessary to complete all qualification inspections or group A and group B verifications, as applicable. In order for printed wiring boards to be potential compliant printed wiring boards, they would have been fabricated on inspection panels.

A.7.7 Printed wiring board test specimen. The term 'printed wiring board test specimen' is used to describe all of the following; production printed wiring boards, portions of production printed wiring boards, qualification test specimens, or test coupons.

A.7.8 Procedure. A particular way of accomplishing an objective; generally refers to the method rather than the result. Procedures are usually developed to describe the methods for implementing policy.

A.7.9 Resin systems families.

A.7.9.1 Thermosetting resin. For the purposes of this document, the following base material types are classified as containing thermosetting resins: AF, BF, BI, GB, GC, GF, GH, GI, GM, QI, and SC.

A.7.9.2 Thermoplastic resin. For the purposes of this document, the following base material types are classified as containing thermoplastic resin: GR, GP, GT, GX, and GY.

A.7.10 Printed wiring board thickness. The overall printed wiring board thickness includes metallic depositions, fusing, and solder mask. The overall thickness is measured across the printed wiring board extremities (thickest part), unless a critical area, such an edge card connector or card guide mounting location, is identified on the master drawing.

A.7.11 Quality conformance test circuitry (QCTC). See IPC–T–50.

A.7.12 Non-stressed specimens (as-received condition) microsection. Non-stressed specimens means after tin-lead is reflowed or fused or after solder coating but prior to solder float thermal stress, rework simulation, thermal shock or bond strength testing.

A.7.13 Fold cycle. A fold cycle can be defined as either of the following:

a. A fold cycle is defined as taking one end of the specimen and folding it around a mandrel and then unfold back to the original starting position, traveling 180 degrees in one direction and 180 degrees in the opposite direction.

b. A fold cycle may also be defined as folding (using opposite ends) the ends toward each other (fold the same direction) and then unfold back to the original starting position, with each end traveling 90 degrees in one direction and 90 degrees in the opposite direction.

A.7.14 Soda strawing (solder mask). A long tubular-like void along the edges of conductive patterns where the solder mask is not bonded to the base material surface or the edge of the conductor. Tin-lead fusing fluxes, fusing oils, solder fluxes, cleaning agents or volatile materials may be trapped in the soda straw void.

A.7.15 Traceability code. The manufacturer defined traceability code is used to ensure traceability between the printed wiring boards and the quality conformance test circuitry that represent them for manufacturing history.

A.7.16 Qualified Products Database Supplemental Information Sheet (QPDSIS). The DLA Land and Maritime–VQ QPDSIS is an electronic file that is available from the DLA Land and Maritime–VQ web site to provide users and customers with additional qualification details and serve as a support document to the official online QPD. The QPDSIS can be viewed or downloaded at URL:
http://www.landandmaritime.dla.mil/Programs/QmlQpl/QPLdetail.aspx?qpl=50884.

A.7.17 Supporting data. Data or information to provide backup and depth to required inspections or verifications.

A.7.18 First piece produced design inspection (first article). The analysis of the first item manufactured in a production run to verify correct setup and process alignment.

A.7.19 Referee testing. The re-inspection or testing of a printed board attribute for the purpose of resolving an acceptance issue at the request of the acquiring activity, manufacturer, or the qualifying activity.

A.7.20 Plated hole structure. Plated hole structures include all of the following: blind vias, buried vias, low aspect ratio blind vias, microvias, plated-through holes, and through vias.

A.7.21 Screenable defect. A screenable defect is one for which an effective, nondestructive screening test or inspection can be reasonably developed and applied to eliminate with confidence the nonconforming items from the lot.

PRODUCT ASSURANCE (PERFORMANCE AND VERIFICATION) REQUIREMENTS FOR QUALIFIED MANUFACTURER LIST LEVEL

B.1 SCOPE

B.1.1 Scope. This appendix contains optional requirements concerning the QML product assurance level for printed wiring boards covered by this specification. This appendix is a mandatory part of this specification when the product assurance requirements of appendix A are not used. The information contained herein is intended for compliance when the product assurance requirements of appendix A are not used.

B.2 APPLICABLE DOCUMENTS

B.2.1 General. The documents listed in this section are specified in sections B.3 and B.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections B.3 and B.4 of this specification, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

B.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS

B.3.1 Performance requirements. The performance requirements of the applicable MIL–PRF–31032 specification sheet shall apply to all printed wiring boards procured to the QML product assurance level.

B.3.2 Accept/reject criteria. The accept/reject criteria of the applicable MIL–PRF–31032 specification sheet shall apply to all printed wiring boards procured to the QML product assurance level.

B.3.3 QML brand. At the option of the manufacturer, the QML brand specified in MIL–PRF–31032 may be placed on printed wiring boards that comply with the product assurance requirements of this appendix.

B.4 VERIFICATION

B.4.1 Qualification inspection. Manufacturers shall be qualified for listing on QPD–31032 for the technology and capabilities required to produce printed boards under this appendix.

B.4.2 QML product assurance. The product assurance requirements for the QML level of printed wiring board furnished under this specification shall be satisfied by certification to MIL–PRF–31032. All printed wiring boards manufactured and delivered in compliance with this appendix shall be produced in accordance with the approved quality management plan.

B.4.3 Printed wiring board performance verification. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and test coupons specified in the applicable MIL–PRF–31032 specification sheet. The following details are applicable to the QML product assurance level:

a. Lot conformance inspection (LCI) product acceptance testing shall be based on the applicable verification flows (in-process and group A) offered by this document (see A.4.4 and appendix D) or the routine from a similar technology described by a MIL–PRF–31032 specification sheet. The various verification flows shall be based upon the design standard used to design the printed wiring boards and the available panel test coupons for the printed wiring boards.

b. MIL–PRF–31032 periodic conformance inspection (PCI) program can be used in lieu of groups B and C inspection of this document.

c. Test optimization is applicable to this appendix and can be applied to any verification flow detailed in this document.

B.5 PACKAGING

B.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

B.6 NOTES

B.6.1 Intended use. This appendix is intended to be used by manufacturers certified to MIL–PRF–31032 and qualified to MIL–PRF–31032/3 or MIL–PRF–31032/4 to reduce the complexity of maintaining multiple product/process and testing flows (both MIL–P–50884, MIL–PRF–50884, or MIL–PRF–31032) within a the manufacturing and testing facility.

B.6.2 Application of the QML product assurance level to existing requirements.

B.6.2.1 Use of existing master drawings. The QML printed wiring board manufacturer can use pre-existing master drawing without any modifications.

B.6.2.2 Form, fit, and function. The form, fit, and function of the printed wiring boards, whether the QML product assurance level or the QPL/QML product assurance level is used, will be the same.

B.6.2.3 Certification of conformance. The printed wiring boards can be certified as being compliant to appendix B of this document (MIL–PRF–50884).

B.6.3 Benefits of the QML product assurance level. Printed wiring boards produced by QML manufacturers using the provisions of this appendix in lieu of previous revisions would be compliant to this document (MIL–P–50884) when using the QML product assurance level with the added benefits as follows:

a. The QML manufacturer can use pre-existing master drawing without any modifications needed.

b. The printed wiring boards, whether the QML option or the QPL option is used, will be the same.

c. The level of quality will be the same or higher than the QPL product assurance level.

d. When using the correct verification test (for the design), the cost should be the same or less due to enhancements made to accept/reject criteria.

e. Customers will be more confident that a QML manufacturer has demonstrated the capabilities to build its design dues to its QML certification and qualification rather the generic standardized qualification test vehicle of the QPL quality assurance level portion of previous revisions of this document.

B.6.4 Retention of qualification. The manufacturer need only to keep the qualifying activity apprised of its total QML program, i.e., MIL–PRF–31032 QML and this document's QML product assurance level. This means that the manufacturer does not have to maintain two separate compliance programs, (i.e., no need for a QPL compliance program for this document and a QML program for MIL–PRF–31032).

B.6.5 Certification of conformance and acquisition traceability. The manufacturer can certify QML printed wiring boards processed under their MIL–PRF–31032 QML program as compliant to this document. The certificate of compliance should reference the QML product assurance level to differentiate the compliant product from printed wiring boards verified using the QPL product assurance level offered in this document.

B.6.6 Past specification revisions (see appendix D for more details). Printed wiring boards procured to this document meets and exceeds all quality and reliability requirements of previous revisions of MIL–P–50884.

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C = 0 (ZERO DEFECT) SAMPLING, TEST EQUIPMENT, AND SUITABILITY OF INSPECTION FACILITIES

C.1 SCOPE

C.1.1 Scope. This appendix details the statistical sampling procedures to be used with the QPL product assurance level of this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, and C.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections C.3, C.4, and C.5 of this specification, whether or not they are listed.

C.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM E29 – Standard Practice for Using Significant Digits in Test Data to Determine Conformance with Specifications.

(Copies of these documents are available online at http://www.astm.org.)

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–QL–653 – Certification of Facilities That Inspect/Test Printed Boards Components and Materials.

(Copies of these documents are available online at http://www.ipc.org.)

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO 17025 – General Requirements for the Competence of Testing and Calibration Laboratories.

(Copies of these documents are available online at http://www.iso.org.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540.3 – Requirements for the Calibration of Measuring and Test Equipment.

(Copies of these documents are available online at http://www.ncsli.org.)

C.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 DEFINITIONS AND SYMBOLS

C.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. C = 0 sample plan: The C = 0 sample plans are defined as a combination of a test specimen usage identifier (see C.3.1.b) and a sample size series (see C.3.1.c). The resulting C = 0 sample plan will be a two character designator combination that identifies the sample size series that is to be with a type of test specimen for a particular verification (see C.4.5).

b. Test specimen usage identifier (see C.4.5 for examples): The following usage modifiers are used to differentiate when a particular plan is to be used for a particular test specimen:

(1) The letter "B" will be used to signify that production printed wiring boards are to be sampled.

(2) The letter "T" will be used to signify that test coupons are to be sampled based on the number of panels in the lot.

(3) An asterisk "*" will be used for either printed wiring boards or test coupons.

c. Sample size series: The sample size series is defined as the following series of letters: A, D, F, H, J, L, and N that are listed in table C–I (see C.4.5 for examples).

d. Tightened inspection: Tightened inspection is defined as inspection performed using the next sample size value in the sample size series lower than that specified.

e. Acceptance number (C): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

f. Rejection number (R): Rejection number is defined as one plus the acceptance number.

C.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. C: Acceptance number.

b. R: Rejection number.

C.4 STATISTICAL SAMPLING PROCEDURES AND SAMPLE PLAN TABLE

C.4.1 General. Statistical sampling shall be conducted using the C = 0 method. The C = 0 method as specified herein is a sampling plan that provides a high degree of assurance that a lot having a proportion defective greater than the specified acceptance number (C = 0) will not be accepted. For all situations, the acceptance number (C) shall be equal to 0 (C = 0) and the rejection number (R) shall be 1 or greater (R ≥ 1).

C.4.2 Acceptance and procedure.

C.4.2.1 Acceptance number (C = 0). Acceptance of inspection lots shall be based on an acceptance number of zero (C = 0).

C.4.2.2 Rejection number (R ≥ 1). Failure of a sample unit for one or more tests of a subgroup shall be charged as a single failure. One or more sample rejects shall be cause for failure of the lot or sublot, as applicable. Any failure on any of the sample units shall constitute a failure of the entire inspection lot or sublot.

C.4.3 Tightened inspection (for reevaluation purposes). Tightened inspection shall be performed by sampling using double the sample size as specified in table C–I with zero failures allowed or 100 percent.

C.4.4 Sample size. The sample size for each subgroup shall be determined from table C–I. If lot size is smaller than sample size, test all of the units. The manufacturer may, at their option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number.

C.4.5 C = 0 sample plan construction (selection and usage of the sample size series). The sample size series of table C–I to be used will be directed from the appropriate inspection table. The inspection table will specify the C = 0 sample plan (test specimen identifier and sample size series) or plans (test printed wiring board, test coupons, or either one) to use.

EXAMPLES: If an inspection table specified that "Plan BF or TL" be used when verifying test specimens, it is specifying that sample size series "F" of table C–I shall be used for selecting printed wiring boards and sample size series "L" shall be used for selecting test coupons. If the same inspection table specified that "Plan *H" be used (the asterisk "*" representing both printed wiring boards and test coupons), then sample size series "H" of table C–I shall be used for either printed wiring boards or test coupons.

TABLE C–I. C = 0 (zero defect) sampling.

Lot size	Sample size (number of test specimens to be inspected) 1/						
	Series A	Series D	Series F	Series H	Series J	Series L	Series N
1 to 8	All	All	All	5	3	2	1
9 to 15	All	All	13	5	3	2	1
16 to 25	All	All	13	5	3	2	1
26 to 50	All	32	13	5	5	3	2
51 to 90	50	32	13	7	6	4	2
91 to 150	50	32	13	11	7	5	2
151 to 280	50	32	20	13	10	6	4
281 to 500	50	48	29	16	11	7	4
501 to 1,200	75	73	34	19	15	8	4
1,201 to 3,200	116	73	42	23	18	9	4

1/ If lot size is smaller than sample size test all of the units.

C.5 TEST EQUIPMENT, CALIBRATION, AND MEASUREMENTS

C.5.1 Test equipment and calibration. All tests and measurements for process control, qualification testing, inspection of product for delivery (in-process and group A), or periodic conformance inspection (groups B or C) shall be made with capable instruments whose accuracy has been verified. Calibration of measurement, test equipment, and test standards that control the accuracy of inspection and test equipment and facilities shall be in accordance with NCSL Z540.3, or equivalent. Calibrated test equipment and test standards shall be controlled, used, and stored in a manner suitable to protect calibration integrity. Test equipment requiring calibration shall be identified and labeled in accordance with NCSL Z540.3, or an equivalent system, approved by the qualifying activity.

C.5.1.1 Resolution of measurement devices and test equipment capability. Unless otherwise specified (see A.3.1.1), the resolution of measurement devices and test equipment used for the evaluation of printed wiring board performance shall be at least a factor of 10 better than the limits or tolerances of a value to be determined. For example: A voltmeter would need a resolution of ±0.1 percent to determine a tolerance of ±1 percent. NOTE: State of the art requirements in which a 10:1 ratio cannot be effectively achieved due to a lack of national standards shall be justified and documented.

C.5.1.2 Electrical test frequency. When specified (see A.3.1.1), the frequency of the electrical test shall be the specified operating frequency of the printed wiring board. Where a frequency range is specified, major functional parameters shall be tested at the maximum and minimum frequencies of the range in addition to those tests conducted at any specified frequency within the range. Whenever electrical tests are conducted on printed wiring boards for which a range of frequencies, or more than a single operating frequency is specified, the frequency at which tests are conducted shall be recorded along with the parameters measured at those frequencies.

C.5.2 Test methods.

C.5.2.1 Acquiring activity or manufacturer imposed tests. Acquiring activity or manufacturer imposed tests shall be in accordance with the requirements specified in the master drawing. If any additional imposed tests detect a problem, the manufacturer shall submit all panels/printed wiring boards in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure.

C.5.2.2 Test method alternatives or variations. Alternate test methods or variation from the specified test method are allowed provided that it is demonstrated to the qualifying activity or their agent that such alternatives or variations in no way relax the requirements of this specification or the referenced test method. Alternate test methods, or variation from the specified test method, shall be approved by the qualifying activity or their agent before testing is performed. For proposed test variations, a test method comparative error analysis shall be made available for checking by the qualifying activity or their agent (see appendix B).

C.5.2.3 Procedure in case of test equipment malfunction or operator error. When it has been established that an improper test is due to test equipment malfunction or operator error, the inspection facility shall document the results of its investigations and corrective actions, if required, and shall make this information available to the qualifying activity and the acquiring activity, as applicable.

C.5.3 Numeric reporting. The results of printed wiring board verification shall be presented in accordance with the requirements outline herein.

C.5.3.1 Observed values (true and nominal). The specification limit requirements specified are for true values. Nominal values are indicated by the inclusion of a tolerance. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the values to be measured, so that the values of the test specimen parameters (as they would be under nominal test conditions) can be determined properly.

C.5.3.2 Significant digits. Unless otherwise specified (see A.3.1.1), the significant digits to be retained of an observed value shall be in accordance with the resolution requirements of C.5.1.1.

C.5.3.3 Rounding method. For purposes of determining conformance with the specification limit, an observed value, or a calculated value, shall be rounded "to the nearest unit" in the last right-hand significant digit to be retained in expressing the specification limit, in accordance with the rounding method of ASTM E29. The significant digits to be retained of an observed value or calculated value shall reflect the resolution requirements of C.5.1.1.

EXAMPLE 1: The minimum specified etchback requirement is .0002 inch. The resolution required of the measurement device in accordance with C.5.1.1 would to the ±.00001 inch. The significant digit to be retained would be one digit to the right of requirement, in this example, ".000RS" inch, where "R" is the requirement and "S" is the significant digit. In a situation where a test personnel uses an instrument capable of resolution to ±.000001 inch, a measurement of .000186 inch is determined for etchback on that test specimen. This value can be rounded to .00019 inch or reported as taken, .000186 inch. The observed value of .000186 inch cannot be rounded to .0002 inch.

EXAMPLE 2: The maximum specified printed wiring board thickness requirement is .090 inch. The resolution required of the measurement device in accordance with C.5.1.1 would to the ±.0001 inch. In this situation, the test personnel uses an instrument capable of resolution to ±.0001 inch, and records measurements of .0899, .0900, .0898, and .0897 inch for the printed wiring board thickness on that test specimen. The test determination of (.3594 / 4) .08985 inch is calculated. This test determination can be rounded to .0898 inch or reported as calculated. Rounding this value to .0899 inch would not be in accordance with rounding procedure of ASTM E29.

C.5.4 Control based on uncertainty. Test processes that have complex characteristics are best performed and controlled by the application of uncertainty analysis. The overall uncertainty in a test or measurement process shall be determined and the impact of said uncertainty on the product parameter tolerance shall be taken into account. The methods used for determining uncertainty shall be defined and documented. The method selected may use any or all combinations of the following forms:

a. Arithmetic addition (linear), normally produces an overly conservative estimate and reflects a highly improbable situation in which contributing errors are at their maximum limit at the same time and same direction.

b. Root sum square (RSS), normally applied where the errors tend to fit a normal distribution (Gaussian) and are from independent sources.

c. Partial derivatives, used where complex relationships exist.

d. Monte Carlo simulation, used in very complex situations where other methods are not easily applied or do not fit.

e. Standard reference material (or controlled correlation device) testing providing observable data. NOTE: Observable data from a controlled device may be relied upon to provide feedback that confirms process performance is within statistical limits.

f. Analysis of systematic and random errors, applying corrections as applicable.

g. Any other recognized method of combining errors into an expression of uncertainty substantiated by an engineering analysis.

C.6 SUITABILITY OF INSPECTION FACILITIES

C.6.1 Suitability of inspection facilities. The inspection facility used to perform qualification testing and periodic conformance inspection shall be found suitable by the qualifying activity to the requirements of ISO 17025, IPC–QL–653, or equivalent for the performance of the tests and inspection of compliant printed wiring boards. Additional details regarding the suitability status of an inspection facility are outlined in the DLA Land and Maritime publication "DSCC–VQ Laboratory Suitability Information" that can be downloaded or viewed at the following URL: http://www.landandmaritime.dla.mil/Downloads/VQGeneral/Labsuit-Book-140116.pdf.

C.6.2 Suitability status and test reports. Granting of laboratory suitability to an inspection facility does not mean that the Government will automatically accept or approve a test report prepared by the laboratory. Some of the most common reasons for rejection of qualification and periodic conformance test reports are the following:

a. Testing prior to receipt of an authorization to test.

b. Failure to record actual test conditions or results.

c. Failure to perform the proper test.

d. Failure to perform the test on the proper qualification test specimen.

e. Failure to test the minimum number of samples specified.

f. Incorrect test procedures.

g. Use of improperly calibrated test equipment.

h. Use of test equipment not previously found acceptable by DLA Land and Maritime.

C.6.3 Referee testing. Concerns with sample condition or sample identification shall be made to the qualifying activity prior to commencement of the referee testing. Comments on deviations from the applicable test method shall be made immediately at the time of testing. Unresolved concerns shall be specific in nature and submitted in writing to the laboratory's designated qualifying activity representative and the other observer at the time of testing.

C.7 DEFINITIONS FOR TEST EQUIPMENT AND INSPECTION FACILITIES

C.7.1 Accuracy. A measure of the closeness of an individual measurement or the average of a number of measurements to the true value. Accuracy includes a combination of random error (precision) and systematic error (bias) components that are due to sampling and analytical operations.

C.7.2 Bias. The systematic or persistent distortion of a measurement process, which causes errors in one direction (i.e., the expected sample measurement is different from the sample's true value).

C.7.3 Calibration. Calibration is an activity related to measurement and test equipment. Calibration is the comparison of measurement standard, instrument, or item of known precision and bias with another standard, instrument, or item to detect, correlate, report, or eliminate by adjustment, any variation in the precision and bias of the item being compared. Use of calibrated measurement standard, instrument, or items provide the basis for value traceability of product technical specifications to national standard values.

C.7.4 Limit or specification limit. A specification limit are numerical requirements specified in appendix A, in the applicable master drawing, or in referenced documents, for the minimum or maximum value used for acceptance purposes.

C.7.5 Measurement and testing equipment. Tools, gauges, instruments, sampling devices, or systems used to calibrate, measure, test, or inspect in order to control or acquire data to verify conformance to specified requirements.

C.7.6 Precision. The degree to which a measurement standard, instrument, item, test, or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC), the term is many times used interchangeably with "repeatability". Precision is a measurement of how closely the analytical results can be duplicated.

C.7.7 Resolution. The smallest unit of readability or indication of known value on an instrument, device, or assemblage thereof. It is also related to the gradations on measuring instruments and the ability of the inspection/test personnel to interpret between those gradations. The resolution value is frequently used in the device literature to classify the instrument.

C.7.8 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRMs used in product testing provide traceability for technical specifications. SRMs do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

C.7.9 Tolerance (IPC–T–50). The total amount by which a specific dimension is permitted to vary. A tolerance is indicated in this specification only if it is expressed as the variation about a specified value (also known as a "nominal value").

C.7.10 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

C.8 Supporting documents. The documents in this section may be used as guidelines for understanding measurement and test assurance principals.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO 10012 – Measurement Management Systems – Requirements for Measurement Processes and Measuring Equipment – First Edition
ISO 14253–1 – Geometrical Product Specifications (GPS) - Inspection by Measurement of Workpieces and Measuring Equipment - Part 1: Decision Rules for Proving Conformance or Non-Conformance with Specifications.

(Copies of these documents are available online at http://www.iso.org.)

ASME INTERNATIONAL (ASME)

ASME B89.7.3.1 – Guidelines for Decision Rules: Considering Measurement Uncertainty in Determining Conformance to Specifications.
ASME B89.7.3.2 – Guidelines for the Evaluation of Dimensional Measurement Uncertainty.

(Copies of these documents are available online at http://www.asme.org.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540.2 – U. S. Guide to the Expression of Uncertainty in Measurement.

(Copies of these documents are available online at http://www.ncsli.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

SUPERSESSION AND USAGE OF LEGACY DESIGN STANDARDS

D.1 SCOPE

D.1.1 Scope. This appendix contains guidance concerning the supersession of legacy Department of Defense documents such as MIL–P–50884 revision C and MIL–STD–2118. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

D.2 APPLICABLE DOCUMENTS

D.2.1 General. The documents listed in this section are specified in sections D.3 and D.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections D.3 and D.4 of this specification, whether or not they are listed.

D.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50	–	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.
IPC–2221	–	Generic Standard on Printed Board Design.
IPC–2223	–	Sectional Design Standard for Flexible Printed Boards.
J–STD–003	–	Solderability Tests for Printed Boards.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

D.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3 DEFINITIONS

D.3.1 Design standard. A document that establishes the standard practices, guidelines, and default values for the design of printed wiring boards. Within this document, the term "design standard" is used to describe those documents that contain the design, construction, material, and test coupon requirements and guidelines.

D.3.2 Legacy designs or documents. See D.4.1.

D.3.3 Supersession. The act of replacing a legacy document that no longer exists or is no longer supported with a currently supported document.

D.3.4 Quality conformance test circuitry. See IPC–T–50.

D.3.5 Printed wiring board type. The printed board types are defined in IPC–2223.

D.4 SUPERSESSION

D.4.1 Superseded specifications. Appendix A of this document includes the essential requirements of the previous revision and can be used to supersede the following specifications:

a. MIL–P–50884C, dated 4 May 1984 with amendment 1, dated 19 August 1988.

b. MIL–P–50884C, dated 4 May 1984 with amendment 2, dated 22 June 1990.

c. MIL–P–50884C, dated 4 May 1984 with amendment 3, dated 13 December 1991.

d. MIL–P–50884C, dated 4 May 1984 with amendment 4, dated 9 April 1993.

e. MIL–P–50884C, dated 4 May 1984 with amendment 5, dated 27 November 1998.

f. MIL–P–50884D, dated 28 December 2000.

g. MIL–P–50884D, dated 28 December 2000 with amendment 1, dated 13 September 2002.

h. MIL–P–50884D, dated 28 December 2000 with amendment 2, dated 29 May 2006.

j. MIL–P–50884E, dated 24 November 2008.

k. MIL–P–50884E, dated 24 November 2008 with amendment 1, dated 4 July 2009.

l. MIL–P–50884E, dated 24 November 2008 with amendment 2, dated 14 February 2010.

m. MIL–P–50884E, dated 24 November 2008 with amendment 3, dated 1 September 2010.

D.4.1.1 Reference to superseded specifications. All the requirements of this document (MIL–PRF–50884F) can be interchangeable with those of MIL–P–50884. Therefore, existing procurement documents (master drawings or OEM documents) referencing MIL–P–50884 need not be revised, updated, or changed to make reference to MIL–PRF–50884F in order for this document to be used.

D.4.1.2 Revisions. Printed wiring boards tested to this document generally would meet or exceed the performance requirements of past revisions. However, due to various changes in acceptability and evaluation criteria, testing procedures and test coupon sampling, an exact duplication of a previous revision cannot be claimed or made in all areas of concern. Manufacturers should not pick-and-choose or mix acceptability requirements and test procedures from one revision of MIL–P–50884 to another. Compliance should be either to MIL–P–50884B, MIL–P–50884C (with a specific amendment, if applicable), or this document entirely, unless the manufacturer documents a direct correlation between the revisions (with any amendments, if applicable) under consideration.

D.4.2 Superseded guidelines and standards. The following design standards have been superseded by IPC–2221 and IPC–2223 for all types and classes of printed wiring boards:

a. MIL–STD–2118, dated 4 May 1984.

b. MIL–P–50884B (appendix), dated 19 January 1976.

c. MIL–P–50884A, dated 5 June 1972.

D.4.2.1 Retooling. Printed wiring boards that were designed using superseded Department of Defense design standards shall be converted to IPC–2221 and IPC–2223.

D.4.2.2 Superseded types. Before MIL–P–50884C, only single and double sided printed wiring boards were covered in MIL–P–50884. The obsolete type A requirements in MIL–P–50884B (flexible printed wiring that is capable of withstanding at least one solder operation without terminal degradation) did not carry over to MIL–P–50884C. However, the type B requirements in MIL–P–50884B (flexible printed wiring that is capable of withstanding at least five solder and unsolder operations without terminal area degradation, i.e., rework simulation) was carried over to and extended to all printed wiring board designs in MIL–P–50884C.

D.4.3 Testing.

D.4.3.1 Group A inspection. Group A inspection should be performed to the specific revision, and amendment if applicable, called out by the acquisition documents. For example, if printed wiring boards are produced to MIL–P–50884C with amendment 1, MIL–P–50884C with amendment 3 and MIL–P–50884D, a manufacturer would be expected to perform group A testing, for the applicable lot, to the requirements of the revision specified. In those three different revisions (C w/amendment 1, C w/amendment 3, and D) a requirement for an acceptability criteria or test procedure may be the same or it might be significantly different. Retention of qualification summaries for group A should list the lots produced, grouped by revision and amendment.

D.4.3.2 Group B samples and testing. Samples to be selected for group B testing should be based on the most complex compliant printed wiring boards produced that month. For example, if printed wiring boards are produced to MIL–P–50884C, MIL–P–50884C with amendment 4 and MIL–P–50884D during a given month, and the most complex printed wiring boards produced that month were in the lot ordered to MIL–P–50884C with amendment 4, then that should be the lot from which the group B sample should be selected. The samples should be tested in accordance with MIL–P–50884C with amendment 4. If during that same month, printed wiring boards were produced to MIL–P–50884B and MIL–P–50884C (unamended), group B tests to those specific revisions would also be required in order to be compliant to those revisions, unless specifically specified in the contract.

D.4.3.3 Group C samples and testing. Group C testing is for manufacturers of installation use A and use B printed wiring boards to verify that it is still capable of meeting the flexibility class performance requirements. Samples to be selected for group C testing, unlike group B inspection, are not based on the most complex compliant printed wiring boards produced that month or reporting period. The group C samples can be either production printed wiring boards or the appropriate test coupon.

D.4.4 Superseded test coupons. Before MIL–P–50884C, test coupons were only used for first article inspection and not required for production. The production panel test coupons were introduced within MIL–P–50884C and MIL–STD–2118 were for the supplier certification program concept. The production test coupons of MIL–P–50884C, described within MIL–STD–2118, should be used when already incorporated onto production tooling. New designs or jobs should use the test coupons specified in IPC–2221. Table D–I contains a cross listing of the various test coupon designations that have been used in superseded design standards.

D.4.5 Test coupons, placement, quantity and usage. IPC–2221 contains a table that specifies for each production panel the test coupon placement, quantity (see note below) and usage. However, MIL–STD–2118 did not provide a table that specifies for each production panel the test coupon placement, quantity, and usage.

NOTE: A sufficient number of test coupons should be incorporated onto the production panel in order to be able to perform group A and when necessary, group B inspection regardless of the number of test coupons specified by the design standard.

D.4.5.1 Intended use and intent of this appendix. This appendix can be used to understand the test coupons that were referenced in previous revisions of this document. These guidelines are intended for the re-identification and proper usage of test coupons within this document that are or were originally identified in various legacy Department of Defense printed wiring board design standards. This appendix is intended for use in conjunction with a manufacturer's verification conformance compliancy program.

D.4.5.2 Guidance concerning legacy test coupons. IPC–2221 contains a table that specifies for each production panel the test coupon placement, quantity, and usage. However, MIL–STD–2118 did not contain a table that specifies for each production panel the test coupon placement, quantity, and usage. In the past, when attempting to be compliant with the group A table of MIL–P–50884C, it was confusing and difficult to determine how many test coupons were needed on the production panel, how many test coupons needed to be microsectioned, and what evaluations could be combined during group A inspection.

TABLE D–I. Test coupon translation.

Usage in this document	MIL–STD–2118	IPC–D–249	IPC–2221 1/	
			Legacy	New design
Hole solderability Non-stressed specimens (microsection)	A	A	A	A
Resistance to soldering heat (solder float thermal stress) Rework simulation	B	B	B	B
Plating adhesion	C	C	C	C
Interconnect resistance (continuity)	D	D	D	D
Insulation resistance	E		E	E
Flexibility	F	H	H	H
Solder mask	I or G 2/	G	G/T	G
Peel strength	3/		P	
Solderability			S	
Registration			F	

1/ H coupon was added to IPC–2221 with the issuance of amendment 1.
2/ MIL–P–50884C, group A table reference test coupon "G" while MIL–STD–2118 displayed a test coupon "I" next to the solder mask test coupon figure.
3/ See appendix H.

QUALIFICATION REQUIREMENTS FOR ALL LEVELS OF PRODUCT ASSURANCE

E.1 SCOPE

E.1.1 Scope. This appendix contains the qualification requirements for all levels of product assurance of printed wiring boards covered by this specification. The process for extending qualification is also outlined herein. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

E.2 APPLICABLE DOCUMENTS

E.2.1 General. The documents listed in this section are specified in sections E.3 and E.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections E.3 and E.4 of this specification, whether or not they are listed.

E.2.2 Government documents.

E.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.
MIL–PRF–31032/3 – Printed Wiring Board, Flexible, Single and Double Layer, With or Without Plated Holes, With or Without Stiffeners, for Soldered Part Mounting.
MIL–PRF–31032/4 – Printed Wiring Board, Rigid-Flex or Flexible, Multilayer, with Plated Holes, with or Without Stiffeners, for Soldered Part Mounting.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

E.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3 REQUIREMENTS

E.3.1 Qualification inspection. Qualification testing shall be performed on suitable test vehicles in accordance with the qualifying activity approved MIL–PRF–31032 qualification test plan.

E.3.1.1 Expiration of qualification. Manufacturers already qualified to the QPL level of this document will retain that listing until it expires. The 3 year expiration time will not apply to any qualifications performed to this appendix.

E.3.1.2 Requalification. Products qualified in accordance with this appendix shall be monitored and maintained through the manufacturer's Capability Verification Inspection program and do not require requalification to this specification.

E.3.2 Reciprocal qualification from MIL–PRF–31032. A reciprocal qualification listing (i.e., from a technology qualified to a MIL–PRF–31032 specification sheet) to this appendix will depend on the level of QML technology qualified. Unless otherwise detailed in MIL–PRF–31032 qualification test plan, following guidelines will apply:

a. Printed wiring board type (see 6.4.3 and D.3.5). The extent of qualification for base materials types defined in E.4 will apply. EXAMPLE: A type 2 qualification under a MIL–PRF–31032 specification sheet will not justify a type 4 qualification listing to this appendix.

b. Printed board material. The extent of qualification for base materials types defined in MIL–PRF–31032 will apply. EXAMPLE: An adhesiveless flexible metal clad base material qualification under a MIL–PRF–31032 specification sheet will justify an adhesiveless flexible metal clad base material qualification listing to this appendix (of the corresponding type).

c. Complexity. Printed wiring board designs verified using the QML product assurance option shall flow through the conversion of customer requirements element of the approved Quality Management (QM) plan as described in MIL–PRF–31032, appendix A. The Technical Review Board (TRB) shall evaluate designs exceeding their current QPD–31032 qualification listing to determine if the add–on qualification provisions of MIL–PRF–31032 shall be used. Reasons for not using the add–on qualification provisions shall be documented in the periodic status reports.

E.3.3 Retention (see B.6.4). The QML status report described in MIL–PRF–31032 will cover the retention requirements to this appendix.

E.4 EXTENT OF QUALIFICATION

E.4.1 General. The extent of qualification shall be in accordance with the following ranges specified in E.4.1.1 through E.4.1.7.

E.4.1.1 Printed wiring board type. Qualification of a particular printed wiring board type shall be extended to cover all conductor patterns of that same printed wiring board type produced.

a. Qualification of type 4 printed wiring boards shall be extended to cover all other types (5, 3, 2, and 1).

b. Qualification of type 3 printed wiring boards shall be extended to cover types 1 and 2 printed wiring boards.

c. Qualification of type 2 printed wiring boards shall be extended to cover type 1 printed wiring boards.

d. Qualification of type 5 printed wiring boards shall be extended to cover type 1 printed wiring boards.

e. Qualification of any type shall be extended to cover the approved type or types with a stiffener.

E.4.1.2 Installation use. Qualification to installation use B shall be extended to cover installation use A. If not qualifying installation use B, installation use A shall be qualified.

E.4.1.3 Rework capability. Qualification to rework capability grade R shall be extended to cover rework capability grade U.

E.4.1.4 Base materials. All flexible and rigid base materials to be used in subsequent production shall be qualified.

E.4.1.5 Conductor surface finish. All conductor surface finishes to be used in subsequent production shall be qualified.

E.4.1.6 Foil lamination. If foil lamination techniques are to be used in subsequent production, the process shall be qualified.

E.4.1.7 Solder mask. All solder masks to be used in subsequent production shall be qualified.

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EXTERNAL VISUAL AND DIMENSIONAL ILLUSTRATIONS

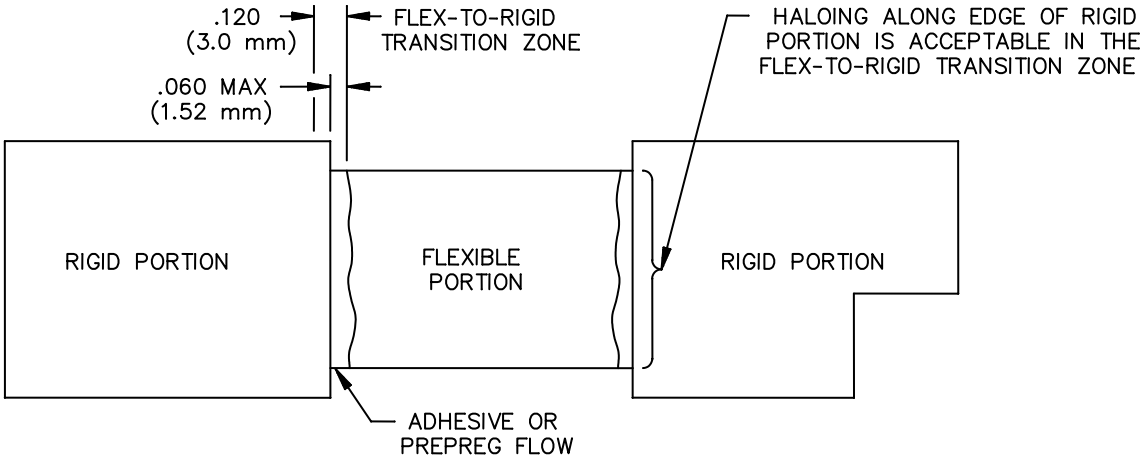
F.1 SCOPE

F.1.1 Scope. This appendix establishes uniform criteria for evaluating and classifying defects on partially complete or completed printed wiring boards, qualification test specimens, and test coupons during visual and dimensional inspections. This appendix describes the desired, acceptable, and nonconforming conditions of printed wiring boards that are externally observable. It represents the visual interpretation of minimum requirements set forth in appendix A of this specification. The criteria shall apply whether a 100-percent inspection or a sampling plan procedure is used. This appendix is a mandatory part of this specification for manufacturers qualified to the QPL product assurance level of appendix A. The information contained herein is intended for compliance.

F.2 APPLICABLE DOCUMENTS This section is not applicable to this appendix.

F.3 EXTERNALLY OBSERVABLE CHARACTERISTICS

F.3.1 General. This section addresses those characteristics which are observable from the surface of printed wiring boards. This includes those characteristics that are external and internal in the printed wiring board, but visible from the surface (see figures F–1 through F–14 for examples).



NOTES:
1. Dimensions are in inches.
2. Millimeter equivalents are given for general information only.

FIGURE F–1. Transition zone for flexible to rigid junctions.

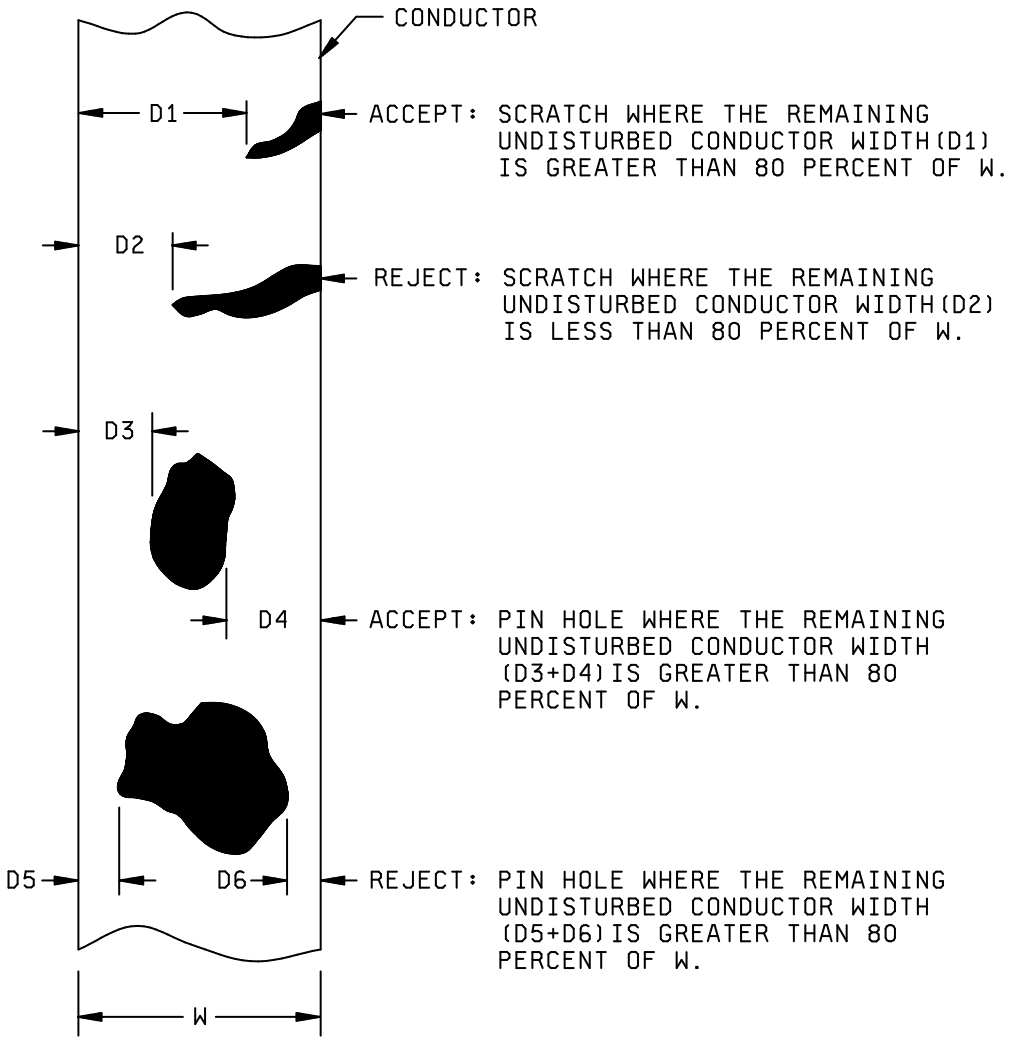


FIGURE F–2. Conductor pattern imperfections.

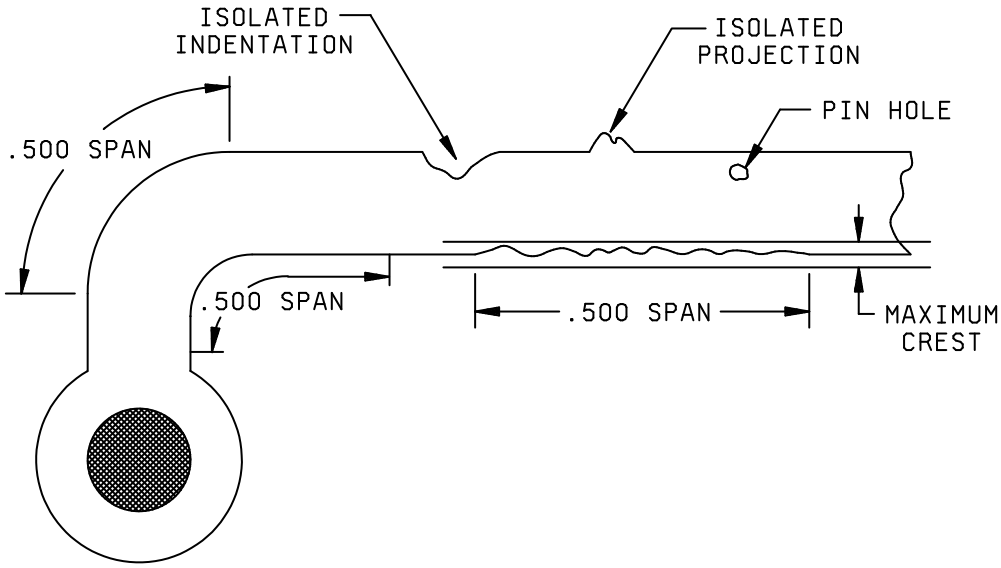


FIGURE F–3. Conductor edge definition imperfection measurement.

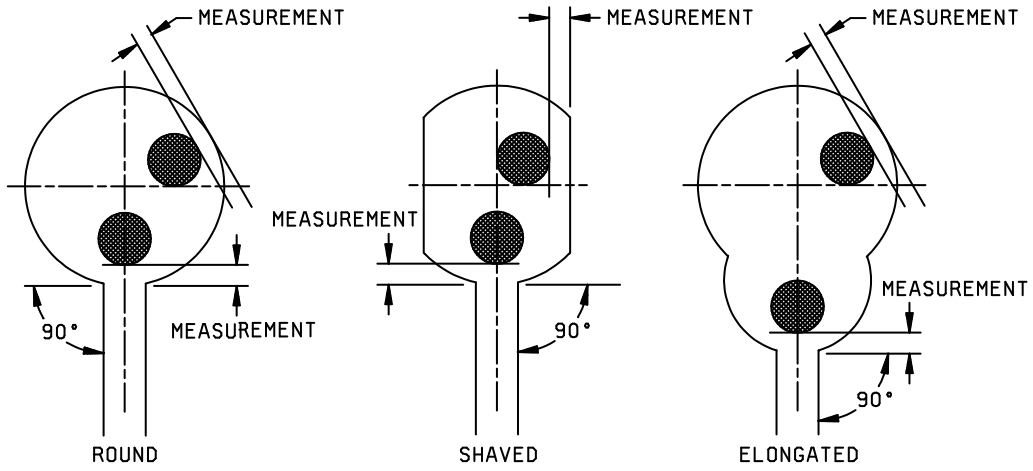


FIGURE F–4. External annular ring measurement.

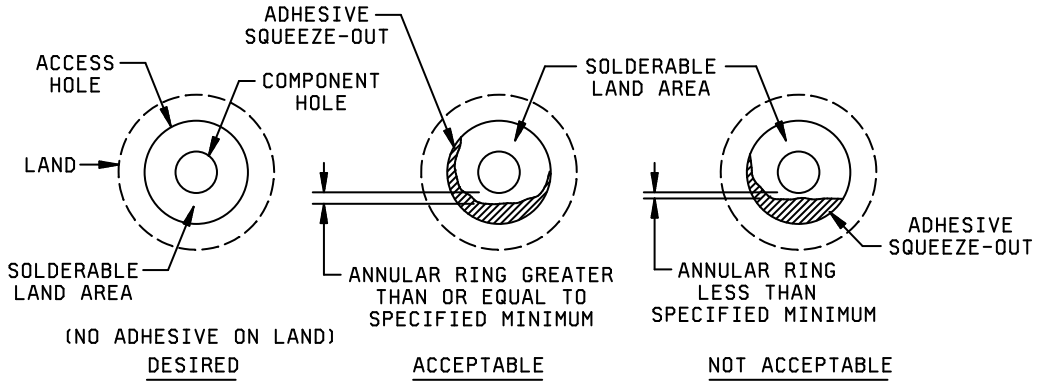


FIGURE F–5. Adhesive on land.

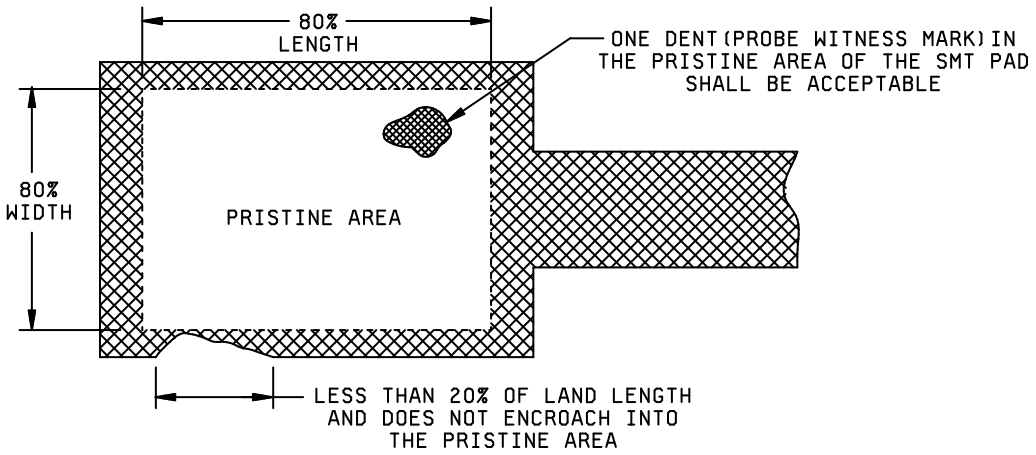


FIGURE F–6. Rectangular surface mount lands.

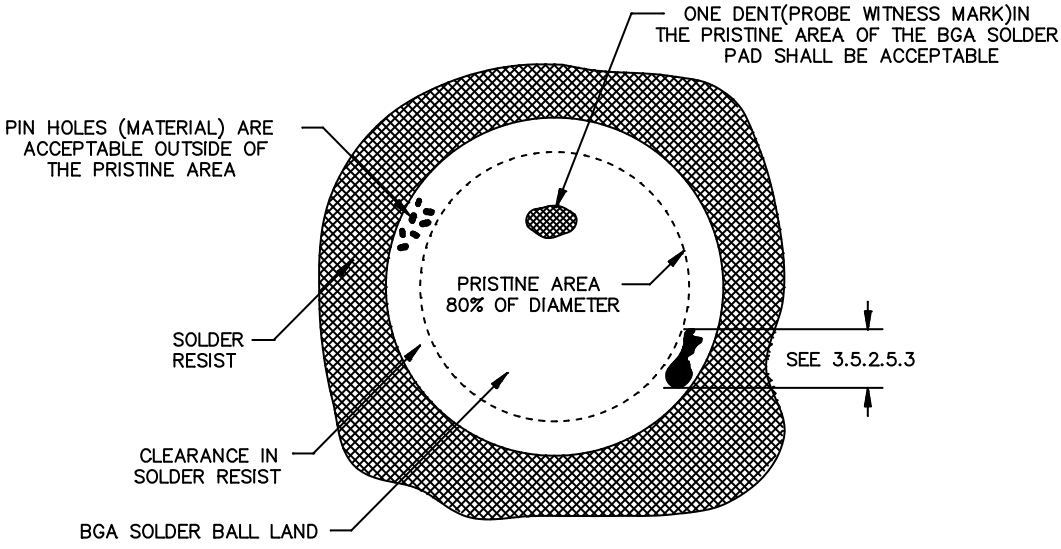


FIGURE F–7. Round surface mount lands (BGA pads).

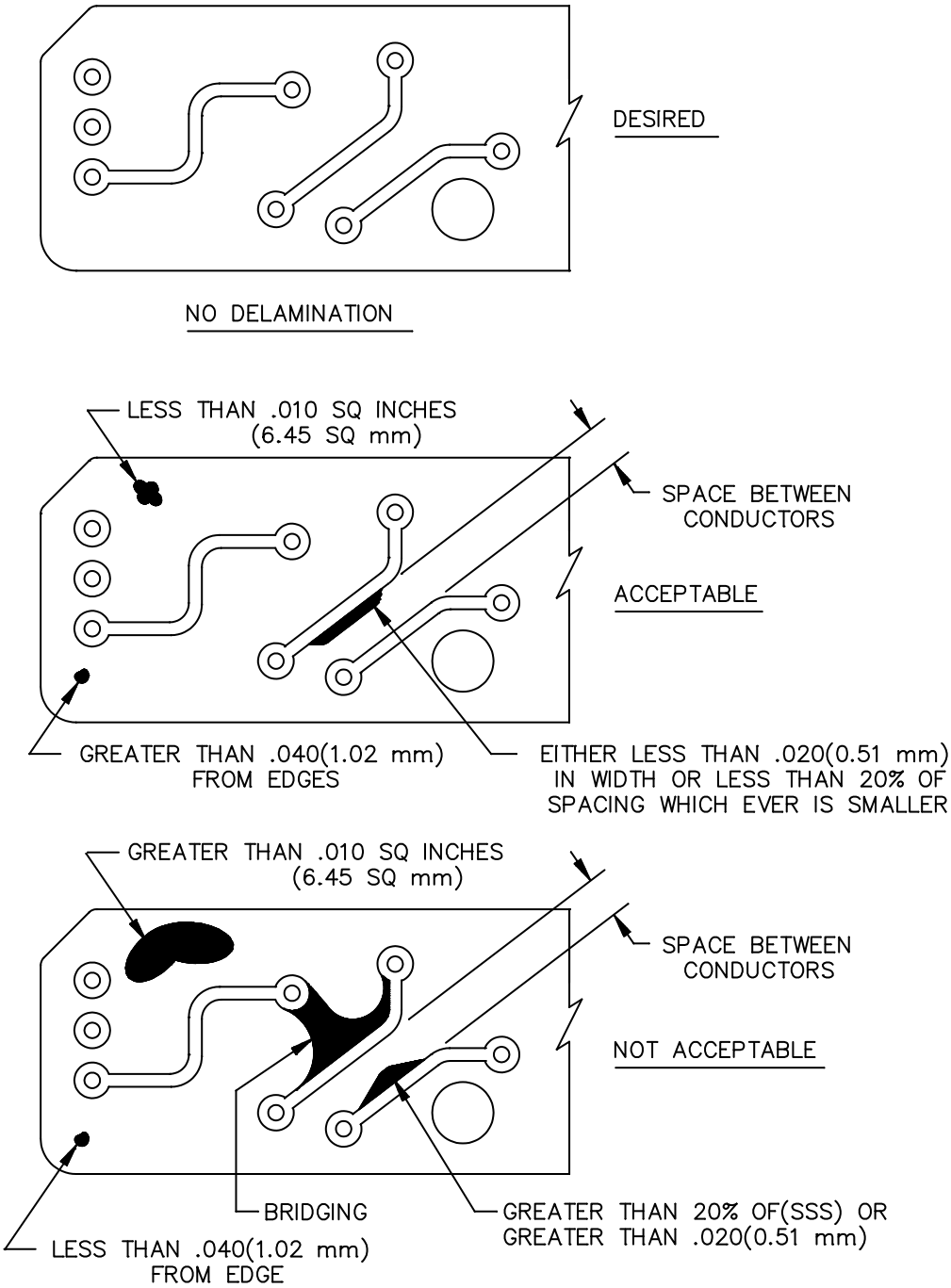


FIGURE F–8. Cover material separations.

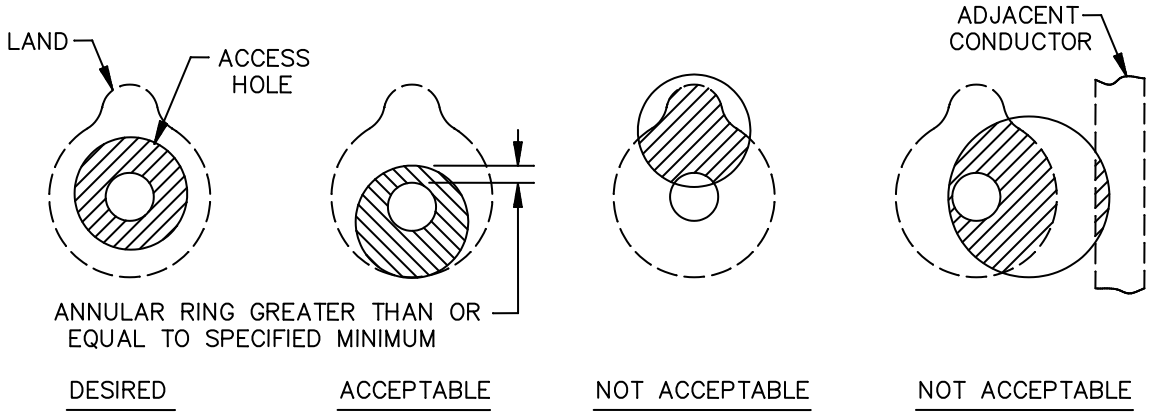
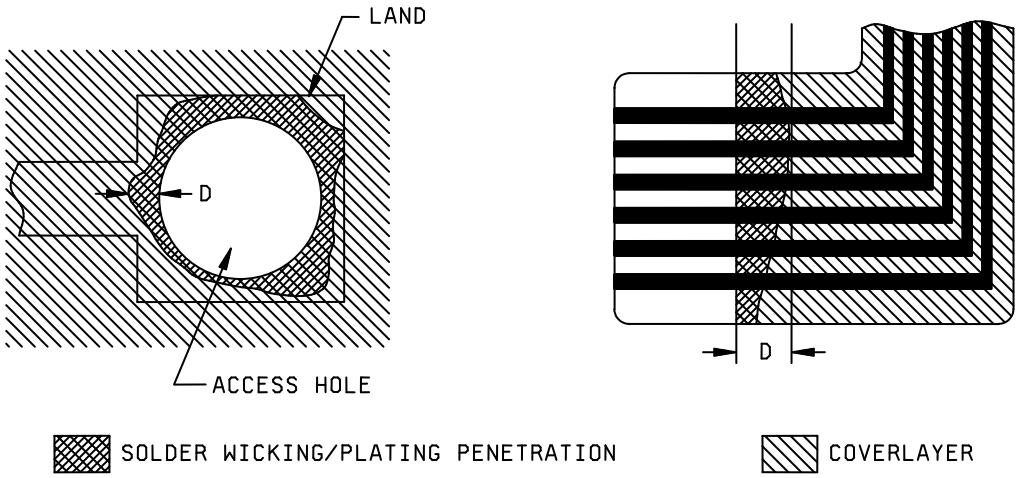


FIGURE F–9. Cover layer access hole registration.



NOTE: Dimension D is the distance of maximum wicking penetration.

FIGURE F–10. Cover layer, wicking of conductor surface finish.

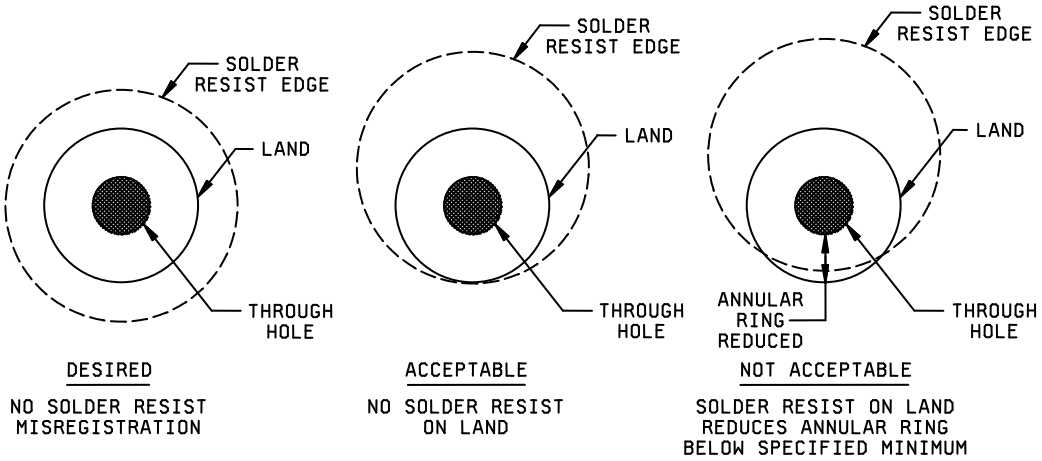


FIGURE F–11. Solder mask registration.

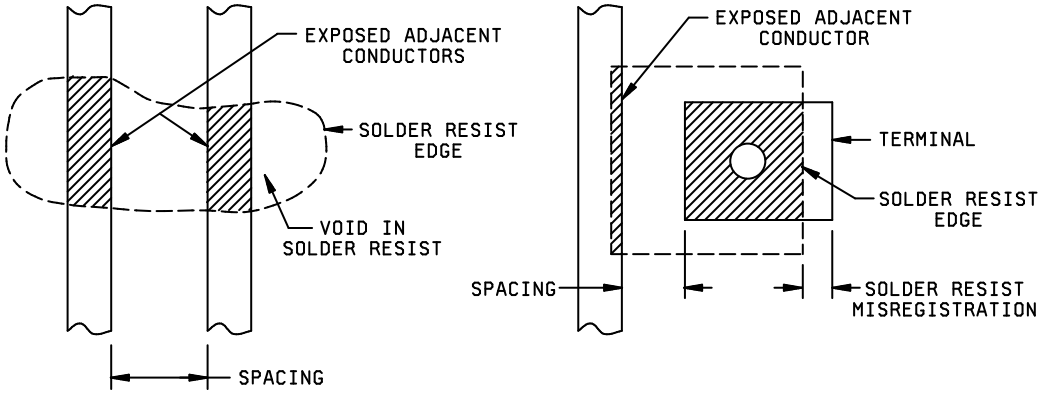


FIGURE F–12 Solder mask deviations.

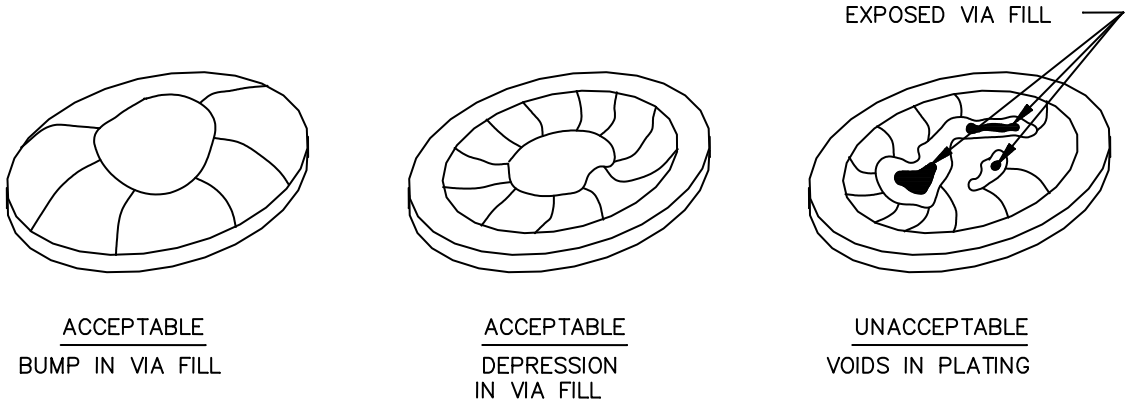


FIGURE F–13 Via cap plating details.

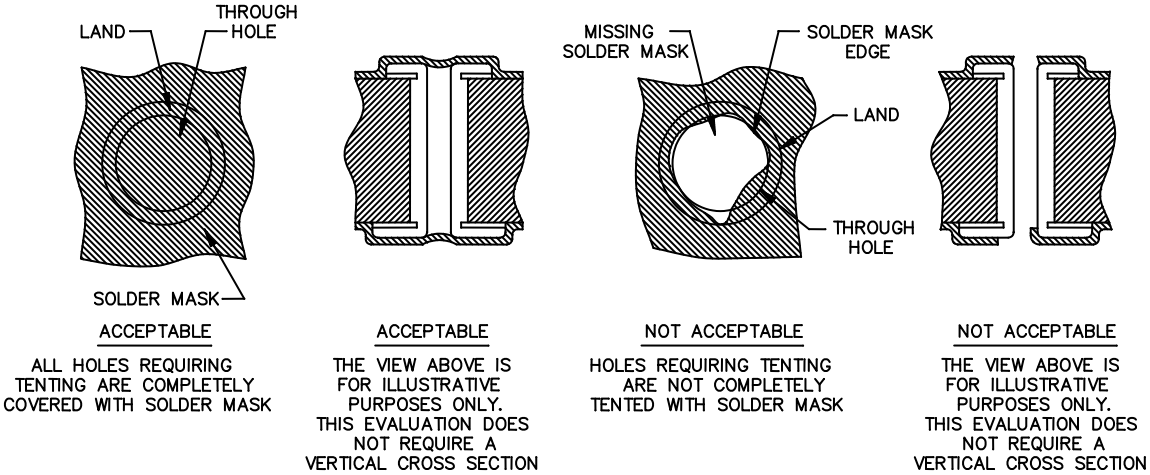


FIGURE F–14 Tented solder mask details.

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METALLOGRAPHIC ILLUSTRATIONS

G.1 SCOPE

G.1.1 Scope. This appendix establishes uniform criteria for evaluating and classifying characteristics and defects which are observable using metallographic techniques on partially complete or completed printed wiring boards, qualification test specimens, and test coupons. This appendix describes the preferred, acceptable, and nonconforming conditions that are either externally or internally observable. It represents the visual interpretation of minimum requirements set forth in appendix A of this specification. The criteria shall apply whether a 100-percent inspection or a sampling plan procedure is used. This appendix is a mandatory part of this specification for manufacturers qualified to the QPL product assurance level of appendix A. The information contained herein is intended for compliance.

G.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

G.2.1 General. The documents listed in this section are specified in sections A.3 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections A.3 of this specification, whether or not they are listed.

G.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–A–600 – Acceptability of Printed Boards.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

G.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

G.3 INTERNALLY OBSERVABLE CHARACTERISTICS

G.3.1 General. This section addresses those characteristics which are observable during metallographic examination. This includes those characteristics that are both internal and on the surface layer of the printed wiring board test specimen (see figures G–1 through G–20 for examples). IPC–A–600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein, or specified on the printed board procurement documentation, it shall comply with the class 3 "acceptable" or "target condition" criteria of IPC–A–600.

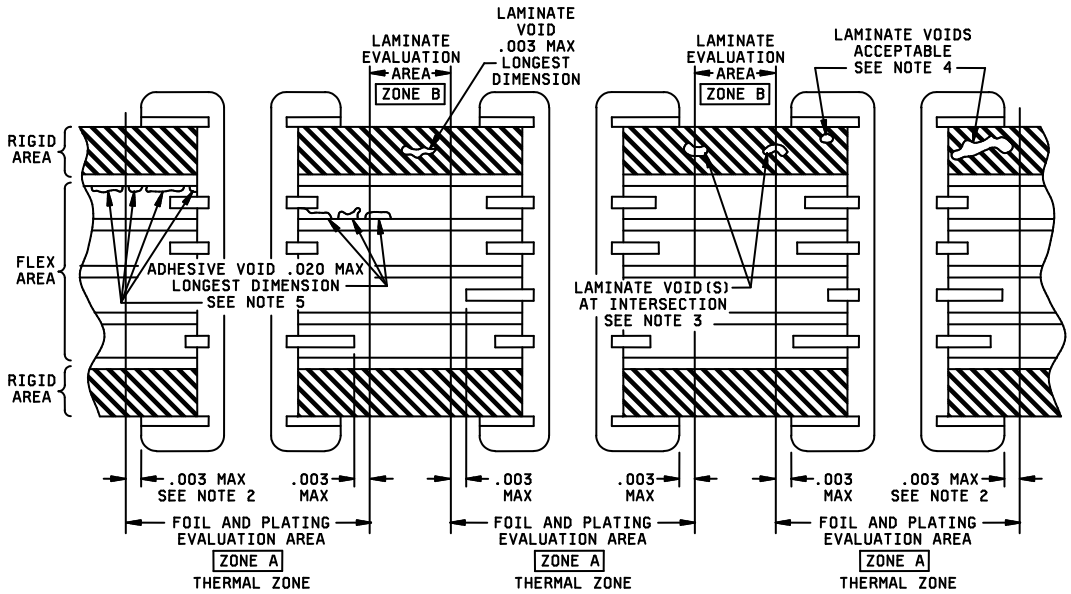


FIGURE G–1. Thermal zone for plated-through holes (cross section) after stress testing.

NOTES:

1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than .003 inch (0.08 mm) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.
5. Multiple adhesive voids between two adjacent plated-through holes in the same plane shall not have a combined length exceeding .02 inch (0.5 mm).

FIGURE G–1. Thermal zone for plated-through holes (cross section) after stress testing.

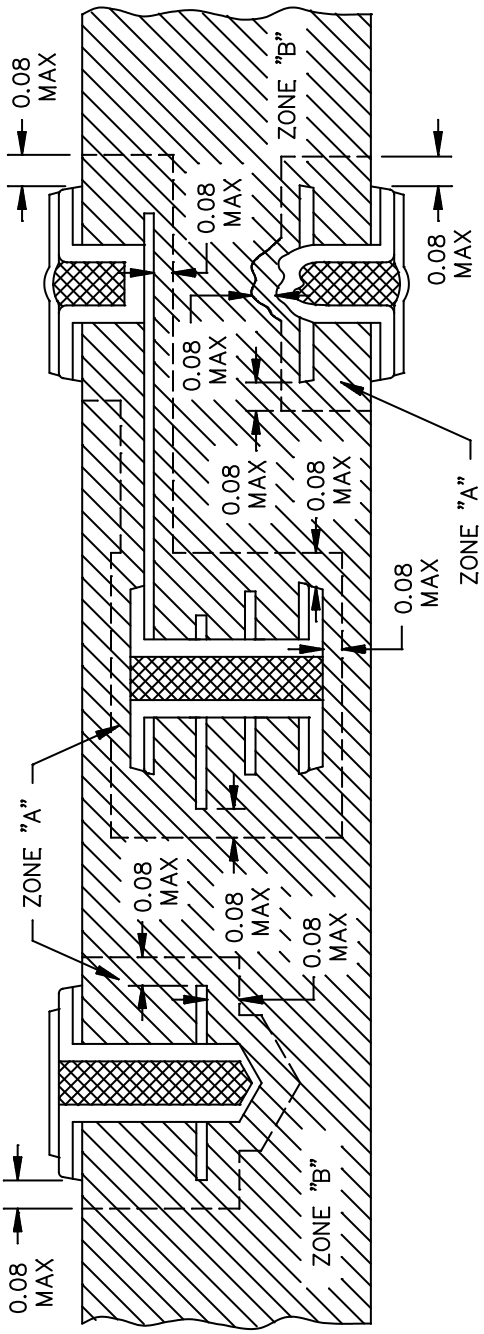


FIGURE G–2. Thermal zone for blind and buried vias cross section after stress testing.

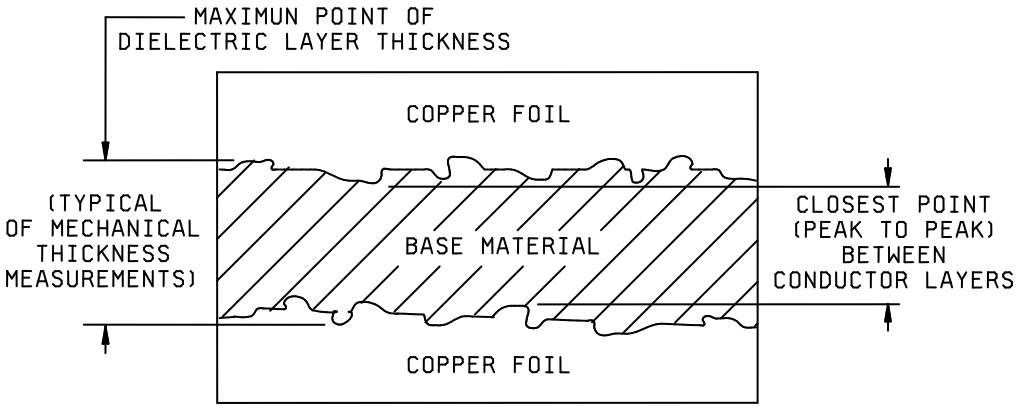


FIGURE G–3. Dielectric thickness measurement.

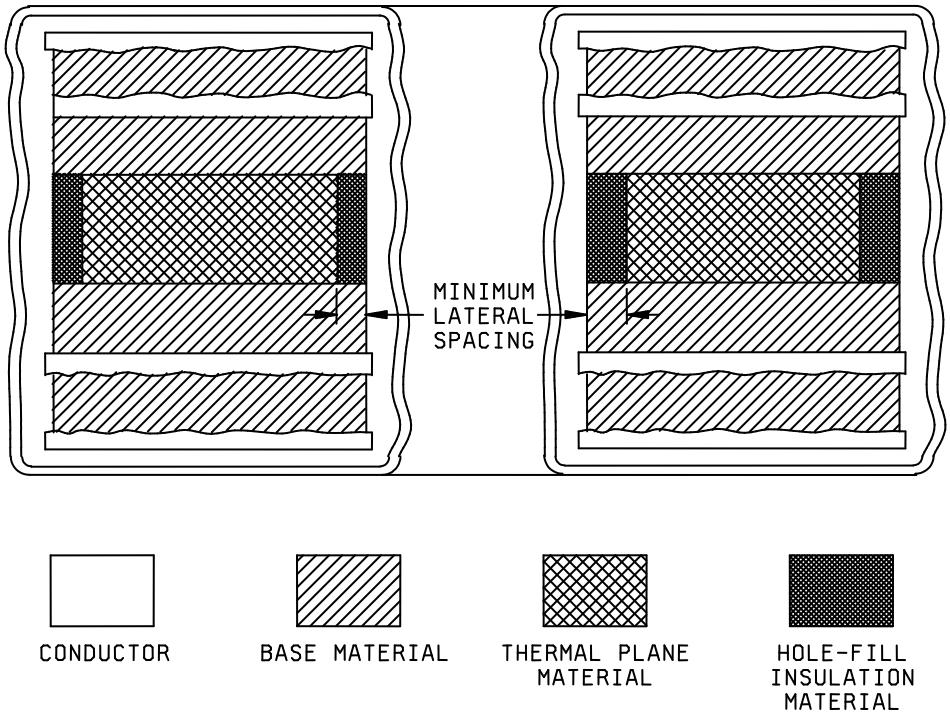


FIGURE G–4. Isolated heat sink plane dielectric spacing.

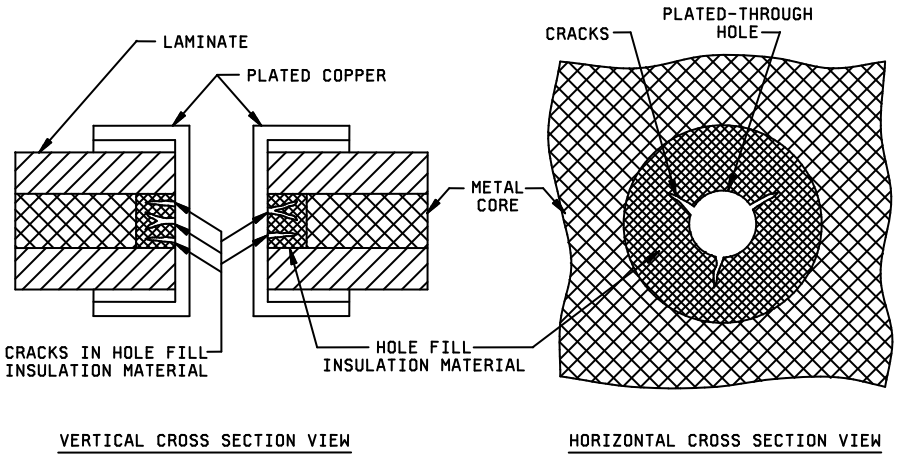


FIGURE G–5. Insulation material cracks; metal cores or heat sink planes.

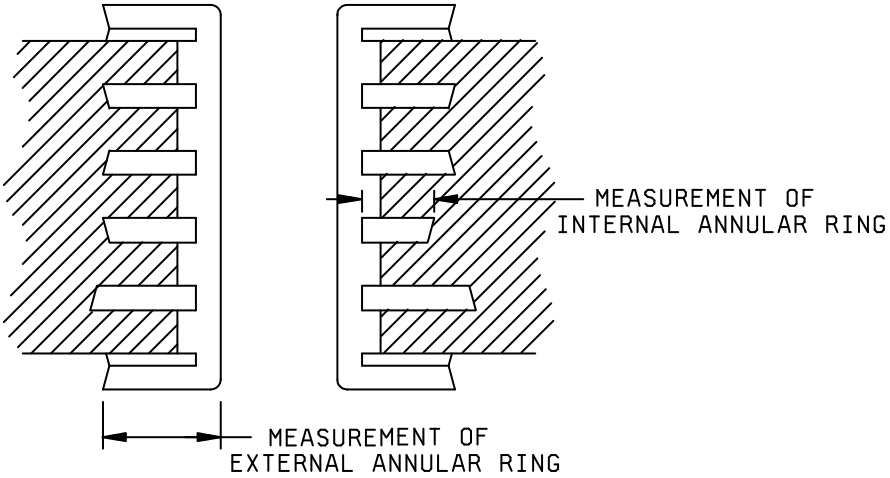


FIGURE G–6. Internal annular ring measurements.

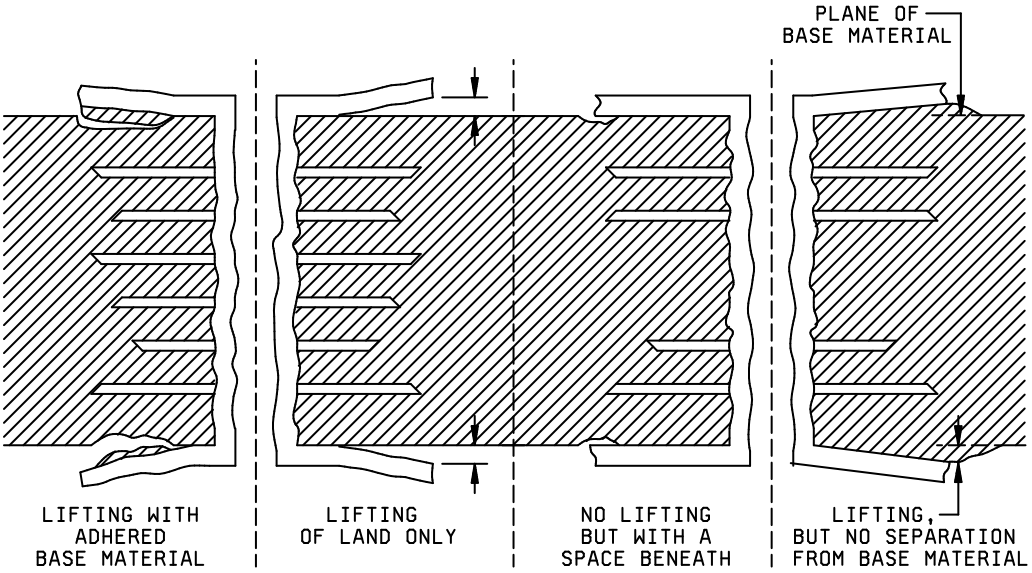
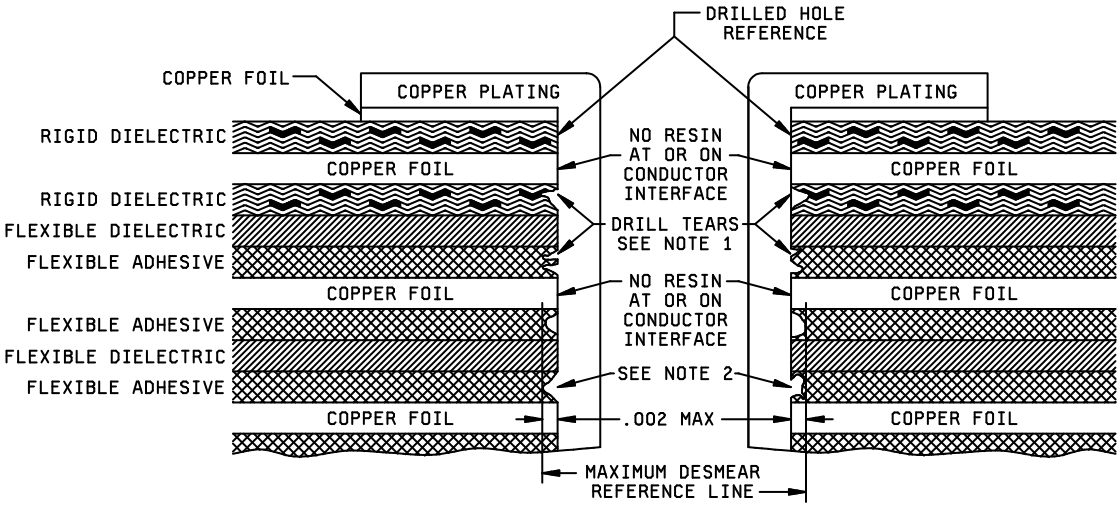


FIGURE G–7. Bonding of conductor to base material and lifted lands.



NOTES:

1. Drill tears are not measured. Drill tear-outs shall be enclosed.
2. The adhesive or dielectric material removed shall be enclosed.

FIGURE G–8. Smear removal.

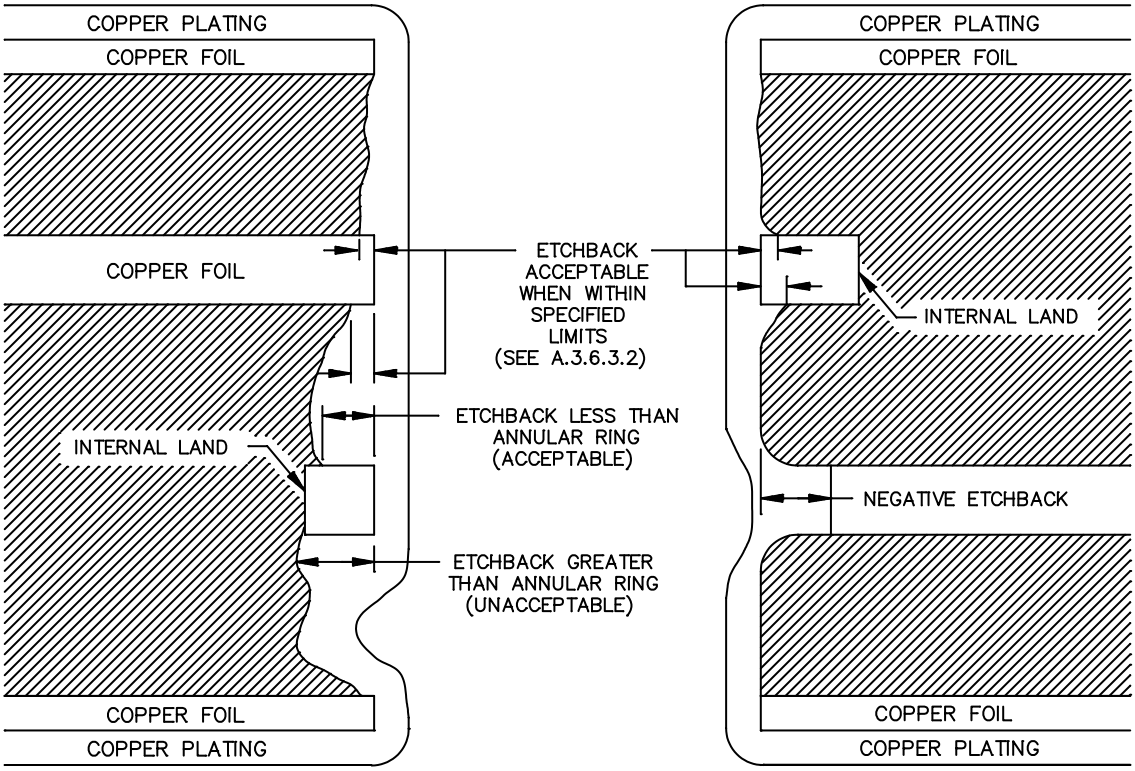


FIGURE G–9. Etchback.

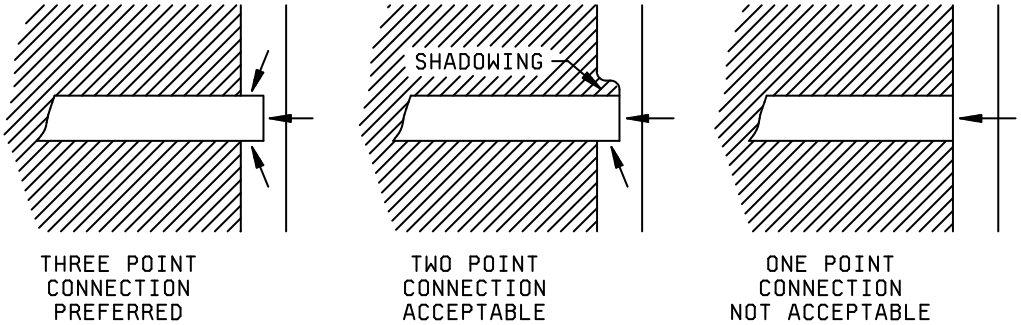


FIGURE G–10. Forms of plating connections to internal layers.

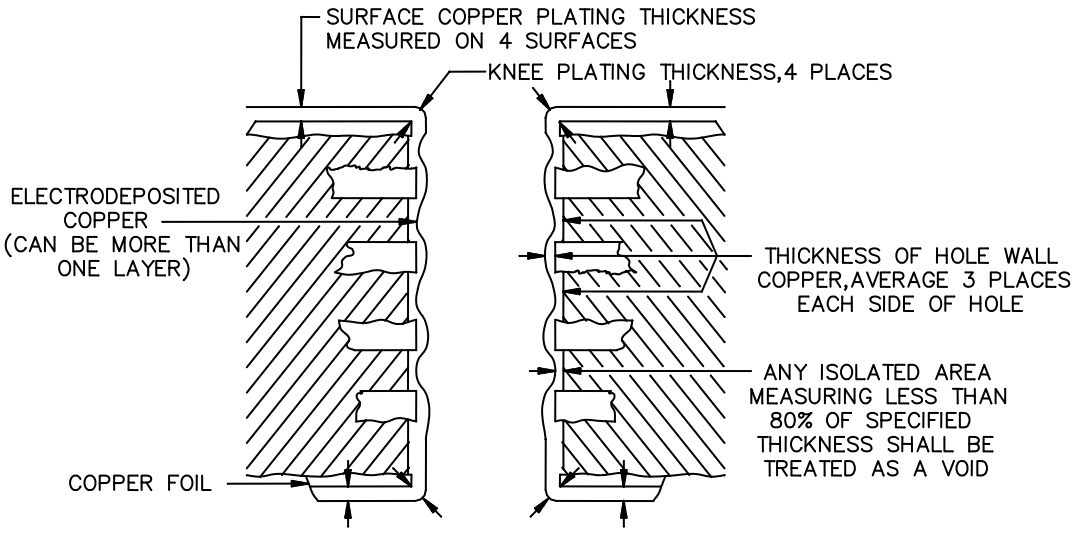


FIGURE G–11. Copper plating thickness.

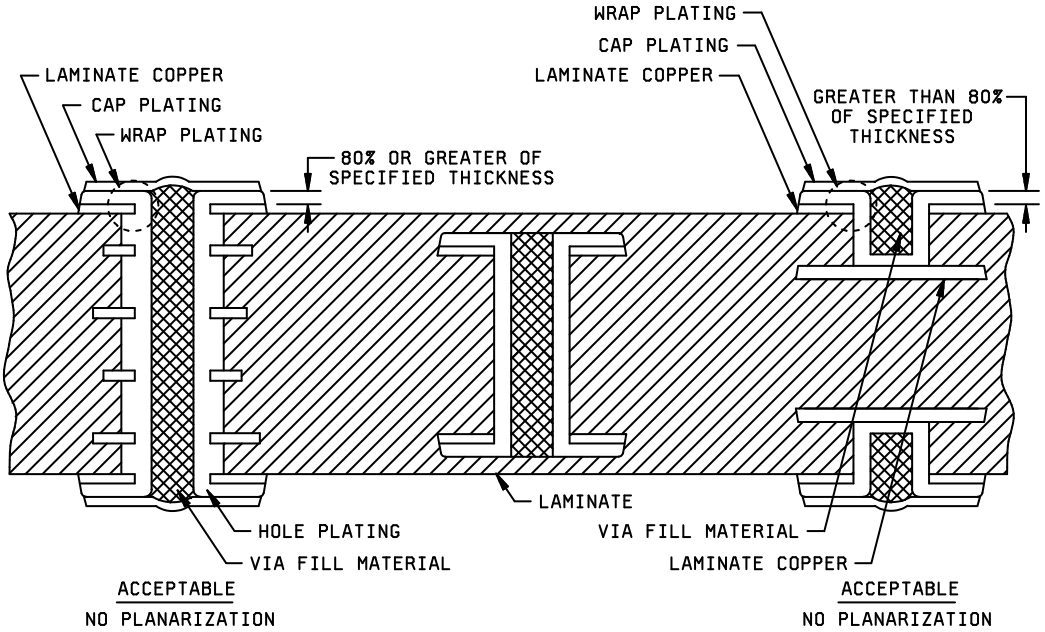


FIGURE G–12. Acceptable non-planarized plated hole structure wrap copper plating.

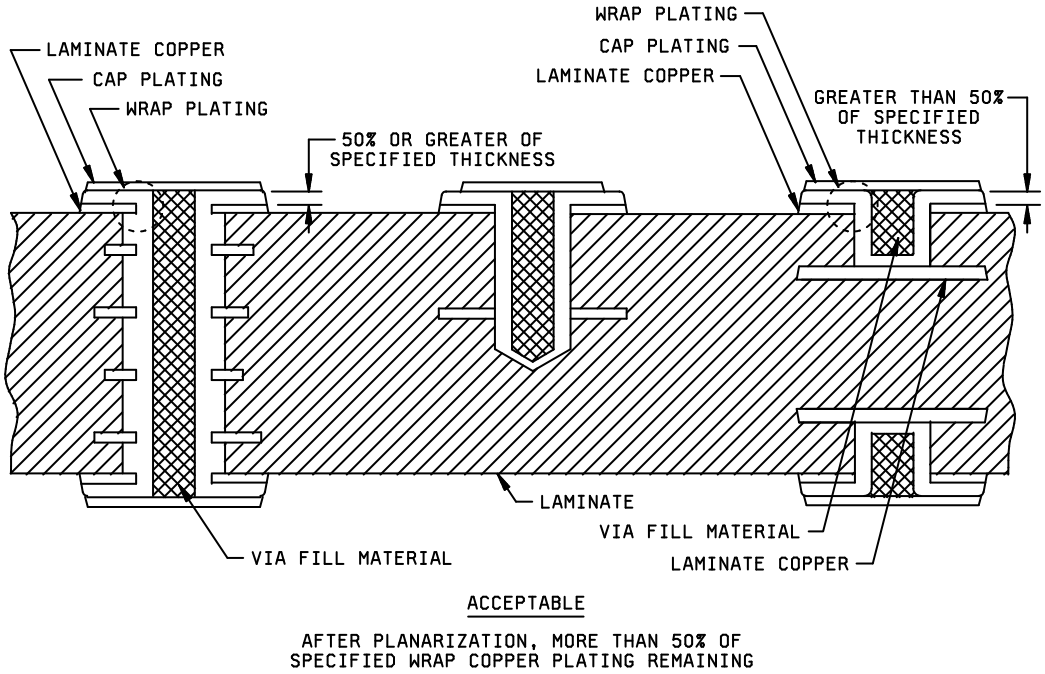


FIGURE G–13. Acceptable planarized plated hole structure wrap copper plating.

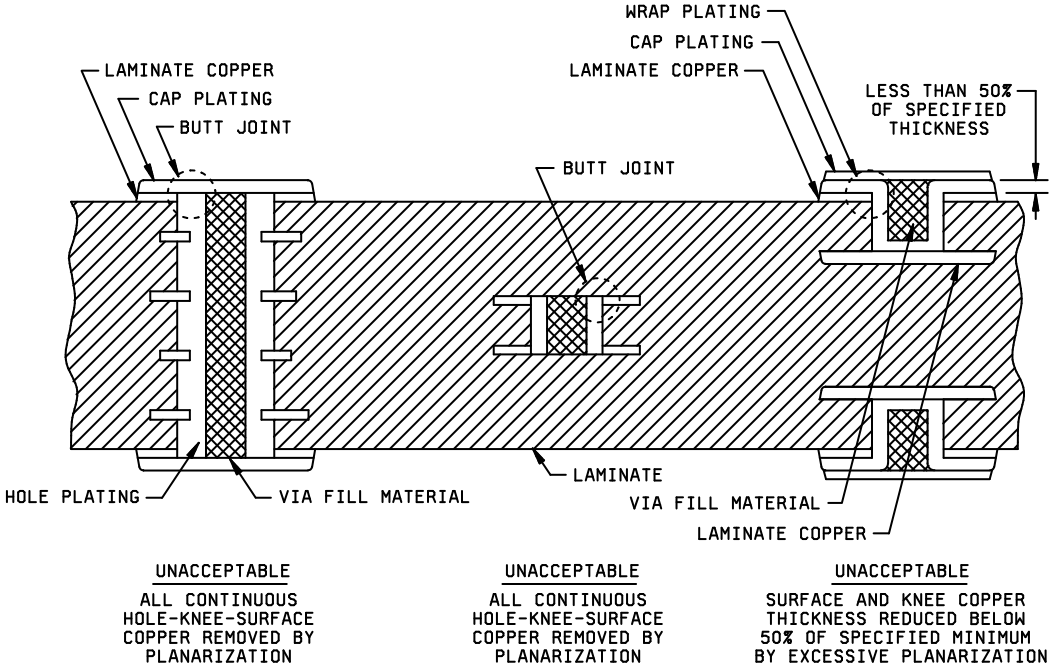


FIGURE G–14. Unacceptable planarized plated hole structure wrap copper plating.

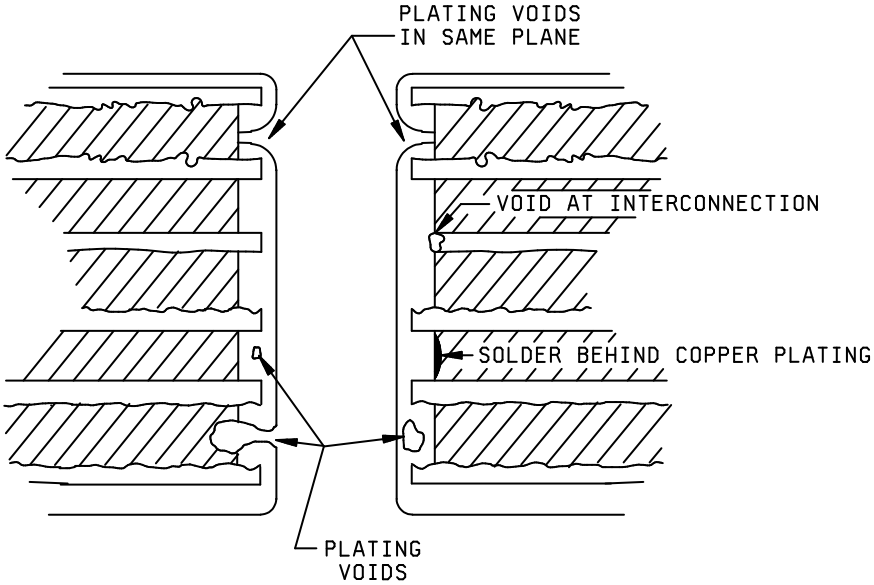


FIGURE G–15. Copper plating voids.

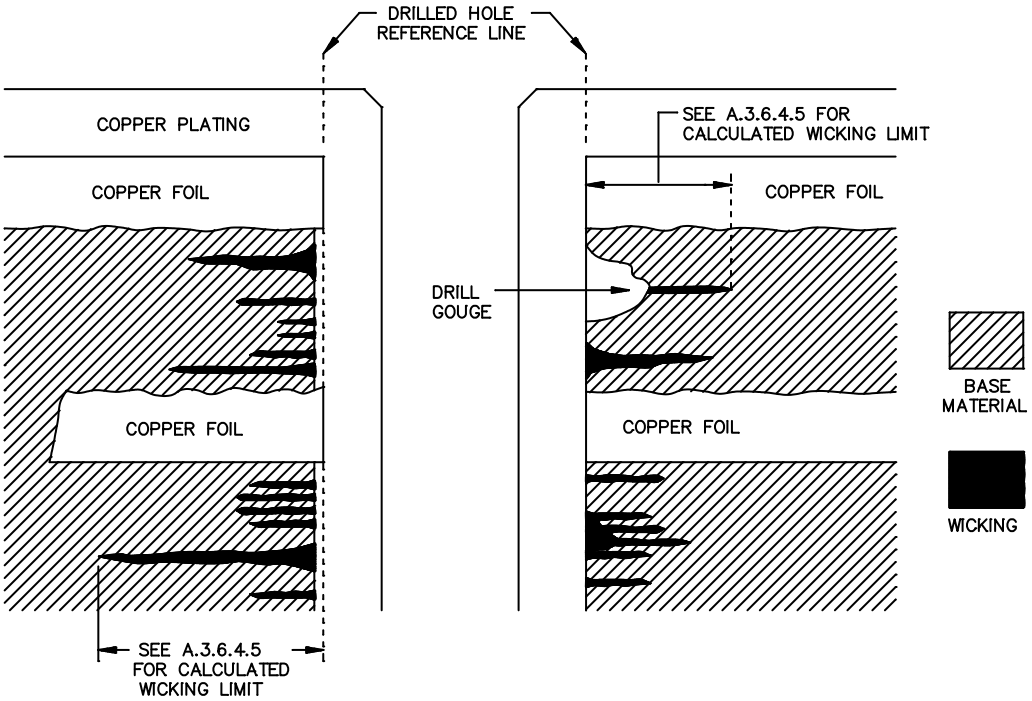


FIGURE G–16. Wicking of copper plating.

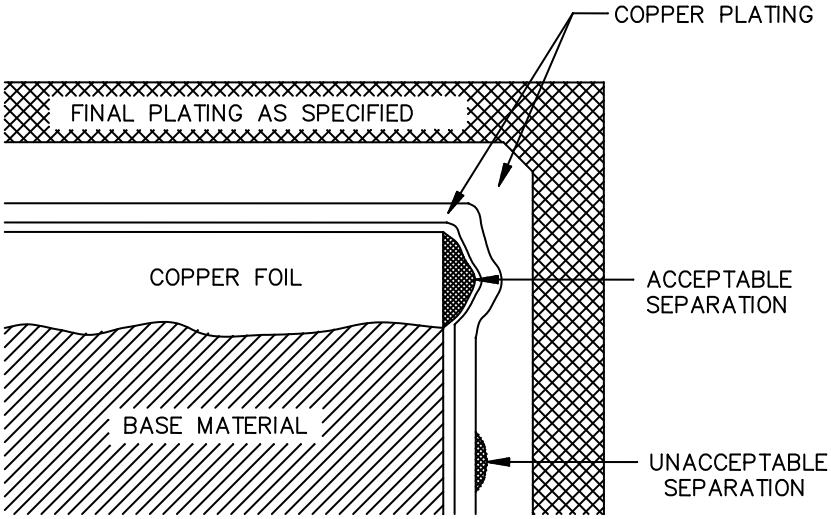


FIGURE G–17. Conductive interface separations.

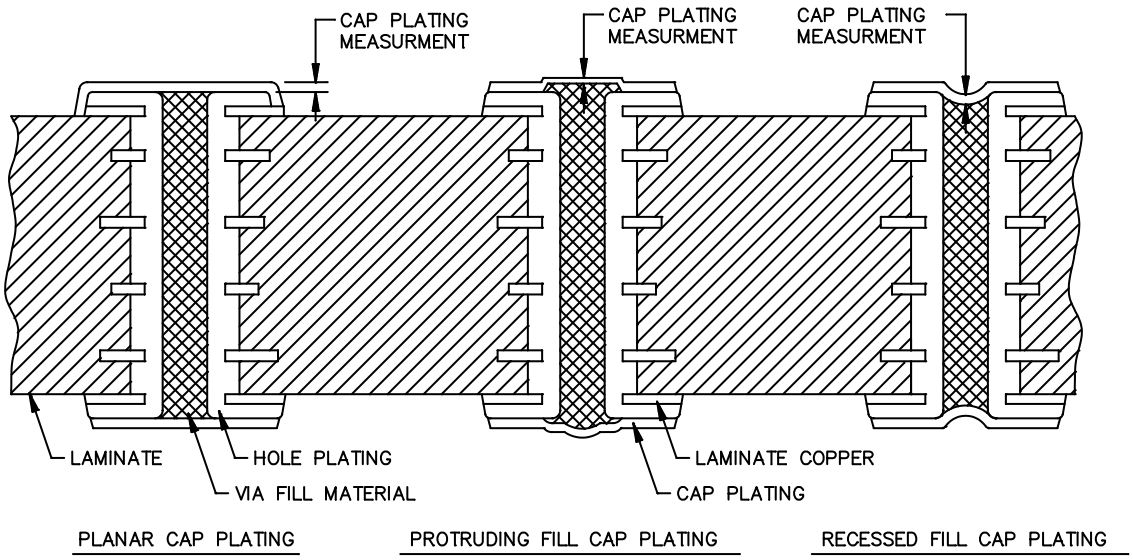


FIGURE G–18. Acceptable via cap plating.

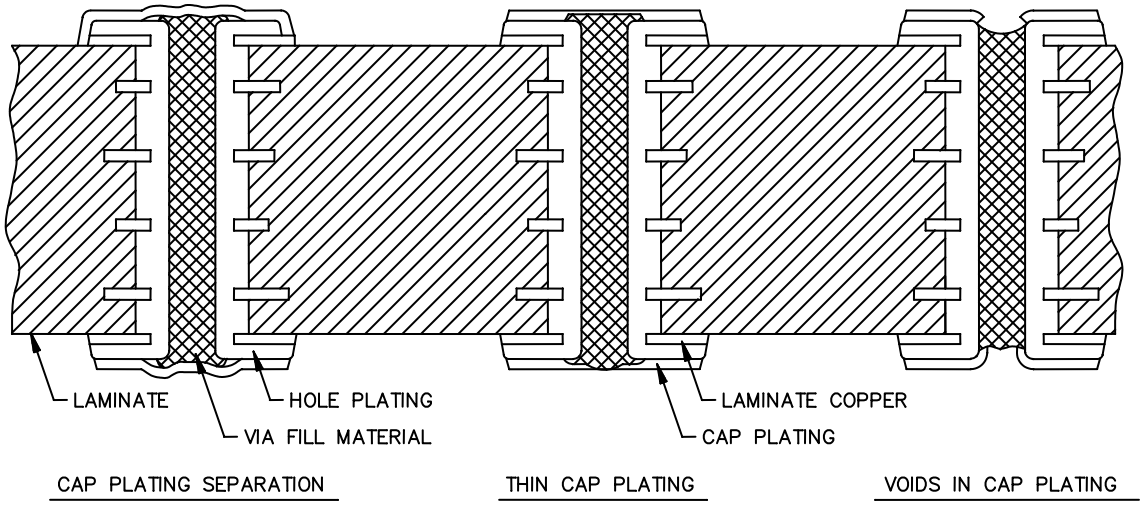


FIGURE G–19. Unacceptable via cap plating.

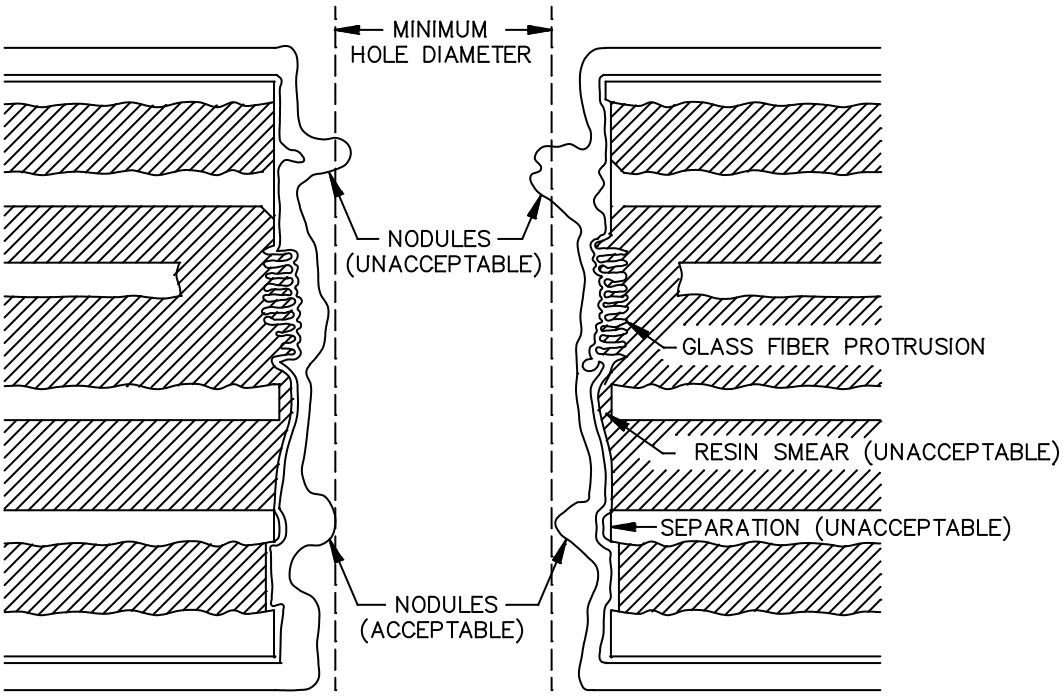
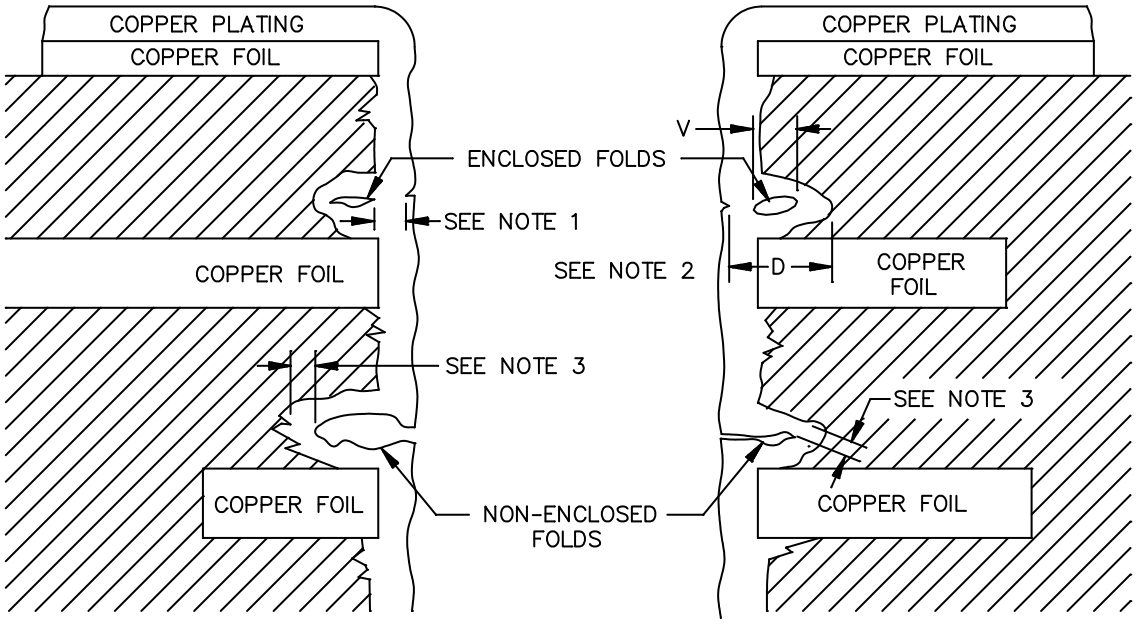


FIGURE G–20. Plated-through hole deficiencies.



NOTES:

1. Minimum copper plating thickness measurement point. Plating folds that are enclosed shall be acceptable if the minimum copper plating thickness is met.
2. Regions with the appearance of plating folds where there is no plating demarcation evident between the void and the inside edge of plating. Measure the distances between lines on inclusion and the overall . The dimension D minus dimension V shall meet the minimum copper plating thickness.
3. Minimum copper plating thickness measurement point. Plating folds that are not enclosed shall be acceptable if the minimum copper plating thickness is met.

FIGURE G–21. Plating fold evaluation.

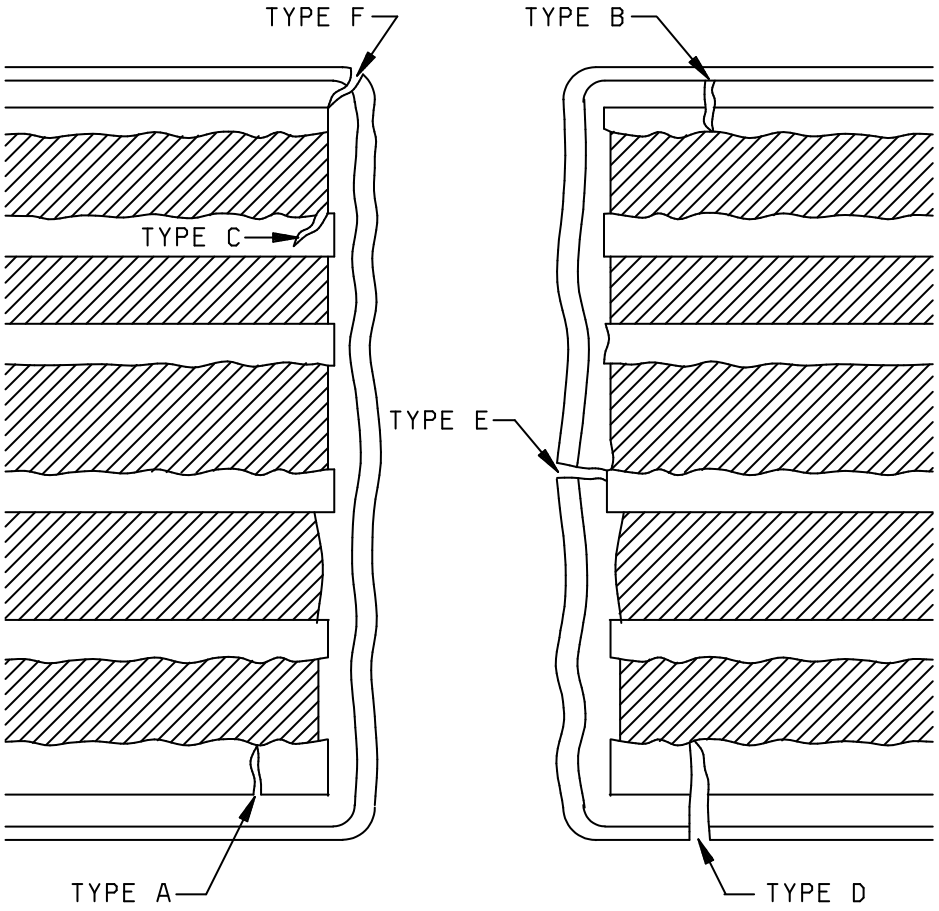


FIGURE G–22. Metallic cracks.

QUALITY CONFORMANCE TEST CIRCUITRY

H.1 SCOPE

H.1.1 Scope. This appendix contains requirements, information, and guidance concerning design standards IPC–2221 and IPC–2223. This appendix is a mandatory part of this specification for manufacturers using the QPL product assurance level of appendix A for printed wiring board verification. The information contained herein is intended for compliance.

H.2 APPLICABLE DOCUMENTS

H.2.1 General. The documents listed in this section are specified in sections H.3 and H.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections H.3 and H.4 of this specification, whether or not they are listed.

H.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50	–	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.
IPC–2221	–	Generic Standard on Printed Board Design.
IPC–2223	–	Sectional Design Standard for Flexible Printed Boards.
IPC–TM–650	–	Test Methods Manual.
IPC–100043	–	Master Drawing for 10 Layer Multilayer Printed Boards.
IPC–100044	–	Master Drawing for 4 Layer Multilayer Printed Boards.
J–STD–003	–	Solderability Tests for Printed Boards.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

H.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

H.3 QUALITY CONFORMANCE TEST CIRCUITRY (QCTC) REQUIREMENTS

H.3.1 General. Test coupons or QCTC strips shall be a part of every inspection panel on which printed wiring boards intended to be compliant to appendix A are fabricated. When test coupon retention is required for traceability it is recommended that an additional set of test coupons be combined into a common QCTC strip. Figure H–1 shows an example of QCTC strip location and placement concepts.

H.3.1.1 Panel location and placement of test coupons. Except for the "A" and "B" test coupons, the printed wiring board manufacturer may position the QCTC strip or individual test coupons to optimize panelization, tooling and material utilization. The location of the "A" and "B" test coupons shall be positioned no further than .5 inch (12.7 mm) of the printed wiring board profile and shall be closer to the panel corner than the QCTC strip identification, as displayed on figure H–1, in order to reflect fabrication and copper plating characteristics.

H.3.1.2 Performance and reliability verification test coupons. The recommended minimum number of test coupons that are required for performing the in-process, groups A, B, and C verifications of appendix A are specified in table H–I.

H.3.1.3 Process control and acquiring activity required test coupons. Test coupons of custom configuration used for process control or acquiring activity purposes may be added to the production panel. These custom configuration test coupons should incorporate features on the same dimensional plane to ensure compatibility with the required performance verification test coupons specified in table H–I. All applicable custom configuration test coupons shall be defined on the master artwork, the master drawing, or added to the production artwork by the manufacturer.

H.3.2 QCTC strip identification. When test coupons are ganged together in a QCTC strip, the strip shall contain space for QCTC strip identification and traceability marking. Unless otherwise specified, the minimum identification marking shall be as follows:

a. The printed wiring board part identification number (see A.3.8).

b. The manufacturer's Commercial and Government Entity (CAGE) code (see A.3.8.1).

c. The lot date code (see A.3.8.5).

d. The traceability code or identification (see A.3.9).

In addition, any acquiring activity specified special coding systems may be used, provided they are defined on the master drawing.

H.3.3 Using table H–I. The requirements for test coupon quantity and placement on the inspection panel are codified using a 4 digit dash number under the printed wiring board types of table H–I. The last column of table H–I uses a 2 digit code to specify the inspection group the test coupon is typically needed for. The codes for test coupon quantity on an inspection panel are specified in H.3.3.1. The codes for test coupon placement on an inspection panel are specified in H.3.3.2. The codes for test coupon inspection group usage are specified in H.3.3.3. An example of the 4 digit dash number is "1–ML". This dash number designates that a minimum of one test coupon of this type is required on the inspection panel and that its placement is the manufacturer's option.

H.3.3.1 Test coupon quantity codes. The codes used to designate the test coupon quantity in table H–I shall be as follows:

1 – Minimum of one test coupon for this verification on each inspection panel.

2 – Minimum of two test coupons for this verification on each inspection panel.

3 – Minimum of three test coupons for this verification on each inspection panel.

4 – Minimum of four test coupons for this verification on each inspection panel.

– This test coupon is required on the inspection panel only if the performance characteristic represented by the design or construction technique used to fabricate the printed wiring boards is present on the printed wiring boards. The minimum number required needs to be determined by the number of inspection groups needing the test coupon for verification purposes.

H.3.3.2 Test coupon placement codes. The codes used to designate the test coupon placement in table H–I shall be as follows:

ML – The location of the test coupon on the inspection panel is the manufacturer's option.

DC – The location of the test coupon on the inspection panel shall be on opposite corners.

BS – The location of the test coupon on the inspection panel is the manufacturer's option. The test coupon shall be place on each external layer (top and bottom) of the inspection panel.

H.3.3.3 Test coupon inspection group usage codes. The code used to designate the inspection group usage of a test coupon in table H–I shall be as follows:

GA – This code designates that the test coupon is used during group A inspection.

GB – This code designates that the test coupon is used during group B inspection.

GC – This code designates that the test coupon is used during group C inspection.

GD – This code designates that the test coupon is used for process qualification or requalification.

GP – This test coupon is used during in-process inspection.

TABLE H–I. Test coupons on inspection panels.

Inspections (associated with the identified test coupon)		Test coupon identifier	Type 1	Type 2	Type 3	Type 4	Type 5	Inspection Group
Plating adhesion		C	2–ML	2–ML	2–ML	2–ML	2–ML	GP and GA
		M	#–ML	#–ML	#–ML	#–ML	#–ML	GP and GA
Solder mask	Standard	G	2–ML	2–ML	2–ML	2–ML	2–ML	GP and GA
	Tented vias	T		#–ML	#–ML	#–ML		GP and GA
Non-stressed specimens (microsection)		A	1–ML	1–ML	1–ML	1–ML	1–ML	GA
Resistance to soldering heat (microsection)		B	2–DC	2–DC	2–DC	2–DC	2–DC	GA
Non-stressed specimens and resistance to soldering heat 8/		AB–R	2–DC	2–DC	2–DC	2–DC	2–DC	GA
Solderability	Through hole 1/	A		4–ML	4–ML	4–ML		GA
	Through hole 1/	S		1–ML	1–ML	1–ML		GA
	Surface mount	M	#–BS	#–BS	#–BS	#–BS	#–BS	GA
Adhesion, coverlayer		G 2/	1–ML	1–ML	1–ML		1–ML	GA
Adhesion, legend		3/	1–ML	1–ML	1–ML	1–ML	1–ML	GA
Resistance to solvents 4/		3/ 5/	3–ML	3–ML	3–ML	3–ML	3–ML	GA or GB
Rework simulation (through hole)		A	1–ML	1–ML	1–ML	1–ML	1–ML	GB
Insulation resistance 6/		E	2–ML	2–ML	2–ML	2–ML	2–ML	GB
Surface peel strength 7/		P			2–BS	2–BS		GB
Folding flexibility		X	1–ML	1–ML	1–ML	1–ML	1–ML	GB or GC
Flexibility endurance		X	1–ML	1–ML	1–ML	1–ML	1–ML	GC
Thermal shock		D	#–ML	#–ML	#–ML	#–ML	#–ML	GD

1/ Either one "S" or four "A" test coupons are needed on the inspection panel for solderability testing. The through–hole solderability test requires that 30 holes be inspected. One "S" coupon has 40 holes and four "A" test coupons will yield a total of 36 holes for the inspection.
2/ See H.4.3.6 for test specimen details.
3/ See H.4.3.7 for test specimen details.
4/ Test method number 2.3.4 of IPC–TM–650 designates that three solutions shall be used for testing marking. Either one test specimen can be used for each solution (three total specimens needed) or one test specimen can be subjected to all three solutions.
5/ See H.4.3.5 for alternate test coupon design.
6/ See H.4.3.5 for alternate test coupon design.
7/ See A.4.8.4.11 for sampling details.
8/ Optional test coupon that can be used in lieu of test coupons "A" and "B". See H.4.3.9 for alternate test coupon design.

H.4 TEST COUPONS AND TEST SPECIMENS

H.4.1 General test coupon requirements. Individual test coupons shall be designed to evaluate specific individual characteristics of the printed wiring boards they represent. Variations in specified test coupon design shall meet the intent of the original design and be representative of the printed wiring board. The test coupons shall reflect the design of the printed wiring boards in regards to the plated–through holes, conductor patterns, spacings, and other characteristics that are to be evaluated on the specific test coupon.

H.4.2 Process control test coupons. When test coupons are used to establish process control parameters, they shall consistently use a single hole size or land configuration which reflects the process used. The process characteristics and general printed wiring board characteristics should be matched (for example, threshold technology or leading edge technology) by the test coupons.

H.4.3 Designs and placement. The following test specimen configurations and designs shall be used to verify printed wiring boards to the requirements of appendix A.

H.4.3.1 Test specimens for the verification of resistance to solvents (see A.4.8.3.2).

H.4.3.1.1 Design of test specimens used for resistance to solvents. The printed wiring board test specimens for the resistance to solvents verification can be either portions or whole production printed wiring boards, quality conformance test circuitry strip identification areas containing ink, or paint marking.

H.4.3.1.2 Panel placement. The printed wiring test specimens shall be placed on the inspection panel where space is available.

H.4.3.2 Test specimens for the verification of flexibility endurance (see A.4.8.4.7). This printed wiring test specimen is used to evaluate the ability of flexible printed wiring boards to withstand dynamic flexing forces.

H.4.3.2.1 Designs of test specimens used for flexibility endurance. The design or the printed wiring board test specimens for the flexibility endurance verification shall be one of the following:

a. A suitable portion of a single or double sided production flexible printed wiring board.

b. The test coupon specified in test method number 2.4.3 of IPC–TM–650 (see table H–I).

H.4.3.2.2 Panel placement. The printed wiring board test specimens shall be placed on the inspection panel where space is available.

H.4.3.3 Test specimens for the verification of folding flexibility (see A.4.8.4.8). This printed wiring test specimen is used to evaluate the folding ability of stack up combinations of flexible dielectric materials and metallic foils.

H.4.3.3.1 Designs of test specimens used for folding flexibility. Folding flexibility shall be evaluated using any of the following test specimen designs:

a. A suitable portion of a production multilayer rigid–flex printed wiring board.

b. Test coupon H–1, H–2, H–3, H–4, or H–5 as defined in IPC–100043 or IPC–100044.

c. Test coupon "X" specified in IPC–2221.

H.4.3.3.2 Panel placement. The printed wiring board test specimens shall be placed on the inspection panel where space is available.

H.4.3.4 Test coupons for the verification of conductor surface peel strength (see A.4.8.4.11). This printed wiring test specimen is used to evaluate the peel strength of metallic foils as the result of the foil lamination fabrication process.

H.4.3.4.1 Design of test specimens for verification of conductor surface peel strength. The design of this test coupon "P" is shown on figure H–2. The test coupon shall consist of a conductor that provides a minimum test length of 2 inches (50.8 mm) and a minimum conductor width of .125 inch (3.18 mm).

H.4.3.4.2 Panel placement. At least one test coupon "P" for each foil laminated side of the printed wiring board shall be placed on the inspection panel where space is available.

H.4.3.5 Alternate test coupon for the verification of moisture and insulation resistance (see A.4.8.6.1). Alternate design test coupon "E" is used to evaluate the moisture and insulation resistance of laminated base materials.

H.4.3.5.1 Design of alternate test coupon 'E'. The design of this alternate test coupon is shown on figure H–3. This test coupon can be used in lieu of the test coupon "E" specified in IPC–2221.

H.4.3.5.2 Panel placement. At least two alternate test coupons "E" shall be placed on the inspection panel where space is available.

H.4.3.6 Test coupons for the verification of coverlayer adhesion (see A.4.8.4.1).

H.4.3.6.1 Design of test specimen for coverlayer adhesion. The test specimens can be either a production printed wiring board or a portion of a production printed wiring board.

H.4.3.6.2 Panel placement. At least one test coupon "G", for each side of the printed wiring board with cover layers shall be placed on the inspection panel where space is available.

H.4.3.7 Test coupons for the verification of adhesion, legend, and marking (see A.4.8.4.2).

H.4.3.7.1 Design of test specimen for legend and marking adhesion. The test specimens can be either a production printed wiring board, a portion of a production printed wiring board, or a quality conformance test circuitry strip identification areas containing ink or paint marking.

H.4.3.7.2 Panel placement. The placement of the test specimen on the inspection panel shall be where space is available.

H.4.3.8 Alternate test coupon for the verification of registration (see A.3.7.2.2.2 and A.4.8.2.4.2).

H.4.3.8.1 Design of alternate registration test coupon. There are at least two test coupon designs for evaluating registration using non-destructive methods. The designs are as follows:

a. Test coupon "F" (etch factor not needed) as specified in IPC–2221.

b. Test coupon "R" (etch factor of each layer needed) as specified in IPC–2221.

If other registration test coupon designs and requirements are provided as an element of the design documentation set, registration can be evaluated in accordance with the criteria specified on the applicable master drawing.

H.4.3.8.2 Panel placement. When using non-destructive registration in lieu of destructive evaluation of registration, at least one non-destructive registration test coupons shall be placed on the inspection panel where space is available.

H.4.3.9 Alternate test coupon for the verification of structural integrity of plated holes. This test coupon can be used in lieu of test coupon "A" or "B" specified in IPC–2221.

H.4.3.9.1 Design of alternate test coupon 'AB–R'. The layout of this alternate test coupon is shown on figure H–4.

H.4.3.9.2 Panel placement. The alternate test coupon "AB–R" shall be placed on the inspection panel in place of "A" and "B" test coupons.

H.4.3.9.3 Description of test coupon 'AB–R'. A description and brief explanation of the features available on test coupon "AB–R" is as follows:

a. Holes identified as A. These holes are to represent the largest component hole using a pad less than or equal to .0787 inch (2.0 mm) with its smallest associated drill. The holes have round pads present on all layers.

b. Holes identified as B. These holes are to represent the smallest via using a pad less than or equal to .039 inch (1.0 mm) with its smallest associated drill. The holes are differentiated into four categories as follows:

    1. B1 has round pads on layers 2 and n – 1.

    2. B2 has round pads on signal layers.

    3. B3 has round pads on plane layers.

    4. B4 has square pads on all layers. A line width and spacing check is located in-line with B4 pads based on individual layer features.

c. Holes identified as C. These holes are to represent the smallest via or component hole using a pad less than or equal to .0787 inch (2.0 mm) with its smallest associated drill. These holes have round pads on all layers.

d. Holes identified as R. These holes are used to evaluate registration features. The holes are differentiated into four categories as follows:

    1. RA holes are based on holes identified as A design features.

    2. RB holes are based on holes identified as B design features.

    3. RB-1 holes are based on holes identified as B design features minus .0254 inch (1.0 mm).

    4. RC holes are based on holes identified as C design features.

e. Holes identified as T. These holes are tooling holes. The size of the tooling holes are .0787 inch (2.0 mm). These tooling holes have a plane layer anti-pad of .1037 inch (2.635 mm) and solder mask anti-pad of .0866 inch (2.2 mm).

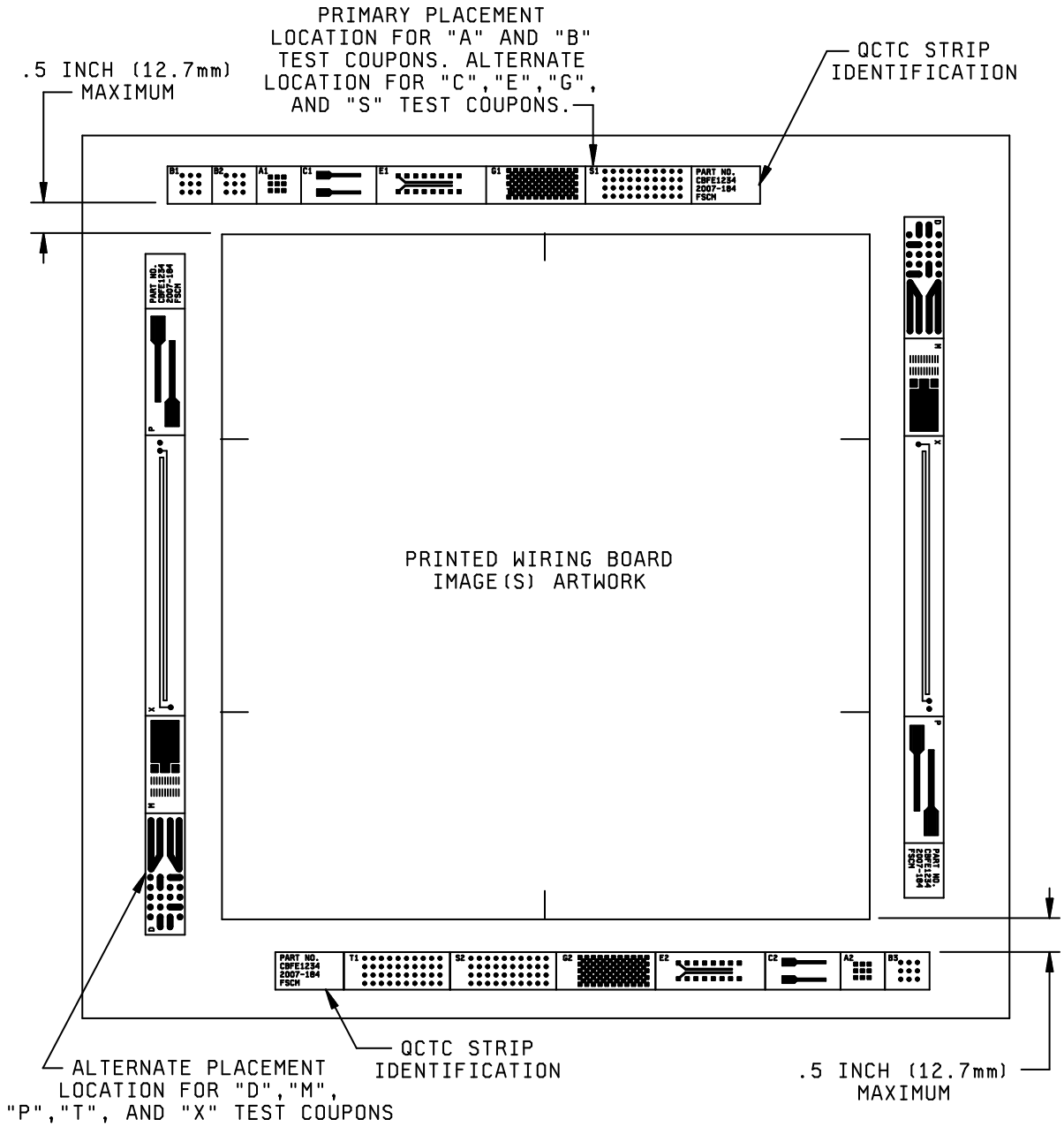
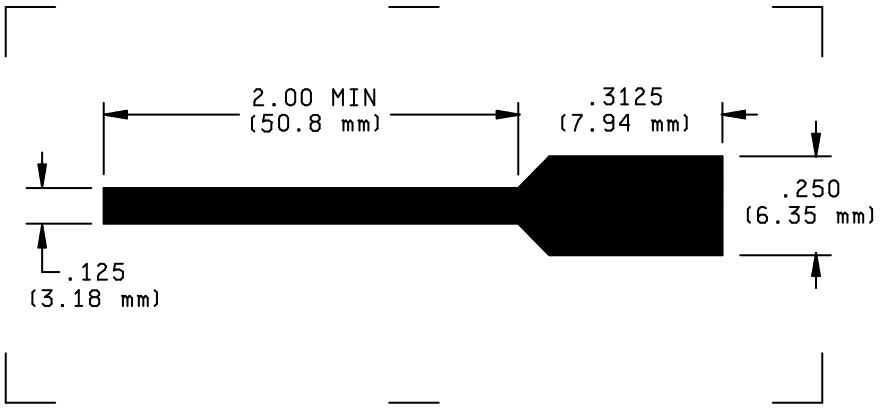


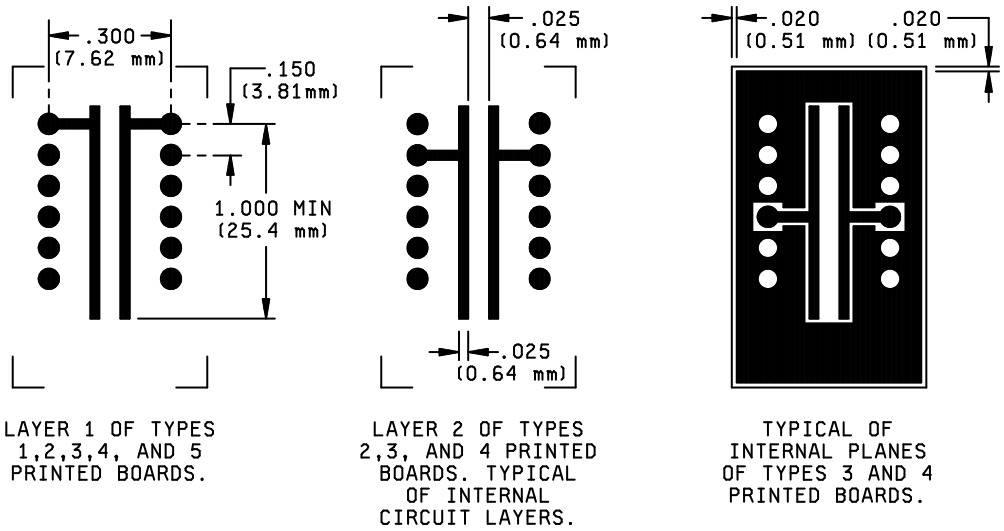
FIGURE H–1. Panel location of quality control test circuitry.



NOTES:

1. Dimensions are in inches. Millimeters are given for information only.
2. Unless otherwise specified, tolerances are for ±.02 inch (0.51 mm) for two place decimals and ±.010 inch (0.25 mm) for three place decimals.

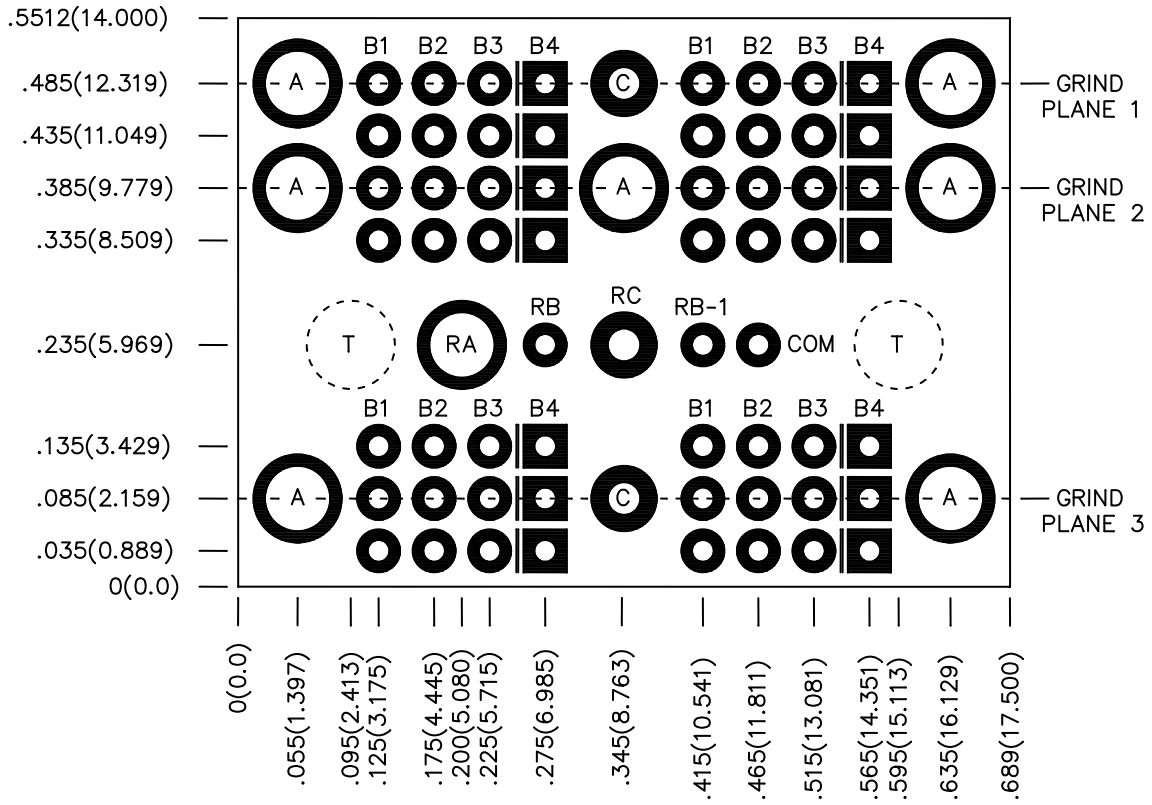
FIGURE H–2. Test coupon P.



NOTES:

1. Dimensions are in inches. Millimeters are given for information only.
2. Unless otherwise specified, tolerances are for ±.02 inch (0.51 mm) for two place decimals and ±.010 inch (0.25 mm) for three place decimals.

FIGURE H–3. Alternate design for test coupon E.



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Holes identified as A are used to evaluate the largest component holes of the printed board design.
3. Holes identified as B1, B2, B3, and B4 are used to evaluate the smallest via holes of the printed board design.
4. Holes identified as C are used to evaluate the smallest component holes of the printed board design.
5. Holes identified as RA, RB, and RC are used for evaluating registration.
6. Holes identified as T are tooling holes.

FIGURE H–4. Alternate design for test coupon A and B (test coupon AB–R).

H.5 NOTES

H.5.1 Discussion. Test coupons used for verification inspections and testing, when required, shall be in accordance with this appendix. Quality assurance provisions often require the use of specific test procedures or evaluations to determine if a particular design of a printed wiring board meets the requirements of the design activity and the specification. Some of the verification inspections are performed visually and are non-destructive, while others are only capable through destructive testing and destructive evaluations. Some quality evaluations are performed on test coupons because the test is destructive or the nature of the test requires a specific structure or configuration which may not exist on the printed wiring board.

Test coupons are used in these types of inspections as representatives of the printed wiring boards fabricated on the same panel. In many cases, a test coupon is a suitable printed wiring board test specimen for physical destructive analysis, or testing, since it has been subjected to the same manufacturing processes as the printed wiring boards on the panel. However, the design of the test coupons and their location on a panel are critical in order to ensure that the test coupons are truly representative of the printed wiring boards they represent. A production printed wiring board may be used for destructive tests. Tests requiring specific conductor pattern configuration (for example, insulation resistance) may also be performed on production printed wiring boards if appropriate conductor patterns are included in the design of the printed wiring board.

Custodians:
Army – CR
Navy – EC
Air Force – 85
DLA – CC

Review activities:
Army – AR, MI
Navy – AS, MC, OS, SH
Air Force – 16, 99

Preparing activity:
DLA – CC

(Project 5998–2015–018)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.