The documentation and process conversion measures necessary to comply with this document shall be completed by 10 March 2025.

INCH-POUND

MIL-PRF-19500/761B
w/AMENDMENT 2
9 October 2024
SUPERSEDING
MIL-PRF-19500/761B
w/AMENDMENT 1
26 January 2023

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, TYPE 1N7069, QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a silicon, Schottky single power rectifier diode for use in high frequency switching power supplies and resonant power converters. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each device type.

1.2 Package outlines. The device package outline is a three terminal flange mount header TO-254AA (T1 suffix) in accordance with figure 1.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25 °C.

Column 1	Column 2	Column 3	Column 4	Column 5	Column 6
Types	V_{RWM}	I_O (1) T_C = +100 °C	I_{FSM} t_p = 8.3 ms T_C = +25 °C	$R_{\theta JC}$ (2)	T_{STG} and T_J
	V dc	A dc	A (pk)	°C/W	°C
1N7069T1	100	35	270	1.1	-65 to +150

(1) See temperature-current derating curves on figure 2.
(2) See thermal impedance curves on figure 3.

1.4 Primary electrical characteristics. $R_{\theta JC}$ = 1.1 °C/W maximum; $R_{\theta JA}$ = 50 °C/W maximum.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A
FSC 5961

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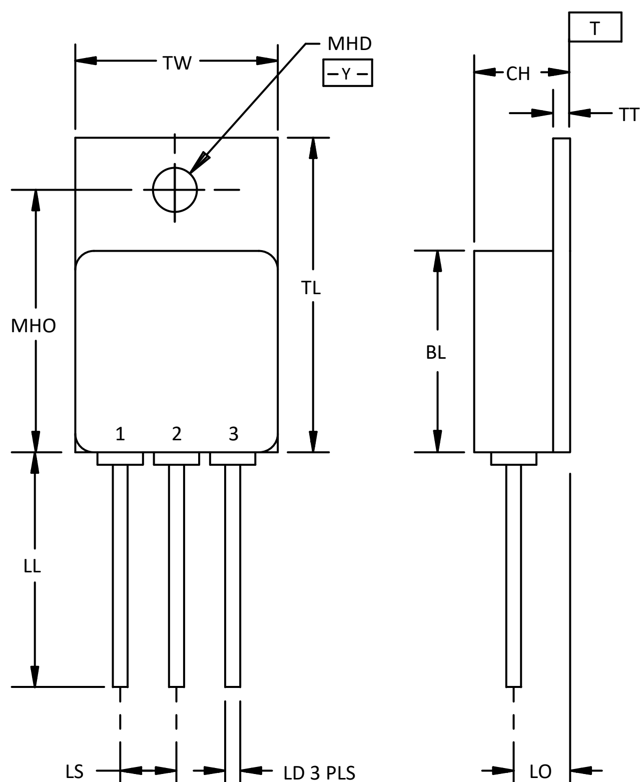


Symbol	Dimensions			
	Inches	Inches	mm	mm
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84

INTERNAL SCHEMATIC

TERM 1 = CATHODE
TERM 2 = N/C
TERM 3 = ANODE

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Protrusion of ceramic eyelets included in dimension LL.
3. All terminals are isolated from case.

FIGURE 1. Dimensions and configuration three terminal flange mount header TO-254AA package.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet are identified by the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows: "7069".

1.5.3 Suffix symbols. The suffix symbols "T1" are used on devices that are packaged in the TO-254AA package of figure 1.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 − Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 − Test Methods for Semiconductor Devices.
* MIL-STD-883 - Test Methods Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 herein. See 6.7 regarding information regarding lead material requirements of previous revisions.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation, material, or finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Lead formation (TO-254 packages only). Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein after the formation.

3.4.3 Lead isolation (TO-254 packages only). Methods used for electrical isolation of the terminal feed through shall employ materials that contain a minimum of 90 percent ceramic AL_2O_3 or equivalent. Examples of such construction techniques are metalized ceramic eyelets or ceramic walled packages.

3.4.4 Polarity. Polarity and terminal configuration shall be in accordance with figure 1 herein.

* 3.4.5 Silicone die coating. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883, on each lot of silicone die coating for its intended applications.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.3 Silicone die coating. When silicone die coating is used, method 5011 of MIL-STD-883 shall be performed on that coating in the full MIL-PRF-19500 qualification process.

4.3 Screening (quality levels JANS, JANTXV, and JANTX only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTX and JANTXV levels
3b	Surge current (see 4.3.4)	Surge current (see 4.3.4)
3c	Thermal impedance (see 4.3.2).	Thermal impedance (see 4.3.2).
3d	Avalanche energy test (see 4.3.3).	Avalanche energy test (see 4.3.3).
* 5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.5)	Not applicable
9, 10	Not applicable.	Not applicable.
11	V_{F1} and I_{R1}	V_{F1} and I_{R1}
12	t = 240 hours minimum. See 4.3.1.	t = 48 hours minimum. See 4.3.1.
13	Subgroup 2 and 3, of table I herein, V_{F1} and I_{R1}; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ±100 percent from the initial value or ±36 μA, whichever is greater.	Subgroup 2, of table I herein; V_{F1} and I_{R1}; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ±100 percent from the initial value or ±36 μA, whichever is greater.

4.3.1 High temperature reverse bias. The high temperature reverse bias shall be performed in accordance with test condition A of method 1038 of MIL-STD-750. Reverse bias conditions shall be as follows: V_R = 80 V dc; T_J = +125 °C.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, and t_{MD}. See table III, subgroup 4, and figure 3 herein.

4.3.3 Avalanche energy test. The avalanche energy test shall be performed in accordance with method 4064 of MIL-STD-750 using the circuit as shown on figure 4 or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: I_{AS} = 1A, V_{BR} = 100 V minimum.

4.3.4 Surge current. The surge current test shall be performed in accordance with condition A of method 4066 of MIL-STD-750. The following details shall apply: I_O = 0; V_{RWM} = 0; I_{FSM} = rated I_{FSM} (see column 4 of 1.3); one pulse, tp = 8.3ms.

* 4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (for quality level JANS) and E-VIB (for quality levels JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Delta measurements shall be in accordance with table II herein.

4.4.2.1 Quality level JANS (table E-VIA of MIL-PRF-19500).

Subgroup	Method	Condition
B4	1037	ΔT_C = +85 °C, I_F = 2 A minimum.
B5	1038	Condition A, V_R = 80 V dc, T_J = +125 °C, t = 340 hours min; heat sinking allowed. This test shall be extended to 1,000 hours on each JANS wafer lot.

4.4.2.2 Quality levels JAN, JANTX and JANTXV (table E-VIB of MIL-PRF-19500).

	Subgroup	Method	Condition
	B3	1037	ΔT_C = +85 °C, I_F = 2 A minimum.
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Delta measurements shall be in accordance with table II herein.

	Subgroup	Method	Condition
	C2	2036	Condition A, weight = 10 lbs (4.54 kg), t = 15 seconds.
*	C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	C5	4081	Limit for thermal resistance for 1N7069T1 is 1.1 °C/W.
	C6	1037	ΔT_C = +85 °C, I_F = 2 A minimum.
	C6	1038	Condition A, V_R = 80 V dc, T_J = +125 °C, t = 1,000 hours minimum; heat sinking allowed (for quality levels TX and TXV only).

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table III herein. Delta measurements shall be in accordance with table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3101	See 4.3.2	$Z_{\theta JC}$			°C/W
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 35 (pk)	V_{F1}		1.05	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 70 (pk)	V_{F2}		1.52	V dc
Reverse current	4016	Condition A or B; V_R = 100 V	I_{R1}		36	µA dc
Subgroup 3						
High temperature operation:		T_C = +125 °C				
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 8 A (pk)	V_{F3}		1.0	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 16 A (pk)	V_{F4}		1.47	V dc
Reverse current	4016	Condition A or B; V_R = 100 V	I_{R2}		28	mA dc
Low temperature operation:		T_C = -55 °C				
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 35 A (pk)	V_{F5}		1.0	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, I_F = 70 A (pk)	V_{F6}		1.42	V dc
Subgroup 4						
Junction capacitance	4001	V_R = 5 V dc, f = 1 MHz, V_{SIG} = 50 mV (p-p)	C_J		1,375	pF

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	Condition A, see 1.3, column 4 herein, ten surges. 60 seconds between surges, (see 4.5.1)				
Electrical measurements		See table I, subgroup 2 herein				
Subgroup 7						
Dielectric withstanding voltage	1081	V_R = 500 V dc; all leads shorted; measure from leads to case	I_{DWV}		10	µA
Scope display evaluation	4023	Condition A (stable only)				
Electrical measurements		See table I, subgroup 2 herein.				

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3, 4, and 5 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Delta measurements for groups B, C, and E. 1/ 2/ 3/ 4/ 5/

Step	Inspection	MIL-STD-750		Symbol	Limits	Limits	Unit
		Method	Conditions		Min	Max	
1	Forward voltage	4011	Condition B, pulsed (see 4.5.1) I_F = 35 A (pk)	ΔV_{F1}	±50 mV dc from initial reading.		
2	Reverse current	4016	Condition A or B, V_R = 100V	ΔI_{R1}	±100 percent from initial reading or ±36 μA whichever is greater.		

1/ The delta measurements taken during group B inspection for quality level JANS (table E-VIA of MIL-PRF-19500) shall be as follows:
  a. In addition to the measurements specified for subgroup 4, the measurements of steps 1, and 2 shall also be taken.
  b. In addition to the measurements specified for subgroup 5, see table II herein, the measurements of steps 1 and 2 shall also be taken.

2/ The delta measurements taken during group B inspection for quality levels JAN, JANTX and JANTXV (table E-VIB of MIL-PRF-19500) shall be as follows:
  a. In addition to the measurements specified for subgroup 2, the measurements of steps 1, and 2 shall also be taken.
  b. In addition to the measurements specified for subgroup 3, the measurements of steps 1, and 2 shall also be taken.
  c. In addition to the measurements specified for subgroup 6, the measurements of steps 1 and 2 shall also be taken.

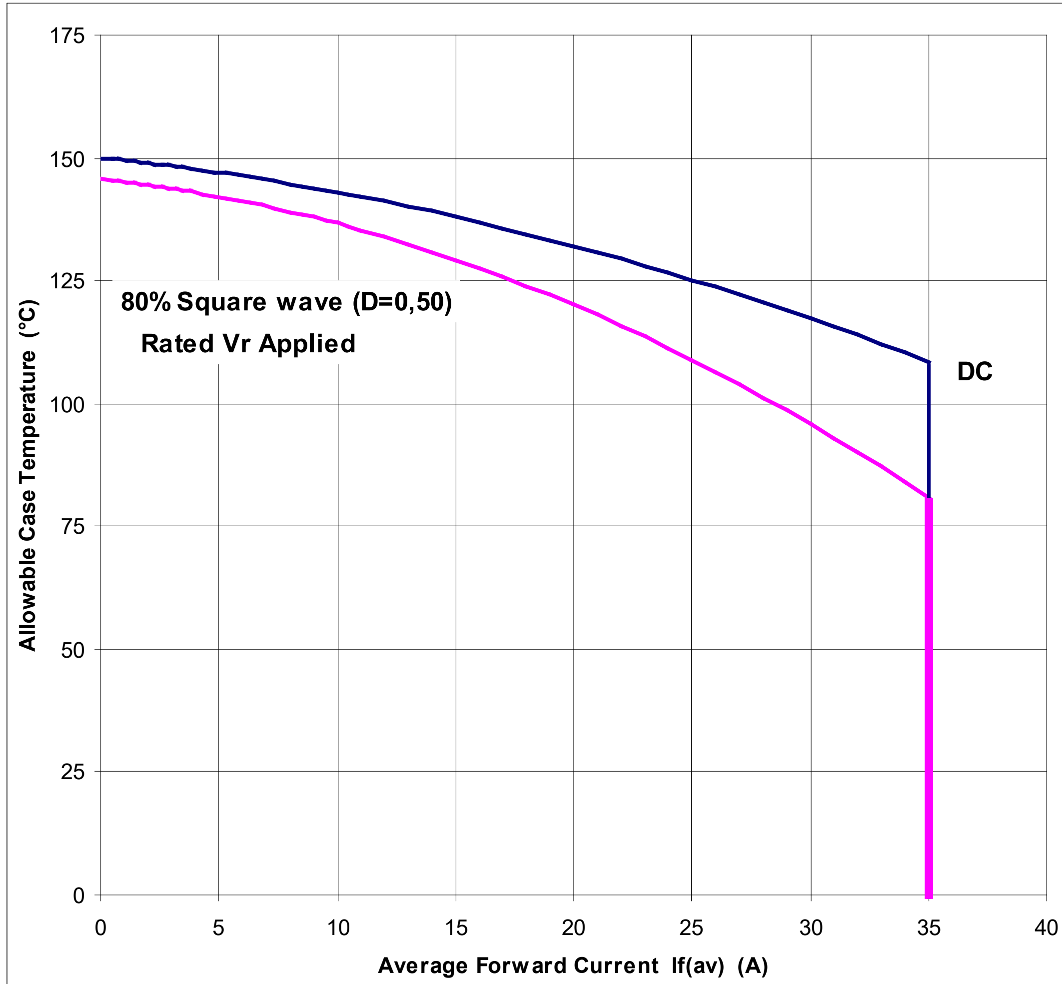
3/ The delta measurements taken during group C inspection for all quality levels (table E-VII of MIL-PRF-19500) shall be as follows:
  a. In addition to the measurements specified for subgroups 2 and 3, the measurements of steps 1, and 2 shall also be taken for all levels.
  b. In addition to the measurements specified for subgroup 6, the measurements of steps 1, and 2 shall also be taken for all levels.

4/ The delta measurements taken during E inspection for all quality levels (table E-IX of MIL-PRF-19500) shall be as follows:
  a. In addition to the measurements specified for subgroup 1, the measurements of steps 1, and 2 shall also be taken.
  b. In addition to the measurements specified for subgroup 2, the measurements of steps 1 and 2 shall also be taken.

5/ Devices which exceed the table I limits for this test shall not be accepted.

TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices, c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55 °C to +150 °C.	
Hermetic seal	1071	Fine and gross leak.	
Electrical measurements		See table I, subgroup 2 and table II herein.	
Subgroup 2			45 devices, c = 0
Life test	1048	t = 1,000 hours, T_J = +125 °C, V_R = 80 percent rated voltage (see 1.3, column 2 herein).	
Electrical measurements		See table I subgroup 2 and table II herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 10			5 devices, c = 0
Surge current	4066	Condition A, T_A = +25 °C, I_{FSM} = 270 A, 100 surges of 8.3 ms half sine wave. V_R = 0; I_O = 0 A pk.	
Electrical measurements		See table I subgroup 2 (V_F and I_R only).	

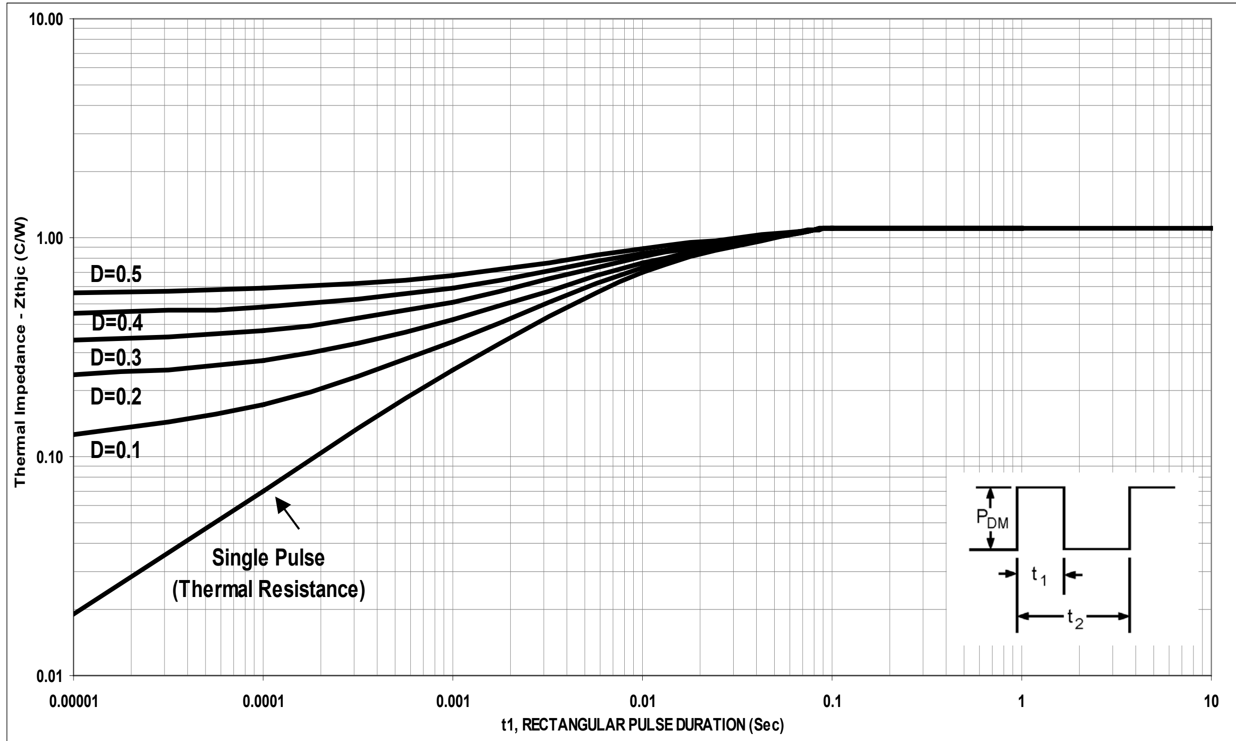


Switch mode operation, 80 percent duty cycle: T_C (°C) (case).
$R_{\theta JC}$ = 1.1 °C/W.

NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 150 °C) and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 125 °C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125 °C, and 110 °C to show current rating where most users want to limit T_J in their application.

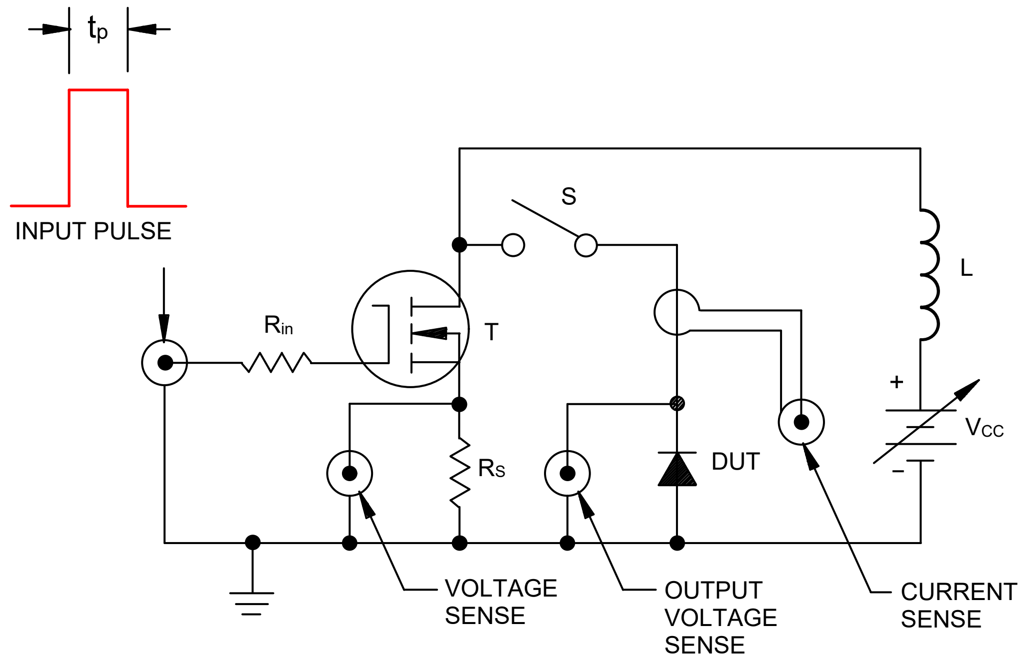
FIGURE 2. Temperature-current derating curve (entire package) for 1N7069T1.



NOTES:

1. Duty factor $D = t_1 / t_2$
2. Peak $T_J = P_{DM} \times Z_{\theta JC} + T_C$

FIGURE 3. Thermal impedance curves for 1N7069T1.



PROCEDURE:
1. With S open, adjust pulse width to test current of 1 amps across R_S.
2. Close S, verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

NOTES:
1. The following input pulse details shall apply: V_G = 10 Volts, P.W. ≈ 30 μs, duty cycle ≤ 1 percent.
2. The following test circuit component values shall apply: L = 100 μH, Z_G = 50 ohms, R_{in} = 50 ohms, 1 watt, R_S = 0.1 ohms, 1 watt, T = 2N6768 (IRF350 or equivalent).
3. The supply voltage V_{CC} ≈ 10 volts.

FIGURE 4. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service’s system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

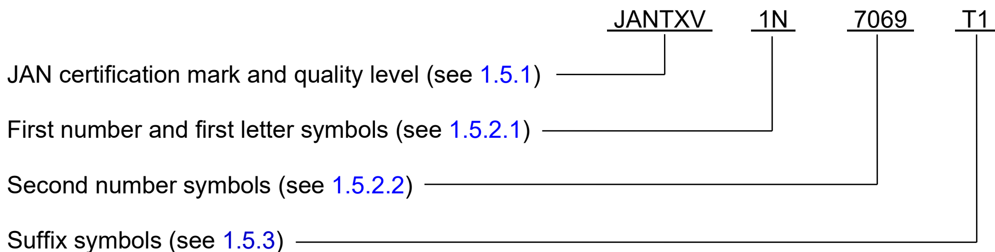
b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1), and if applicable, any needed lead formation (see 3.4.2).

d. The complete PIN, see 1.5 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N7069T1	JANTX1N7069T1	JANTXV1N7069T1	JANS1N7069T1

6.6 Cross reference substitution list. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
35GQ100	JANS, JANTXV, JANTX, JAN1N7069T1

6.7 Lead material. Because of the performance format of this document, lead material is no longer specified. Previous revisions of this specification specified that the wire terminal be constructed of "Kovar or Alloy 52". The requirements also specified that "a copper core or plated core is permitted".

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.9 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army − CR
Navy − SH
Air Force − 85
NASA − NA
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Preparing activity:
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(Project 5961-2024-075)

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