

The documentation and process conversion measures necessary to comply with this revision shall be completed by 20 April 2012.

INCH-POUND

MIL-PRF-19500/759A
 20 January 2012
 SUPERSEDING
 MIL-PRF-19500/759
 1 June 2011

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
 (TOTAL DOSE AND SINGLE EVENT EFFECTS)
 DUAL TRANSISTOR, N-CHANNEL AND P-CHANNEL, LOGIC-LEVEL SILICON
 TYPES 2N7632UD, JANTXVR, F, AND JANSR, F

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for dual N-channel and P-channel, enhancement-mode, low-threshold logic level, MOSFET, radiation hardened (total dose and single event effects(SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

* 1.2 Physical dimensions. See [figure 1](#), UD (LCC-6).

* 1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (free air) (1) $T_A = +25^\circ\text{C}$	$R_{\theta JA}$ (2)	$V_{DS} = V_{DG}$		V_{GS}		T_J and T_{STG}
			N-channel	P-channel	N-channel	P-channel	
2N7632UD	$\frac{W}{1.0}$ (each channel device)	$\frac{^\circ\text{C}/W}{125}$ (each N or P)	$\frac{V\text{ dc}}{100}$	$\frac{V\text{ dc}}{-100}$	$\frac{V\text{ dc}}{\pm 20}$	$\frac{V\text{ dc}}{\pm 20}$	$\frac{^\circ\text{C}}{-55\text{ to }+150}$

Type	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$		I_{D2} $T_C = +100^\circ\text{C}$		I_S		I_{DM} (5)	
	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel
2N7632UD	$\frac{A\text{ dc}}{0.92}$	$\frac{A\text{ dc}}{-0.65}$	$\frac{A\text{ dc}}{0.58}$	$\frac{A\text{ dc}}{-0.41}$	$\frac{A\text{ dc}}{0.92}$	$\frac{A\text{ dc}}{-0.65}$	$\frac{A\text{ (pk)}}{3.68}$	$\frac{A\text{ (pk)}}{-2.60}$

(See notes next page)

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* 1.3 Maximum ratings. - continued.

- (1) Derate linearly 0.008 W/°C (each channel) for T_C > +25°C.
- (2) See [figure 2](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 3](#), maximum drain current graph.
- (5) I_{DM} = 4 X I_{D1} as calculated in note (3).

* 1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 0.25mA dc		V _{GS(TH)1} V _{DS} ≥ V _{GS} I _D = 0.25 mA dc		Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent rated V _{DS}		Max r _{DS(on)} (1) V _{GS} = 4.5V, I _D = I _{D2}			
							T _J = +25°C		T _J = +150°C	
	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel
	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>μA dc</u>	<u>μA dc</u>	<u>Ω</u>	<u>Ω</u>	<u>Ω</u>	<u>Ω</u>
			<u>Min Max</u>	<u>Min Max</u>						
2N7632UD	100	-100	1.0 2.0	-1.0 -2.0	1	1	0.70	1.65	1.19	2.39

Type	E _{AS} @ I _{AS} =I _{D1} N-channel	E _{AS} @ I _{AS} =I _{D1} P-channel
	<u>mJ</u>	<u>mJ</u>
2N7632UD	19.3	34

- (1) Pulsed (see [4.5.1](#)).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

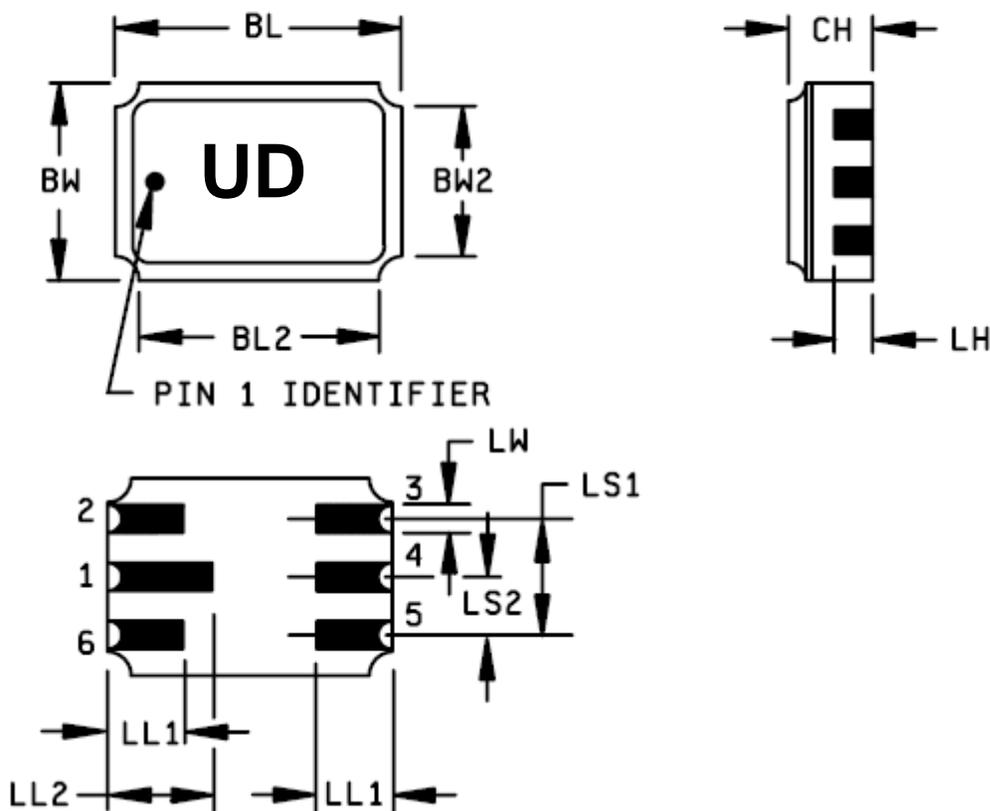
[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or <https://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Pin no.	Transistor
1	Drain no. 1
2	Gate no. 1
3	Gate no. 2
4	Drain no. 2
5	Source no. 2
6	Source no. 1

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL2		.250		6.35
BW	.165	.175	4.19	4.45
BW2		.175		4.45
CH	.044	.080	1.12	2.03
LH	.026	.039	0.66	0.99
LL1	.060	.070	1.52	1.78
LL2	.082	.098	2.08	2.49
LS1	.095	.105	2.41	2.67
LS2	.045	.055	1.14	1.40
LW	.022	.028	0.56	0.71

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. N is the quantity of terminal positions.
5. The package shall meet dimension A without solder.
Maximum allowable solder thickness is .006 inch (0.15 mm).
6. Applied solder to the terminals will increase flatness tolerance by additional .004 inch (0.10 mm).
7. Q1 is N-channel. Q2 is P-channel. All are un-committed.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Dimensions and configuration of leadless chip carrier (LCC-6).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and [figure 1](#) (UD) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#) herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced (see table III). End-point measurements shall be in accordance with table II.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein I _{DSS1} , I _{GSSF1} , I _{GSSR1} as minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} Subgroup 2 of table I herein. ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±0.2 μA dc or ±100 percent of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±0.2 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.	Subgroup 2 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±0.2 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a. JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 15$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS})..... I_{D1} .
- b. Peak gate voltage (V_{GS})..... 10 V dc (up to max rated V_{GS}).
- c. Gate to source resistor (R_{GS}) $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature $+25^{\circ}\text{C}$, $+10^{\circ}\text{C}$, -5°C .
- e. Inductance: $\left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 25 V dc (up to max V_{DS}).

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table III](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#), and herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated V_{GS} ; $T_A = +175^{\circ}\text{C}$, $t = 24$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated V_{DS} ; $T_A = +175^{\circ}\text{C}$, $t = 120$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 240$ hours minimum.
B5	2037	Test condition D.

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition C, 25 cycles.
B3	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated } V_{GS}$; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum; and accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated } V_{DS}$; $T_A = +175^\circ\text{C}$, $t = 170$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 340$ hours minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength is not applicable.
C5	3161	See 4.3.3 , $R_{\theta JA} =$ (see 1.3).
C6	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated } V_{GS}$; $T_A = +175^\circ\text{C}$, $t = 48$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 96$ hours minimum. and accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated } V_{DS}$; $T_A = +175^\circ\text{C}$, $t = 500$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 1,000$ hours minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in [table III](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u> 2N7632UD (N & P-channel)	3161	See 4.3.3	$Z_{\theta JC}$			$^{\circ}C/W$
Breakdown voltage drain to source 2N7632UD N-channel 2N7632UD P-channel	3407	$V_{GS} = 0 V$, bias condition C $I_D = 0.25 \text{ mA dc}$ $I_D = -0.25 \text{ mA dc}$	$V_{(BR)DSS}$	60 -60		V dc V dc
Gate to source voltage (threshold) 2N7632UD N-channel 2N7632UD P-channel	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.25 \text{ mA dc}$ $I_D = -0.25 \text{ mA dc}$	$V_{GS(TH)1}$	1.0 -1.0	2.0 -2.0	V dc V dc
Gate current 2N7632UD N-channel 2N7632UD P-channel	3411	Bias condition C, $V_{DS} = 0 V$ $V_{GS} = +10V \text{ dc}$ $V_{GS} = -10 V \text{ dc}$	I_{GSSF1}		+100 -100	nA dc nA dc
Gate current 2N7632UD N-channel 2N7632UD P-channel	3411	Bias condition C, $V_{DS} = 0 V$ $V_{GS} = -10 V \text{ dc}$ $V_{GS} = +10V \text{ dc}$	I_{GSSR1}		-100 +100	nA dc nA dc
Drain current 2N7632UD N-channel 2N7632UD P-channel	3413	$V_{GS} = 0 V$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		1 -1	$\mu A \text{ dc}$ $\mu A \text{ dc}$
Static drain to source on state resistance 2N7632UD N-channel 2N7632UD P-channel	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$ $V_{GS} = 4.5V \text{ dc}$ $V_{GS} = -4.5V \text{ dc}$	$r_{DS(ON)1}$		0.70 1.65	Ω Ω
Forward voltage 2N7632UD N-channel 2N7632UD P-channel	4011	$V_{GS} = 0 V$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2 -5.0	V dc V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation						
$T_C = T_J = +125^\circ\text{C}$						
Gate current	3411	$V_{GS} = \pm 20 \text{ V dc}$, bias condition C, $V_{DS} = 0 \text{ V}$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0 \text{ V dc}$, bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS2}			
2N7632UD N-channel					10	$\mu\text{A dc}$
2N7632UD P-channel					-10	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$ $V_{GS} = 4.5 \text{ V dc}$ $V_{GS} = -4.5 \text{ V dc}$	$r_{DS(ON)3}$			
2N7632UD N-channel					1.085	Ω
2N7632UD P-channel					2.230	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(TH)2}$			
2N7632UD N-channel		$I_D = 0.25 \text{ mA dc}$		0.5		V dc
2N7632UD P-channel		$I_D = -0.25 \text{ mA dc}$		-0.5		V dc
Low temperature operation						
$T_C = T_J = -55^\circ\text{C}$						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$	$V_{GS(TH)3}$			
2N7632UD N-channel		$I_D = 0.25 \text{ mA dc}$			3.0	V dc
2N7632UD P-channel		$I_D = -0.25 \text{ mA dc}$			-3.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = I_{D2}$, (see 4.5.1), $V_{DD} = 10 \text{ V dc}$ $V_{DD} = -10 \text{ V dc}$	gFS			
2N7632UD N-channel				0.5		S
2N7632UD P-channel				0.7		S
Gate series resistance	3402	Condition A	R_G			
2N7632UD N-channel					12	Ω
2N7632UD P-channel					78	Ω
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4. $t_p = 10 \text{ ms min.}$ $V_{DS} = 80 \text{ percent of max. rated } V_{DS}$				
Electrical measurements		See table I, subgroup 2				

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 6</u> Not applicable						
<u>Subgroup 7</u> Gate charge	3471	Condition B. $I_D = I_{D2}$, $V_{DD} = 50$ percent of rated V_{DS} $V_{GS} = 4.5$ V dc (N-channel); $V_{GS} = -4.5$ V dc (P-channel)				
On-state gate charge 2N7632UD N-channel 2N7632UD P-channel			$Q_{G(on)}$		3.1 3.0	nC nC
On Gate to source charge 2N7632UD N-channel 2N7632UD P-channel			Q_{GS1}		1.2 1.5	nC nC
On Gate to drain charge 2N7632UD N-channel 2N7632UD P-channel			Q_{GD1}		1.4 0.7	nC nC
Turn-Off gate charge 2N7632UD N-channel 2N7632UD P-channel			$Q_{G(off)}$		3.1 3.0	nC nC
Off Gate to source charge 2N7632UD N-channel 2N7632UD P-channel			Q_{GS2}		1.2 1.5	nC nC
Off Gate to drain charge 2N7632UD N-channel 2N7632UD P-channel			Q_{GD2}		1.4 0.7	nC nC
Reverse recovery time 2N7632UD N-channel 2N7632UD P-channel	3473	$di/dt = -100$ A/ μ s, $I_D = I_{D1}$ $V_{DD} \leq 25$ V $V_{DD} \leq -25$ V	trr		60 30	ns ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F		R and F		
				Min	Max	Min	Max	
<u>Subgroup 1</u> Not applicable								
<u>Subgroup 2</u> Steady-state total dose irradiation (V _{GS} bias) 4/	1019	T _C = + 25°C V _{DS} = 0 V V _{GS} = 6 V (N-channel) V _{GS} = -6 V (P-channel)						
Steady-state total dose irradiation (V _{DS} bias) 4/	1019	V _{GS} = 0 V; V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)						
End-point electricals								
Breakdown voltage, drain to source N-channel P-channel	3407	V _{GS} = 0 V; I _D = ±0.25 mA; bias condition C	V _{(BR)DSS}	100 -100		100 -100		V dc V dc
Gate to source voltage (threshold) N-channel P-channel	3403	V _{DS} ≥ V _{GS} I _D = ±0.25 mA	V _{GS(th)1}	1.0 -1.0	2.0 -2.0	1.0 -1.0	2.0 -4.0	V dc V dc
Gate current N-channel P-channel	3411	V _{GS} = ±10 V; V _{DS} = 0 V; bias condition C	I _{GSSF1}		100 -100		100 -100	nA dc nA dc
Gate current N-channel P-channel	3411	V _{GS} = ±10 V; V _{DS} = 0 V; bias condition C	I _{GSSR1}		-100 100		-100 100	nA dc nA dc
Drain current N-channel P-channel	3413	V _{GS} = 0 V; bias condition C V _{DS} = 80 percent of rated V _{DS}	I _{DSS}		1 -1		1 -1	μA dc μA dc
Static drain-source on-state voltage N-channel P-channel	3405	I _D = I _{D2} , condition A; pulsed (see 4.5.1) V _{GS} = 4.5 V V _{GS} = -4.5 V	V _{DS(on)}		0.348 -0.574		0.348 -0.574	V dc V dc
Forward voltage source drain diode N-channel P-channel	4011	V _{GS} = 0 V; I _D = I _{D1} ; bias condition C	V _{SD}		1.2 -5.0		1.2 -5.0	V dc V dc

1/ For sampling plan see [MIL-PRF-19500](#).

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package, or in any qualified package, that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	45 devices c = 0
<u>Subgroup 3</u>			
Switching time test	3472	$I_D = I_{D1}$, $R_G = 24\Omega$, $V_{DD} = 50$ percent rated V_{DS}	
2N7632UD N-channel		$V_{GS} = 5.0$ V dc Maximum limits: $t_{d(on)} = 10$ ns; $t_r = 5$ ns; $t_{d(off)} = 30$ ns; $t_f = 15$ ns	
2N7632UD P-channel		$V_{GS} = -5.0$ V dc Maximum limits: $t_{d(on)} = 17$ ns; $t_r = 20$ ns; $t_{d(off)} = 36$ ns; $t_f = 32$ ns	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves	3161	See MIL-PRF-19500 .	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only. – Continued.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 11</u>			3 devices
SEE <u>2/ 3/ 4/</u> Electrical measurements <u>5/</u> SEE irradiation	1080	See figure 5 I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table 1 , subgroup 2 Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25 \pm 5^\circ C$ Surface LET = $38 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, Range = $38 \mu\text{m} \pm 7.5\%$, energy = $300 \text{ MeV} \pm 7.5\%$	
2N7632UD N-channel		In-situ bias conditions: $V_{DS} = 60 \text{ V}$ and $V_{GS} = -6 \text{ V}$ $V_{DS} = 35 \text{ V}$ and $V_{GS} = -7 \text{ V}$ (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7632UD P-channel		In-situ bias conditions: $V_{DS} = -60 \text{ V}$ and $V_{GS} = 6 \text{ V}$ $V_{DS} = -50 \text{ V}$ and $V_{GS} = 7 \text{ V}$ (typical 3.75 MeV/nucleon at Texas A & M Cyclotron) Surface LET = $62 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $33 \mu\text{m} \pm 7.5\%$, energy = $355 \text{ MeV} \pm 7.5\%$	
2N7632UD N-channel		In-situ bias conditions: $V_{DS} = 60 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 30 \text{ V}$ and $V_{GS} = -6 \text{ V}$ (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7632UD P-channel		In-situ bias conditions: $V_{DS} = -60 \text{ V}$ and $V_{GS} = 6 \text{ V}$ (typical 2.70 MeV/nucleon at Texas A & M Cyclotron) Surface LET = $85 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $29 \mu\text{m} \pm 7.5\%$, energy = $380 \text{ MeV} \pm 10\%$	
2N7632UD N-channel		In-situ bias conditions: $V_{DS} = 60 \text{ V}$ and $V_{GS} = -4 \text{ V}$ $V_{DS} = 40 \text{ V}$ and $V_{GS} = -5 \text{ V}$ (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7632UD P-channel		In-situ bias conditions: $V_{DS} = -60 \text{ V}$ and $V_{GS} = 5 \text{ V}$ (typical 1.89 MeV/nucleon at Texas A & M Cyclotron)	
Electrical measurements <u>5/</u>		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table 1 , subgroup 2	

1/ A separate sample for each test shall be pulled.

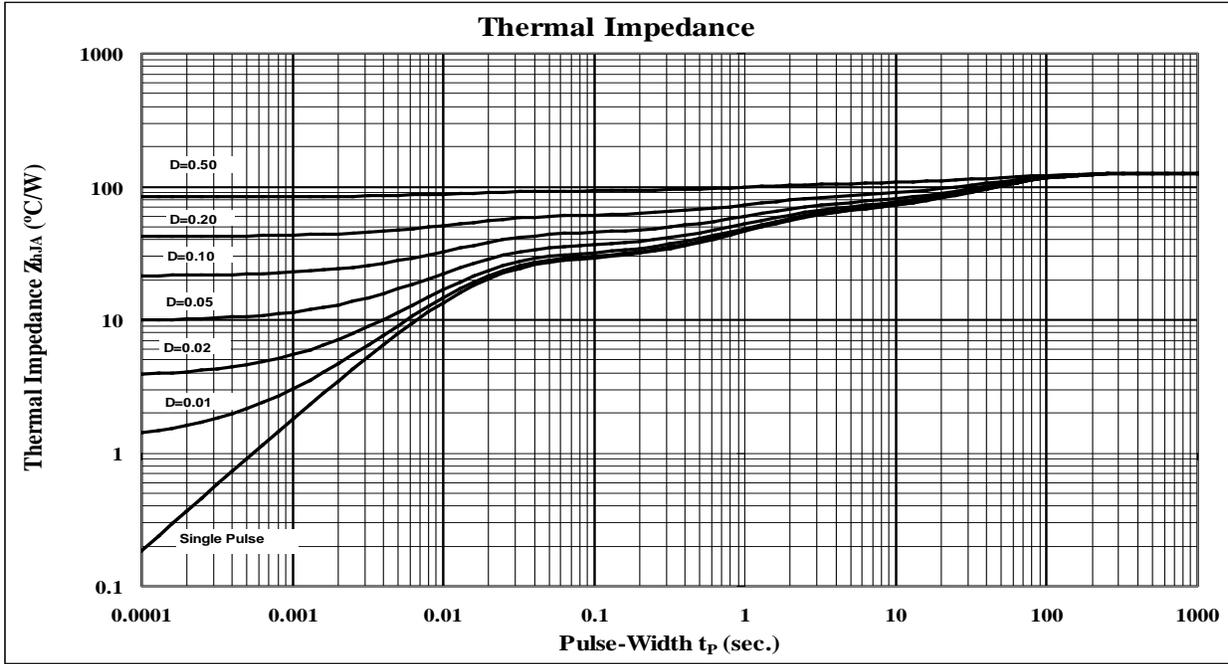
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

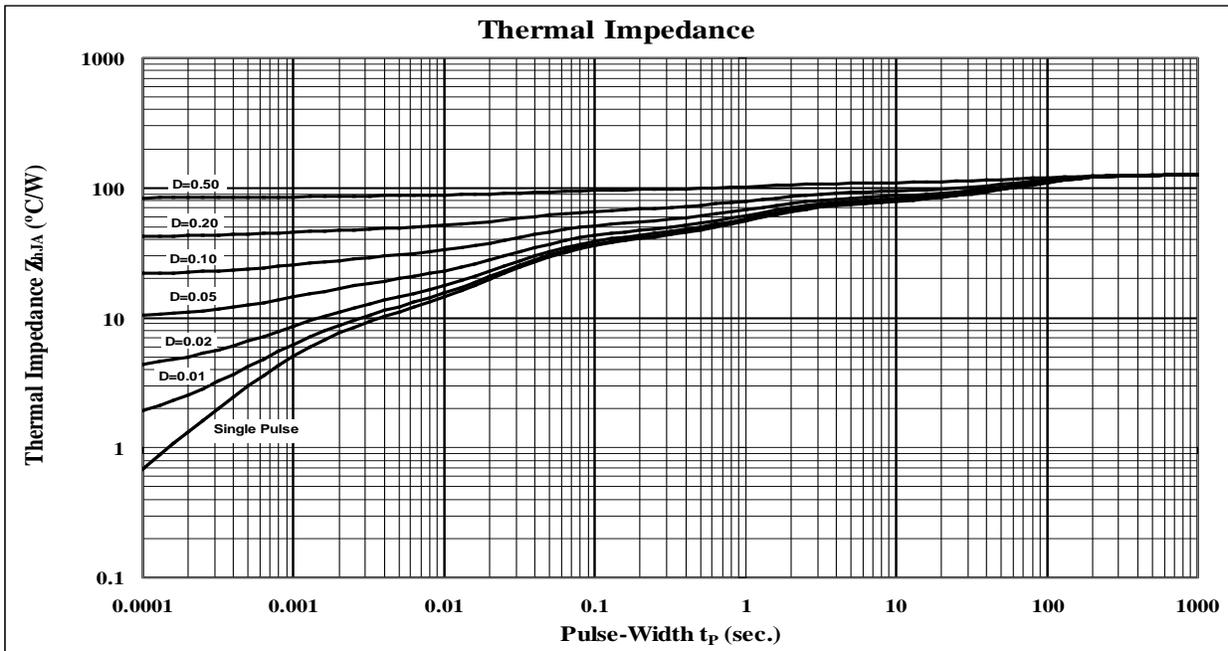
4/ The sampling plan applies to each bias condition.

5/ Examine I_{GSSF1} , I_{GSSR1} , and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table 1](#), subgroup 2, may be performed at the manufacturer's option.

2N7632UD (N-channel)



2N7632UD (P-channel)

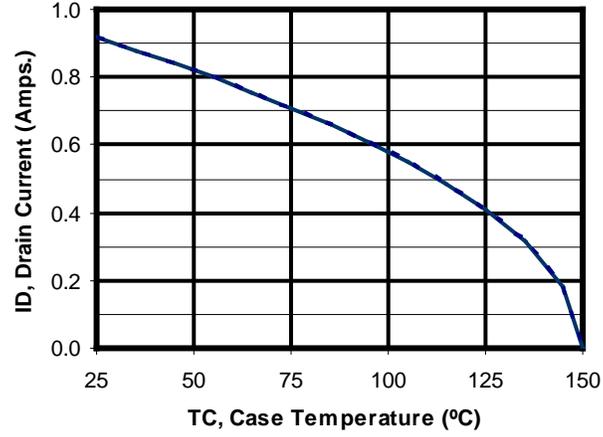


* FIGURE 2. Thermal impedance curves.

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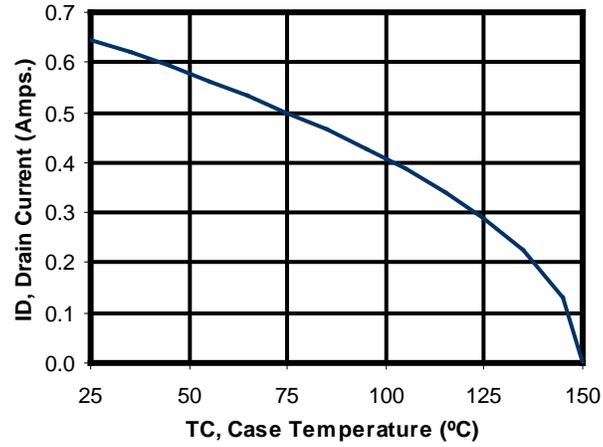
2N7632UD (N-Channel)

Maximum Current Rating



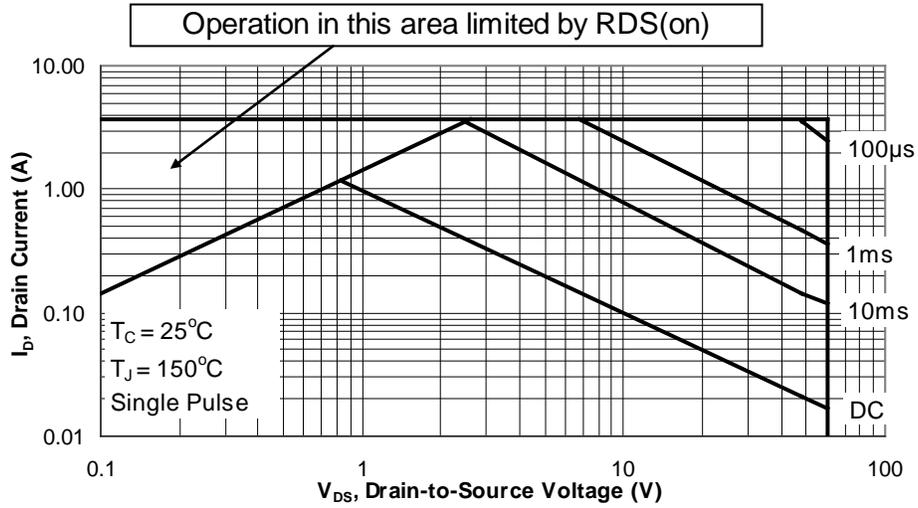
2N7632UD (P-Channel)

Maximum Current Rating

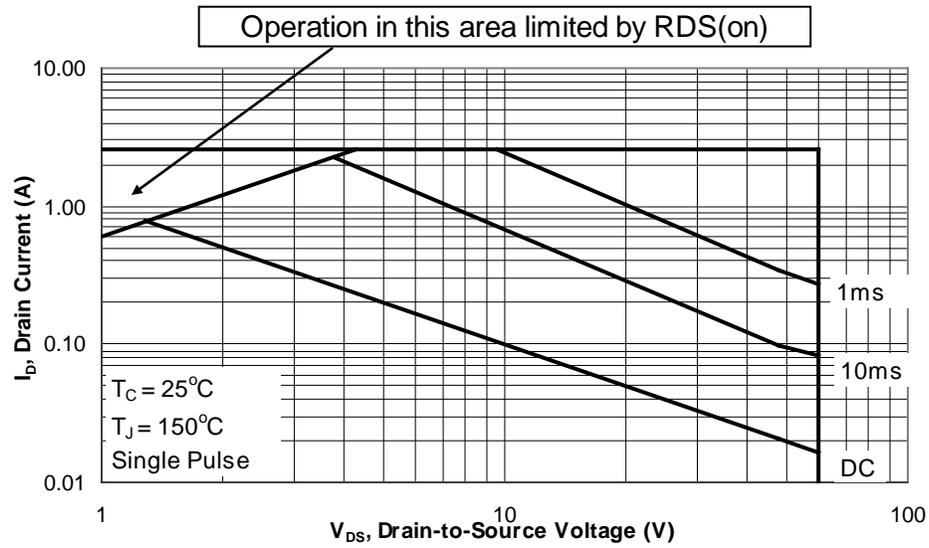


* FIGURE 3. Derating drain current.

2N7632UD N-channel

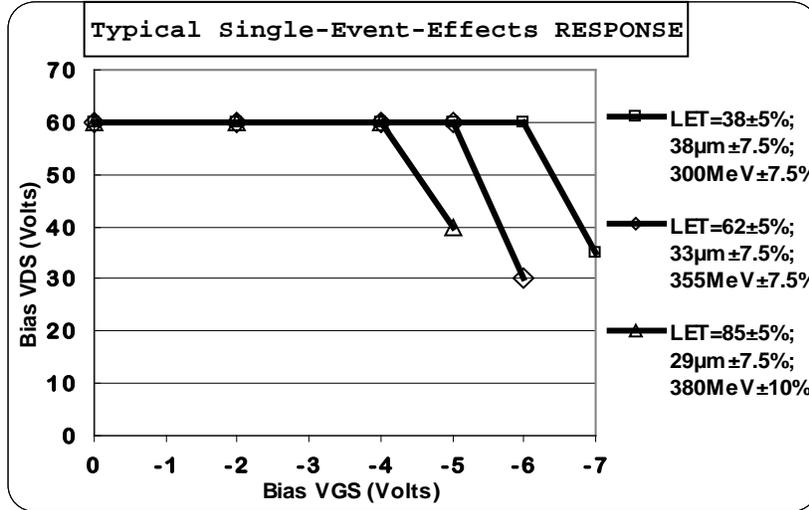


2N7632UD P-channel

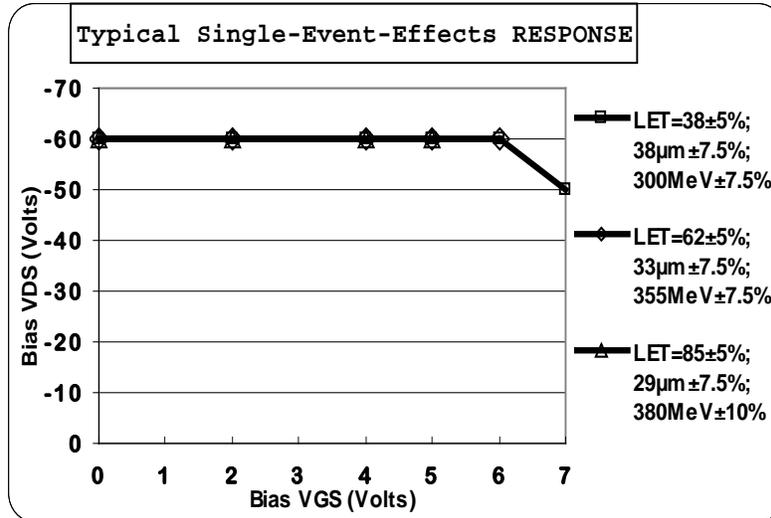


* FIGURE 4. Safe operating area graphs.

2N7632UD (N-channel)



2N7632UD (P-channel)



* FIGURE 5. Typical SEE safe operating area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Commercial PIN
2N7632UD	IRHLUC7670Z4

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2011-064)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil/>.