The documentation and process conversion measures necessary to comply with this revision shall be completed by 25 May 2021

INCH-POUND

MIL-PRF-19500/757C
W/AMENDMENT 2
25 February 2021
SUPERSEDING
MIL-PRF-19500/757C
W/AMENDMENT 1
10 October 2019

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED,
P-CHANNEL, SILICON, THROUGH HOLE AND SURFACE MOUNT, TYPES 2N7624 AND 2N7625
QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, radiation hardened (total dose and single event effects (SEE)), low-threshold logic level, MOSFET, transistor.

* 1.2 Package outlines. The device packages for the encapsulated device types are as follows: TO-257AA in accordance with figure 1, TO-276AA in accordance with figure 2, and a surface mount U3CE (similar to TO-276AA) in accordance with figure 3, for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T (1) T_C =+25°C	P_T T_A =+25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{GS}	I_{D1} T_C =+25°C (3) (4)	I_{D2} T_C =+100°C (3) (4)	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7625T3	75	1.56	1.67	-60	±10	-20	-16.6	-20	-80	-55 to +150
* 2N7624U3, U3CE	57	1.00	2.20	-60	±10	-22	-14.9	-22	-88	

(1) Derate linearly by 0.60 mW/°C (2N7625T3) for T_C > +25°C; by 0.45 mW/°C (2N7624U3) for T_C > +25°C.
(2) See figure 4, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by product design and construction (package, internal wires and pin diameter) to 20 A (T3), to 22 A (U3).

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 5, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)\ DSS}$ V_{GS} = 0 V I_D = 250 µA dc	$V_{GS\ (th)1}$ V_{DS} = V_{GS} I_D = 250 µA dc		Max I_{DSS1} V_{GS} = 0 V V_{DS} = 80 percent rated VDS	Max $r_{DS(on)}$ (1) V_{GS} = 4.5 V dc		E_{AS}	I_{AS}
					at I_{D2} T_J = +25°C	T_J = +150°C		
	V dc	V dc		µA dc	Ohm	Ohm	mJ	A dc
		Min	Max					
* 2N7625	-60	-1.0	-2.0	-1.0	0.074	0.108	181	-20
2N7624	-60	-1.0	-2.0	-1.0	0.072	0.103	79	-22

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "TXV" and "S".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7624" and "7625".

* 1.5.4 Suffix characters. The following suffix letters are incorporated in the PIN for this specification sheet:

T3	Indicates a through-hole mount package similar to a TO-257AA (see figure 1).
U3	Indicates a 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 2).
U3CE	Indicates a ceramic lidded 3 pad surface mount package with enhanced PCB mount features, similar to a TO-276AA (SMD-0.5) (see figure 3).

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML 19500.

* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s)):

For device types 2N7624U3, 2N7624U3CE, 2N7625T3: ..... 300 krads(Si) 1/

Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device types 2N7624U3, 2N7624U3CE, 2N7625T3:
No SEB and SEGR were observed at surface LET (see table IV) ..... ≤ 92.3 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = -40 V and V_{GS} = 0 V)

1/ Manufacturer supplying device types 2N7624U3, 2N7624U3CE, and 2N7625T3 has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 300 krads(Si).

2/ Manufacturer also performed heavy ion SEB and SEGR test at TAMU Radiation Effects Facility for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.
* MIL-STD-883 - Test Method Standard Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

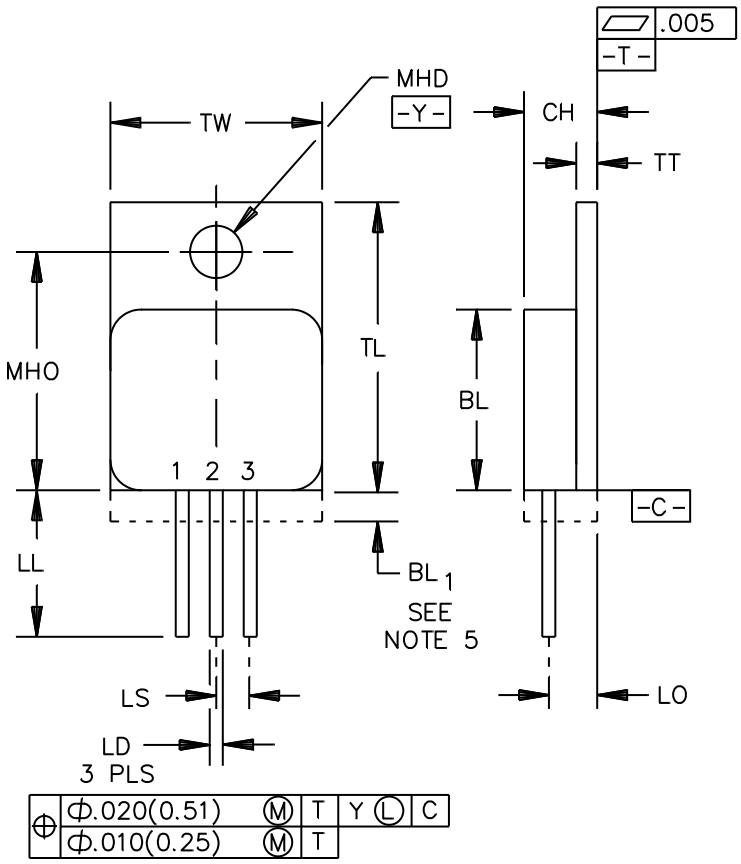
* 3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and figure 1 (TO-257AA), figure 2 (TO-276AA), and figure 3 (similar to TO-276AA) herein. For 2N7625T3, methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the device shall be as shown on figure 1 and figure 2.

3.4.3 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

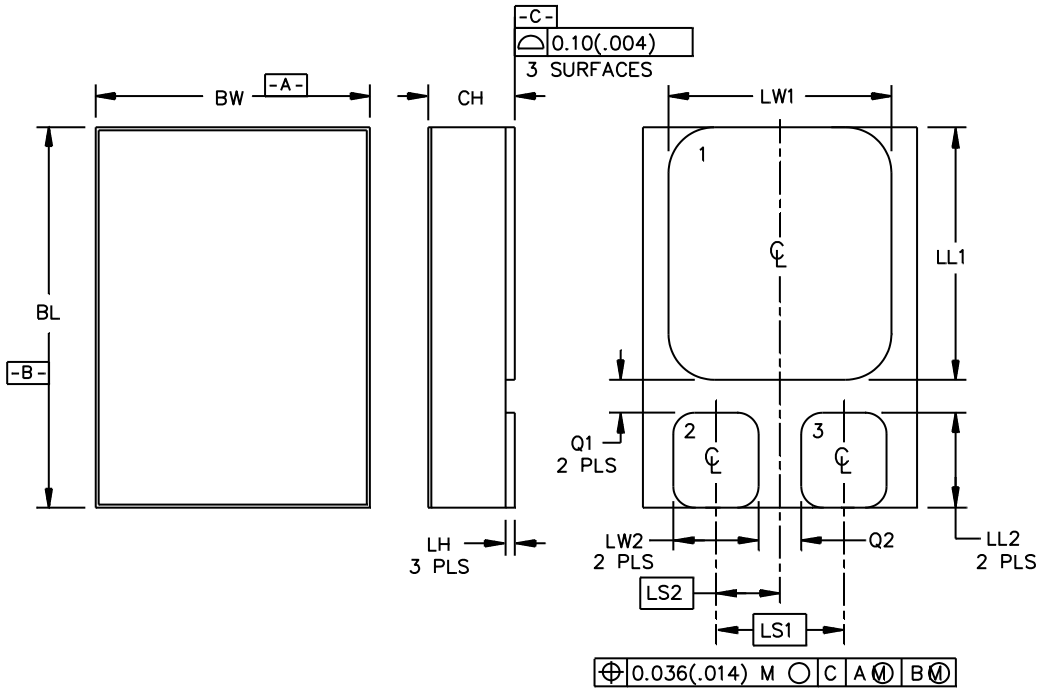
* 3.4.4 Silicone die coating. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each silicone lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.



Ltr	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL_1		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.
5. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).

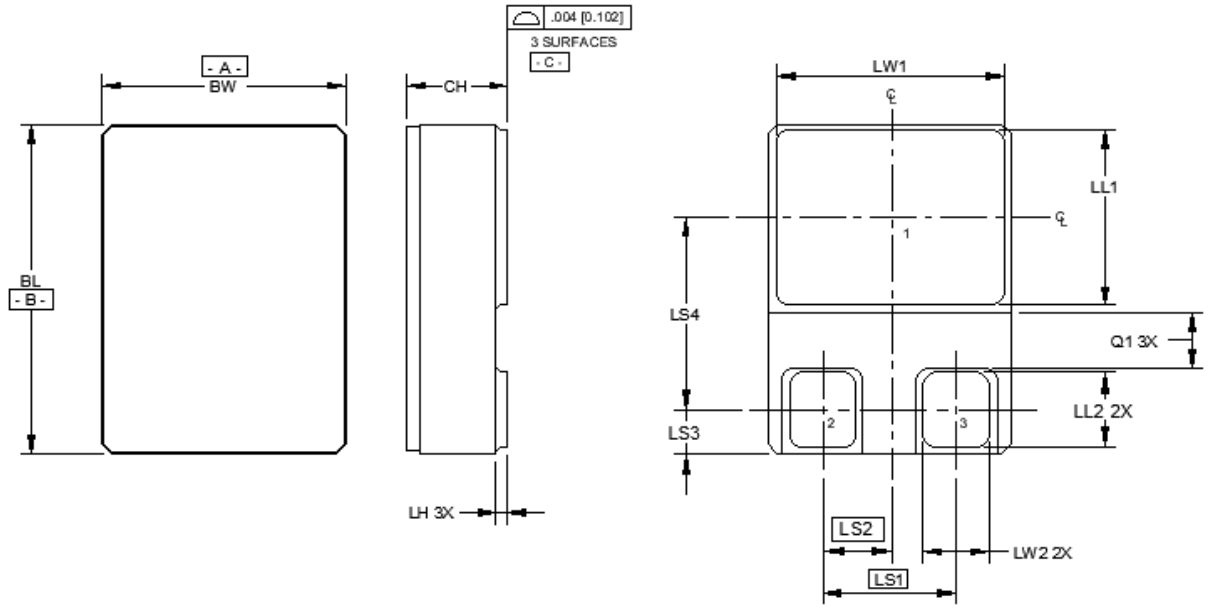
FIGURE 1. Dimensions and configuration, TO-257AA (T3).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.123		3.12
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimension are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 2. Dimensions and configuration TO-276AA, SMD-0.5 (U3).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.122		3.09
LH	.008	.022	0.20	0.55
LW1	.271	.281	6.88	7.14
LW2	.075	.085	1.91	2.16
LL1	.208	.218	5.28	5.54
LL2	.087	.097	2.21	2.46
LS1	.165 BSC		4.19 BSC	
LS2	.083 BSC		2.10 BSC	
LS3	.053 BSC		1.35 BSC	
LS4	.234 BSC		5.93 BSC	
Q1	.006		0.152	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimension are in inches, Millimeters are given for information only.
2. Dimension tolerances ±.005.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.
5. Dimensions are pre solder finish

* FIGURE 3. Dimensions and configuration (Similar to TO-276AA, SMD-0.5), with ceramic lid U3CE.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3 and table I.

3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects SEE. SEE (SEB/SEGR) shall be performed in accordance with TM1080 of MIL-STD-750 at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE(SEB/SEGR) characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
* 5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.5)	Not applicable
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, I_{GSSR1} as minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.5 µA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.5 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.5 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
17	For TO–257AA and U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For TO–257AA and U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 15 V minimum for t = 250 µs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}) ..... I_{D1}.

b. Peak gate voltage (V_{GS}) ..... -5 V dc (up to max rated V_{GS}).

c. Gate to source resistor (R_{GS}) ..... $25 \leq R_{GS} \leq 200\ \Omega$.

d. Initial case temperature ..... +25°C, +10°C, -5°C.

e. Inductance: ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... -25 V dc (up to max V_{DS}).

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, t_{MD}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

* a. Magnitude of test voltage ..... 700 V dc (TO-257AA), 1000 V dc (U3).

b. Duration of application of test voltage ..... 15 seconds (min).

c. Points of application of test voltage ..... All leads to case (bunch connection).

d. Method of connection ..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).

f. Maximum leakage current ..... 1.0 mA.

g. Voltage ramp up time ..... 500 V/second

* 4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for quality conformance inspection in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein.

4.4.2.2 Quality level JANS (table E-VIA of MIL-PRF-19500).

	Subgroup	Method	Condition
	B3	1051	Test condition G, 100 cycles.
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	B4	1042	Condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
	B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS}; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
	B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS}; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.

4.4.2.3 Quality level JANTXV (table E-VIB of MIL-PRF-19500).

Subgroup	Method	Condition
B2	1051	Test condition C, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

	Subgroup	Method	Condition
	C2	2036	Test condition A, weight = 10 lbs., t = 10 s (applicable to TO-257AA only).
*	C3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	C5	3161	See 4.3.3, $R_{\theta JC}$ = (see 1.3).
	C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JA}$			°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0, I_D = -250 µA dc, bias condition C	$V_{(BR)DSS}$	-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -250 µA dc	$V_{GS(TH)1}$	-1.0	-2.0	V dc
Gate current	3411	V_{GS} = -10 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		-100	nA dc
Gate current	3411	V_{GS} = +10 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		+100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		-1.0	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 4.5 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$			
2N7625T3					0.074	Ω
2N7624U3, U3CE					0.072	Ω
Forward voltage	4011	V_{GS} = 0, condition B, pulsed (see 4.5.1), I_D = I_{D1}	V_{SD}		-5.0	V (pk)
Subgroup 3						
High temperature operation:		T_C = T_J = +125°C				
Gate current	3411	V_{GS} = ±10 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		±200	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		-15	µA dc
Static drain to source on-state resistance	3421	V_{GS} = -4.5 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)2}$			
2N7625T3					0.140	Ω
2N7624U3, U3CE					0.140	Ω

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3 - continued						
Gate to source voltage (threshold)	3403	V_{DS} = V_{GS}, I_D = -250 µA dc	$V_{GS(TH)2}$	-0.5		V dc
Low temperature operation:		T_C = T_J = -55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -250 µA dc	$V_{GS(TH)3}$		-3.0	V dc
Subgroup 4						
Forward transconductance	3475	V_{DS} = -10 V dc, I_D = I_{D2}, pulsed (see 4.5.1)	gFS			S
2N7625T3				17		S
2N7624U3, U3CE				16		S
Switching time test	3472	I_D = I_{D1}, V_{GS} = -5.0 V dc up to rated V_{GS}, R_G = 7.5 Ω, V_{DD} = 50 percent rated V_{DS}				
Turn-on delay time			$t_{d(on)}$		32	ns
Rise time			t_r			
2N7625T3					265	ns
2N7624U3, U3CE					250	ns
Turn-off delay time			$t_{d(off)}$		100	ns
Fall time			t_f			
2N7625T3					85	ns
2N7624U3, U3CE					102	ns
Subgroup 5						
Safe operating area test	3474	V_{DS} = 80 percent of rated V_{DS} (see 1.3) t_P = 10 ms, I_D as specified in figure 6				
Electrical measurements		See table I, subgroup 2				
Subgroups 6						
Not applicable						

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 7						
Gate charge	3471	Condition B, $I_D = I_{D1}$, V_{DS} = 50 percent of rated V_{DS}				
On-state gate charge			$Q_{G(on)}$		36	nC
On gate to source charge			Q_{GS1}			
2N7625T3					14	nC
2N7624U3, U3CE					10	nC
On gate to drain charge			Q_{GD1}		18	nC
Turn-off gate charge			$Q_{G(off)}$		36	nC
Off gate to source charge			Q_{GS2}			
2N7625T3					14	nC
2N7624U3, U3CE					10	nC
Off gate to drain charge			Q_{GD2}		18	nC
Reverse recovery time	3473	Condition A, di/dt = 100 A/µs, $V_{DD} \leq$ -50 V, $I_D = I_{D1}$	t_{rr}			
2N7625T3					100	ns
2N7624U3, U3CE					110	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

* TABLE II. Group D inspection.

	Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
		Method	Conditions		R and F		R		F		
					Min	Max	Min	Max	Min	Max	
	Subgroup 1										
	Not applicable										
	Subgroup 2		T_C = + 25°C								
*	Steady-state total dose irradiation (V_{GS} bias) 4/	1019	Condition A, V_{GS} = -10V ; V_{DS} = 0								
*	Steady-state total dose irradiation (V_{DS} bias) 4/	1019	Condition A, V_{GS} = 0;V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)								
	End-point electricals:										
	Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = -250 µA; bias condition C	$V_{(BR)DSS}$	-60		-60		-60		V dc
	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = -250 µA	$V_{GS(th)1}$	-1.0	-2.0	-1.0	-2.0	-1.0	-2.0	V dc
	Gate current	3411	V_{GS} = -10 V, V_{DS} = 0, bias condition C	I_{GSSF1}		-100		-100		-100	nA dc
	Gate current	3411	V_{GS} = +10 V, V_{DS} = 0, bias condition C	I_{GSSR1}		100		100		100	nA dc
	Drain current	3413	V_{GS} = 0, bias condition C; V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS}		-1.0		-1.0		-1.0	µA dc
	Static drain to source on-state voltage	3405	V_{GS} = -4.5 V; condition A, pulsed (see 4.5.1), $I_{D1} = I_{D2}$	$V_{DS(on)}$							
	2N7625T3					-1.262		-1.262		-1.262	V dc
	2N7624U3					-1.132		-1.132		-1.132	V dc
	Forward voltage source drain diode	4011	V_{GS} = 0; I_D = I_{D1} bias condition C	V_{SD}		-5.0		-5.0		-5.0	V dc

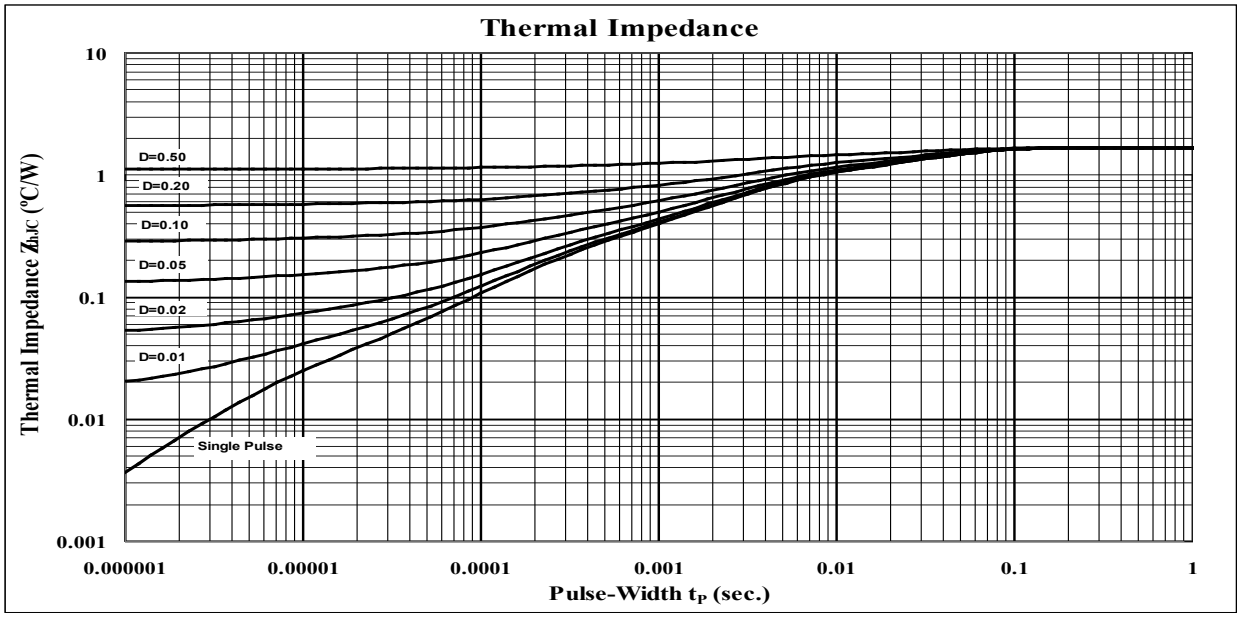
1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias. Devices supplied to this drawing have been characterized through levels R and F of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table II. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.6 herein).

TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

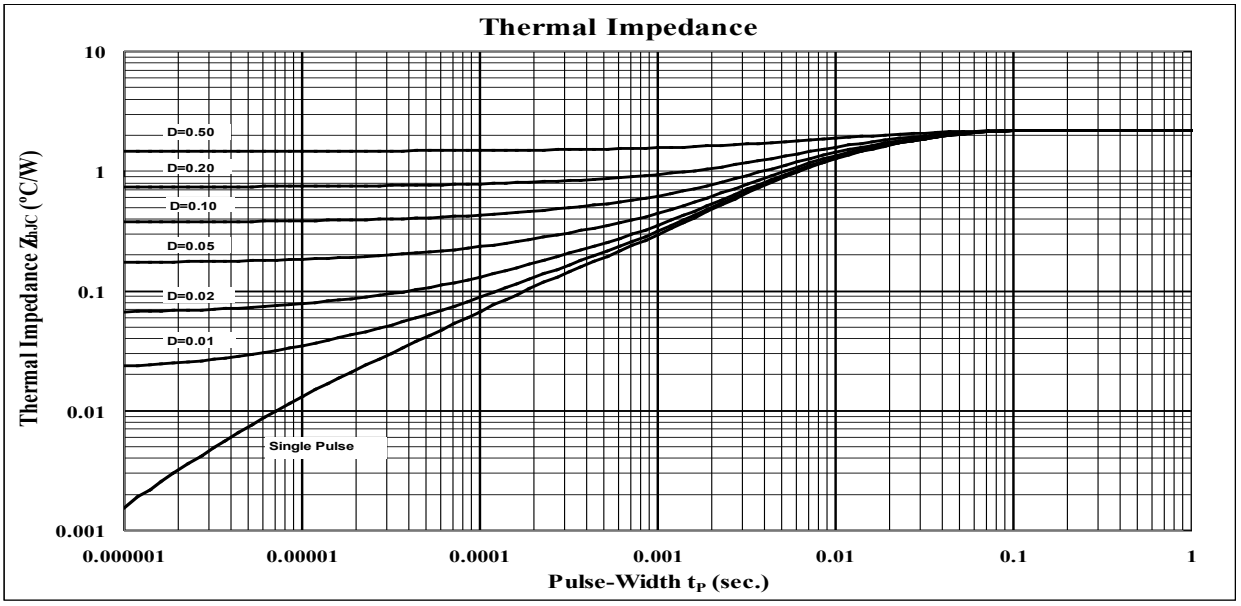
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves	3161	See MIL-PRF-19500	
Subgroup 5			
Not applicable			
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
* Subgroup 11			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ The sampling plan applies to each bias condition.

2N7625T3

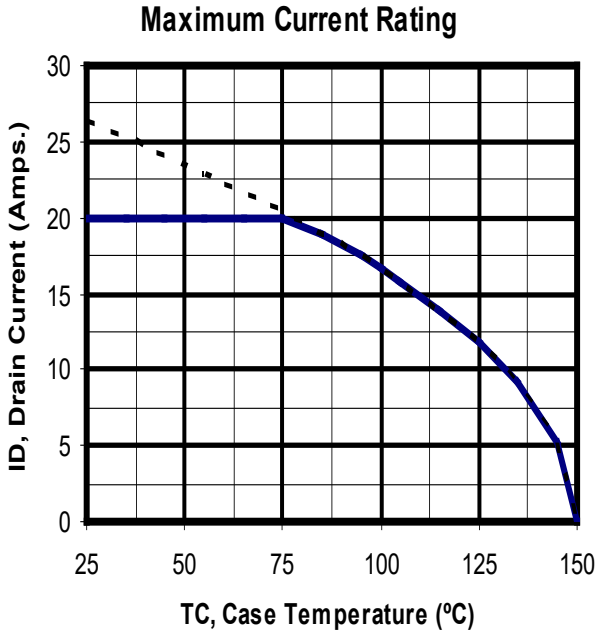


2N7624U3, U3CE

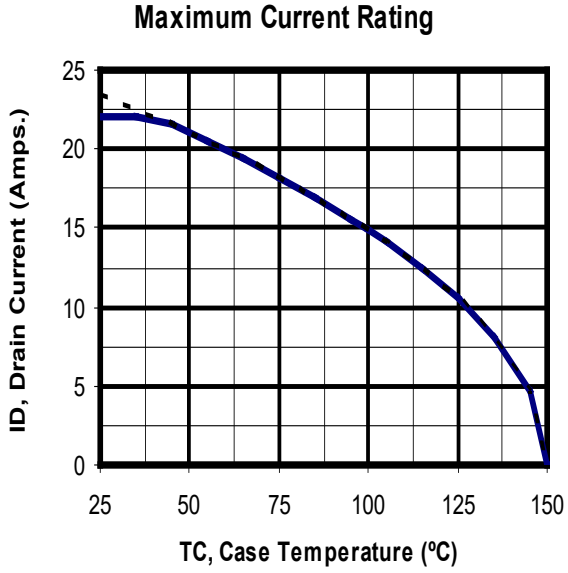


* FIGURE 4. Thermal impedance graph.

2N7625T3

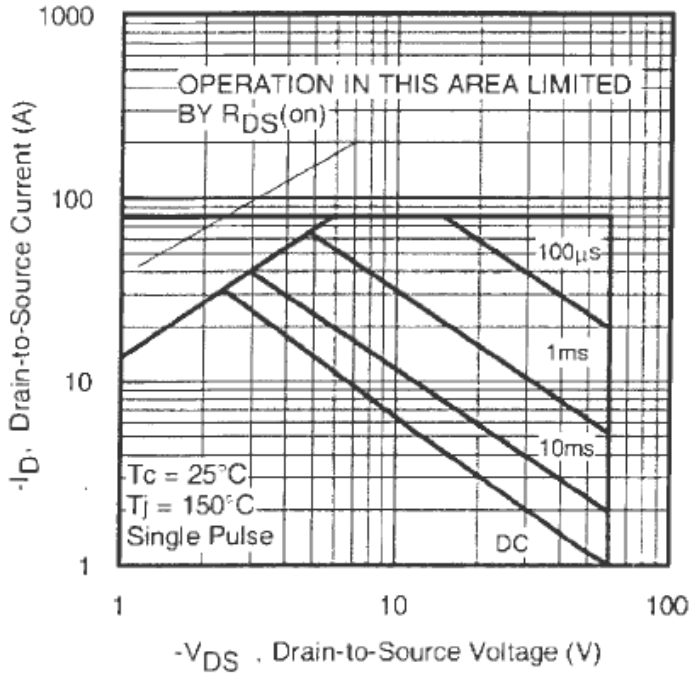


2N7624U3, U3CE

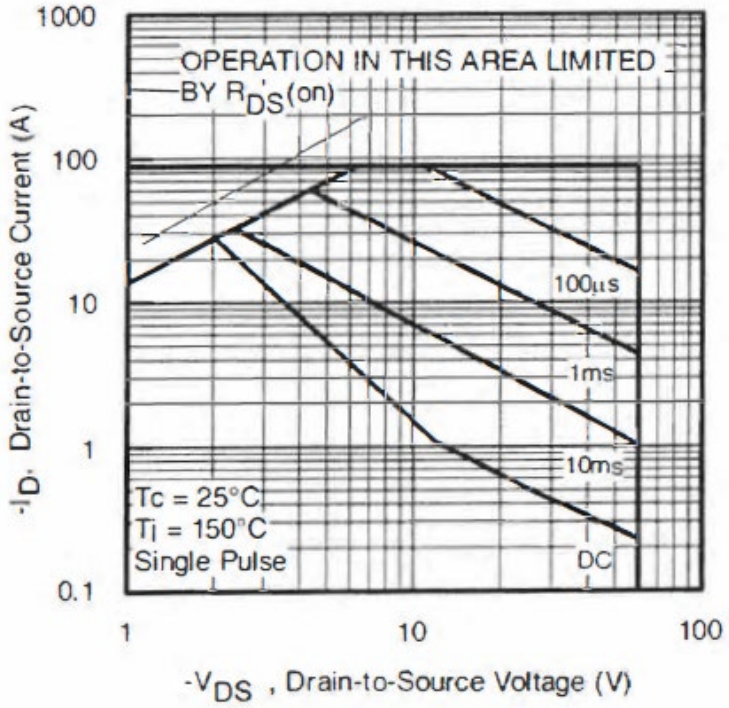


* FIGURE 5. Derating drain current.

2N7625T3



2N7624U3, U3CE



* FIGURE 6. Safe-operating-area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.6.

e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.

f. If specific SEE characterization conditions are desired (see section 6.5 and table IV), manufacturer's cage code should be specified in the contract or order.

g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHLYS797034CM	2N7625T3
IRHLNJ797034	2N7624U3
IRHLNK797034	2N7624U3CE

6.5 Application data.

* 6.5.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE (SEB and SEGR) conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

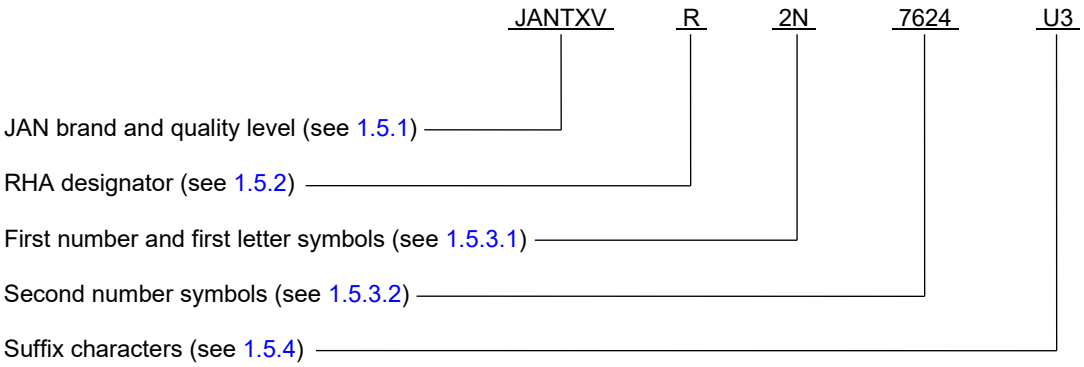
* TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750 method 1080	3 devices
	Pre SEB and SEGR Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation		Fluence = 3E5 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C Surface LET = 32.4 MeV-cm^2/mg, range = 83.3 µm, Kr ion beam energy = 679 MeV In-situ bias conditions: V_{DS} = -60 V and V_{GS} = 6 V (typical 8.09 MeV/nucleon at Texas A & M Cyclotron) Surface LET = 61.7 MeV-cm^2/mg, range = 48.7 µm, Xe ion beam energy = 584 MeV In-situ bias conditions: V_{DS} = -60 V and V_{GS} = 4 V (typical 4.53 MeV/nucleon at Texas A & M Cyclotron) Surface LET = 92.3 MeV-cm^2/mg, range = 65.1 µm, Au ion beam energy = 1156 MeV In-situ bias conditions: V_{DS} = -40 V and V_{GS} = 0 V (typical 5.87 MeV/nucleon at Texas A & M Cyclotron)	
	Post SEB/SEGR Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE SEB/SEGR heavy ion irradiation to determine acceptability for each bias conditions. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

2/ Manufacturer performed heavy ion SEE(SEB/SEGR) test at Texas A & M Radiation Effects Facility for the MOSFET devices in accordance with TM1080 of MIL-STD-750. No single event burnout (SEB) and Single event gate rupture(SEGR) were observed to surface LET as stated above table IV and safe operating area. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE(SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

6.6 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



* 6.7 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices in a TO-276AA package	PINs for devices in a U3CE package	PINs for devices in a TO-257AA package
JANTXVR2N7624U3	JANTXVR2N7624U3CE	JANTXVR2N7625T3
JANSR2N7624U3	JANSR2N7624U3CE	JANSR2N7625T3
JANTXVF2N7624U3	JANTXVF2N7624U3CE	JANTXVF2N7625T3
JANSF2N7624U3	JANSF2N7624U3CE	JANSF2N7625T3

1/ DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Downloads/QPLQML/19500/QPDSIS_19500.pdf/

6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA – CC

Review activity:
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2021-003)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.