

The documentation and process conversion measures necessary to comply with this revision shall be completed by 24 November 2014

INCH-POUND

MIL-PRF-19500/750A  
8 October 2014  
SUPERSEDING  
MIL-PRF-19500/750  
17 October 2008

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, FIELD EFFECT  
N-CHANNEL, SILICON, SURFACE MOUNT PACKAGE, TYPE 2N7507  
QUALITY LEVELS JANTX, JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, power transistor.

\* 1.2 Package outlines. The device packages for this specification sheet are the TO-276AA (SMD 0.5, U3) in accordance with [figure 1](#) for all packaged device types.

1.3 Maximum ratings. (Unless otherwise specified,  $T_A = +25^\circ\text{C}$ ).

Type (1)	$P_T$ (1) $T_C = +25^\circ\text{C}$	$P_T$ $T_A = +25^\circ\text{C}$ (free air)	$R_{\theta JC}$ (2)	$V_{DS}$	$V_{DG}$	$V_{GS}$	$I_{D1}$ (3) (4) $T_C = +25^\circ\text{C}$	$I_{D2}$ $T_C = +100^\circ\text{C}$	$I_S$	$I_{DM}$ (5)	$T_J$ and $T_{STG}$
	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u><math>^\circ\text{C}</math></u>
2N7507U3	75	1.56	1.67	150	150	$\pm 20$	20	12	20	80	-55 to +150

(1) Derate linearly by 0.6 W/ $^\circ\text{C}$  for  $T_C > +25^\circ\text{C}$ .

(2) See [figure 2](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical  $I_D$  limit.  $I_D$  is limited to 22 A by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See [figure 3](#), maximum drain current graph.

(5)  $I_{DM} = 4 \times I_{D1}$ ;  $I_{D1}$  as calculated by footnote (3).

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

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\* 1.4 Primary electrical characteristics at  $T_c = +25^\circ\text{C}$ .

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 0.25$ mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ $I_D = 0.25$ mA dc		Max $I_{DSS1}$ $V_{GS} = 0$ $V_{DS} = 100$ percent of rated $V_{DS}$	Max $r_{DS(ON)}$ (1) $V_{GS} = 10$ V dc		$E_{AS}$ at $I_{AS}$	$I_{AS}$
					$T_J = +25^\circ\text{C}$ at $I_{D2}$	$T_J = +150^\circ\text{C}$ at $I_{D2}$		
	<u>V dc</u>	<u>V dc</u>		<u><math>\mu\text{A dc}</math></u>	<u>ohm</u>	<u>ohm</u>	<u>mJ</u>	<u>A</u>
		Min	Max					
2N7507U3	150	2.0	4.0		25	0.080		

(1) Pulsed (see 4.5.1).

\* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.6 for a list of available PINs.

\* 1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "TX", "TXV" and "S".

\* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

\* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

\* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7507".

\* 1.5.3 Suffix characters. The suffix characters "U3" indicates a 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 1).

\* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

\* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

\* 3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in [MIL-PRF-19500](#) and herein. The device package style is a TO-276AA in accordance with [figure 1](#) for all device types.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

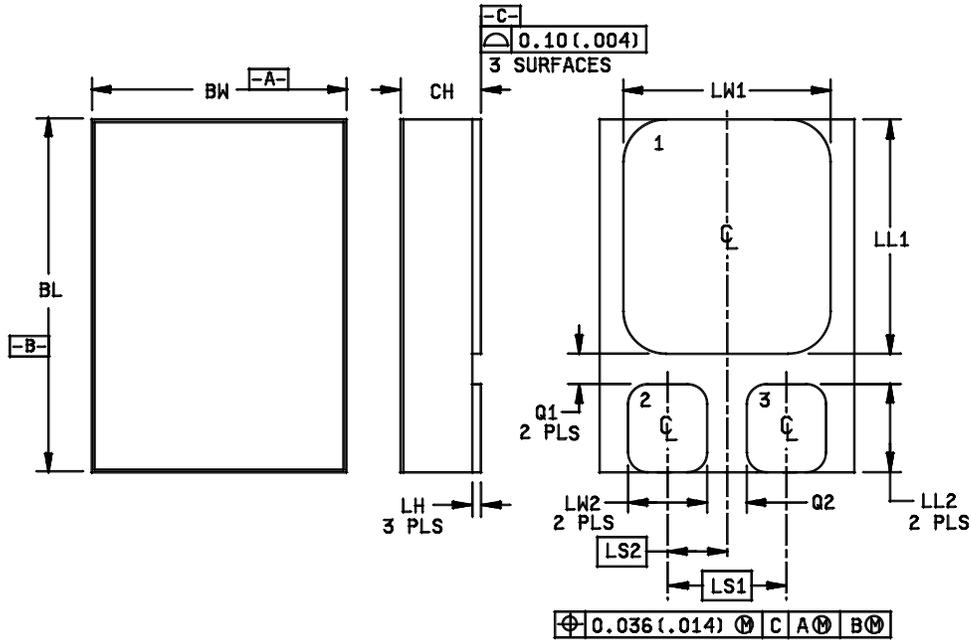
\* 3.4.2 Pin-out. The pin-out of the device shall be as shown on [figure 1](#) and [figure 2](#).

\* 3.4.3 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

\* 3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#) and [table I](#).

\* 3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.



Dimensions				
Ltr.	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.123	2.76	3.12
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.
4. Terminal 1 - Drain, Terminal 2 - Gate, Terminal 3 - Source.

FIGURE 1. Physical dimensions for SMD-0.5, TO-276AA (2N7507U3).

#### 4. VERIFICATION

\* 4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

\* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed by the first inspection lot of this revision to maintain qualification.

\* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3) (4)	Method 3470 of MIL-STD-750 (see 4.3.2) optional	Method 3470 of MIL-STD-750 (see 4.3.2) optional
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.3)	Method 3161 of MIL-STD-750 (see 4.3.3)
9	$I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; $I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , $r_{DS(on)1}$ , $V_{GS(TH)1}$ , $\Delta I_{GSSF1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater.	Subgroup 2 of table I herein, $I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , $r_{DS(on)1}$ , $V_{GS(TH)1}$
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.
* 17	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

(1) At the end of the test program,  $I_{GSSF1}$ ,  $I_{GSSR1}$ , and  $I_{DSS1}$  are measured.

(2) An out-of-family program to characterize  $I_{GSSF1}$ ,  $I_{GSSR1}$ ,  $I_{DSS1}$ , and  $V_{GS(th)1}$  shall be invoked.

\* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

(4) Method 3470 is optional if performed as a sample in group A, subgroup 5.

4.3.1 Gate stress test. Apply  $V_{GS} = +24$  V minimum for  $t = 250$   $\mu$ s minimum.

4.3.2 Single pulsed unclamped inductive switching.

- a. Peak current,  $I_D$ ..... $I_{AS(max)}$ .
- b. Peak gate voltage,  $V_{GS}$  ..... 10 V, up to maximum rated  $V_{GS}$
- c. Gate to source resistor,  $R_{GS}$ ..... $25 \Omega \leq R_g \leq 200 \Omega$ .
- d. Initial case temperature ..... $+25^\circ\text{C}$ ,  $+10^\circ\text{C}$ ,  $-5^\circ\text{C}$ .
- e. Inductance, L .....  $\left[ \frac{2E_{AS}}{(I_{DI})^2} \right] \left[ \frac{(V_{BR} - V_{DD})}{V_{BR}} \right] \text{mH}$  minimum.
- f. Number of pulses to be applied ..... 1 pulse.
- g. Supply voltage ( $V_{DD}$ ) .....50 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$ , (and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 70  $\mu$ s max. See [table II](#), group E, subgroup 4 herein.

\* 4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage..... 600V dc (U3).
- b. Duration of application of test voltage ..... 15 seconds (min).
- c. Points of application of test voltage ..... All leads to case (bunch connection).
- d. Method of connection..... Mechanical.
- e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).
- f. Maximum leakage current..... 1.0 mA.
- g. Voltage ramp up time..... 500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#). Alternate flow is allowed for conformance inspection in accordance with [MIL-PRF-19500](#).

\* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#) herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in [table E-VIA](#) (JANS) and [table E-VIB](#) (JANTX and JANTXV) of [MIL-PRF-19500](#), and herein.

\* 4.4.2.1 Quality level JANS (table E-VIA of MIL-PRF-19500).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B4	1042	The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the "on" cycle.
B5	1042	A separate sample may be pulled for each test. Accelerated steady-state reverse bias; test condition A, $V_{DS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 120$ hours, read and record $V_{BR}(DSS)$ (pre and post) at $I_D = -1$ mA. Read and record $I_{DSS}$ (pre and post).
B5	1042	Accelerated steady-state gate stress; test condition B, $V_{GS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 24$ hours.
B5	2037	Test condition D.

\* 4.4.2.2 Quality levels JANTX and JANTXV (table E-VIB of MIL-PRF-19500).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B2	1051	Test condition G.
B3	1042	The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the "on" cycle.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Not applicable.
C5	3161	$R_{\theta JC} = 1.67$ °C/W maximum, see 4.5.2.
C6	1042	The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the "on" cycle.

\* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$  (and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 70  $\mu\text{s}$  max. See table E-IX of MIL-PRF-19500, group E, subgroup 4.

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\* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			$^{\circ}C/W$
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ V dc, $I_D = 0.25$ mA dc, condition C	$V_{(BR)DSS}$	150		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 0.25$ mA dc	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, $V_{DS} = 0$ , bias condition C	$I_{GSSF1}$		+100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, $V_{DS} = 0$ , bias condition C	$I_{GSSR1}$		-100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, $V_{DS} = 100$ percent of rated $V_{DS}$ ; bias condition C	$I_{DSS1}$		25	$\mu A$ dc
Static drain to source on-state resistance	3421	$V_{GS} = 10$ V dc, pulsed (see 4.5.1); condition A, $I_D =$ rated $I_{D2}$ (see 1.3)	$r_{DS(on)1}$		0.080	$\Omega$
* Forward voltage (source drain diode)	4011	Condition B, Pulsed (see 4.5.1), $I_D =$ rated $I_{D2}$	$V_{SD}$		1.3	V
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^{\circ}C$				
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$ , $I_D = 0.25$ mA dc	$V_{GS(th)2}$	1.0		V dc
Gate current	3411	Bias condition C, $V_{GS} = \pm 20$ V dc, $V_{DS} = 0$ V dc	$I_{GSS2}$		$\pm 200$	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS2}$		0.25	mA dc
* Static drain to source on-state resistance	3421	Condition A, $V_{GS} = 10$ V dc, pulsed (see 4.5.1); $I_D =$ rated $I_{D2}$	$r_{DS(on)2}$		0.168	$\Omega$
Low temperature operation:		$T_C = T_J = -55^{\circ}C$				
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$ , $I_D = 0.25$ mA dc	$V_{GS(th)3}$		5.0	V dc

See footnotes at end of table.

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\* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = \text{rated } I_{D2}, V_{DD} = 15 \text{ V}$ (see 4.5.1)	gFS	12		S
Switching time test	3472	$I_D = \text{rated } I_{D2}, V_{GS} = 10 \text{ V dc},$ gate drive impedance = 5.1 $\Omega$ $V_{DD} = 50 \text{ percent rated } V_{DS}$				
Turn-on delay time			$t_{d(\text{on})}$		25	ns
Rise time			$t_r$		60	ns
Turn-off delay time			$t_{d(\text{off})}$		75	ns
Fall time			$t_f$		60	ns
<u>Subgroup 5</u>						
Safe operating area test	3474	See figure 4; $V_{DS} = 80 \text{ percent of}$ rated $V_{BR(DSS)}, V_{DS} \leq 200 \text{ V};$ $t_p = 10 \text{ ms}$				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = \text{rated } I_{D2}, V_{DD} =$ 80 percent of rated $V_{DS}$	$Q_{g(\text{on})}$		85	nC
On-state charge						
Gate to source charge			$Q_{gs}$		11	nC
Gate to drain charge			$Q_{gd}$		47	nC
Reverse recovery time	3473	Condition A, $di/dt = 100 \text{ A}/\mu\text{s}, V_{DD}$ $\leq 25 \text{ V},$ $I_D = \text{rated } I_{D2}$	$t_{rr}$		260	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

Group B, subgroups 2 and 3 (JANTX and JANTXV).

Group B, subgroups 3 and 4 (JANS).

Group C, subgroup 2 and 6.

Group E, subgroup 1.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycle	1051	Condition G, 200 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 2</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours, $V_{GS} = 80$ percent of rated (see <a href="#">1.3</a> )	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 4</u>			sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring $dv/dt$ during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

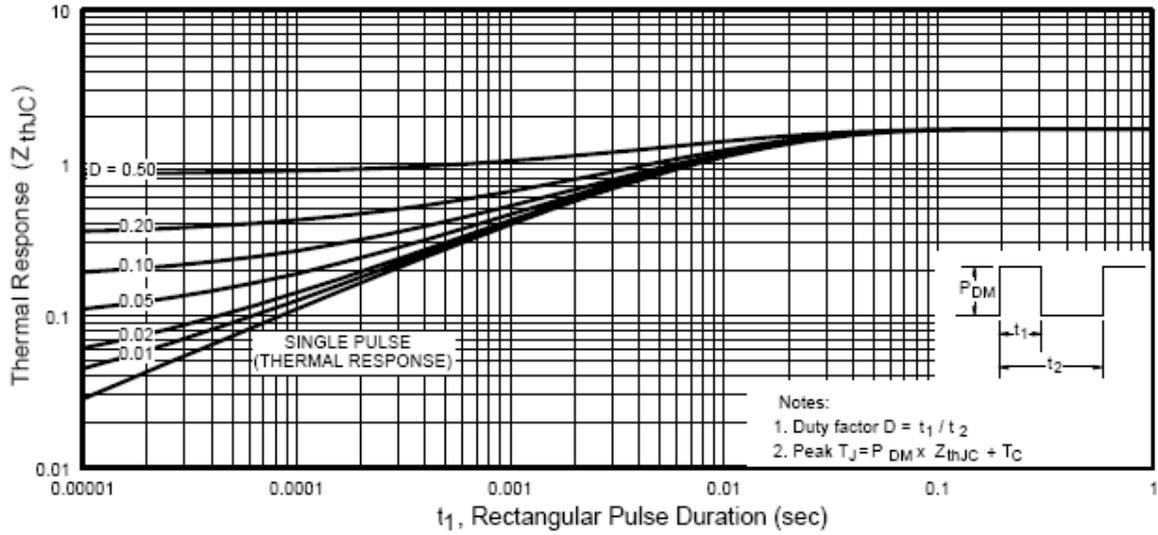


FIGURE 2. Thermal impedance curves.

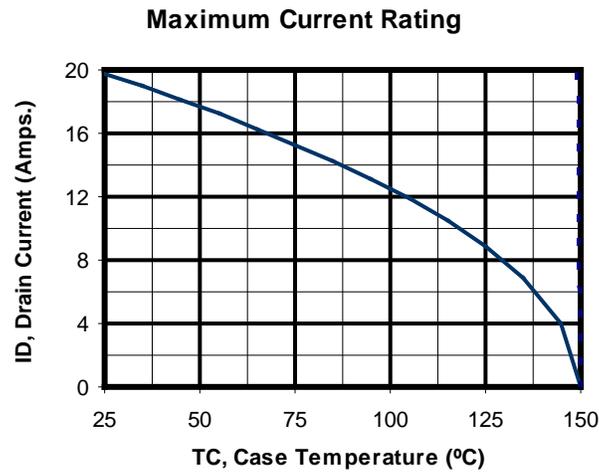


FIGURE 3. Maximum drain current versus case temperature graphs.

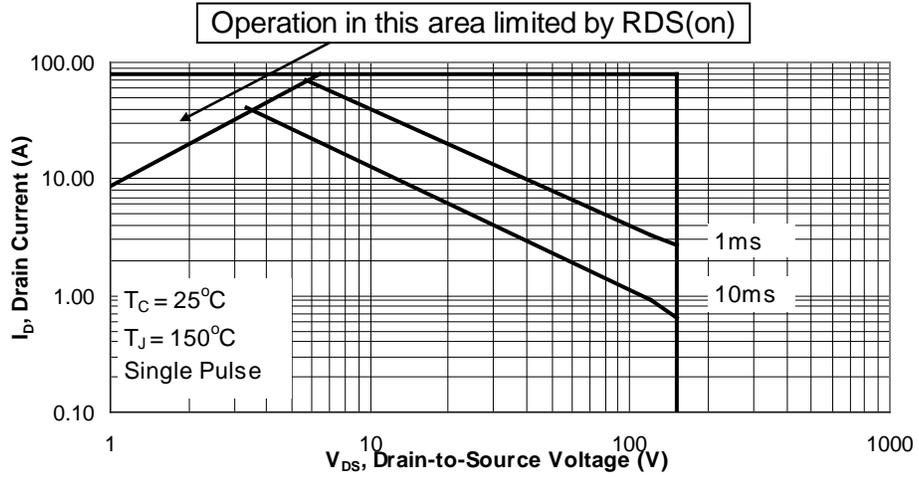


FIGURE 4. Maximum safe operating area.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

\* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see [3.4.1](#)).
- d. The complete Part or Identifying Number (PIN), see [1.5](#).

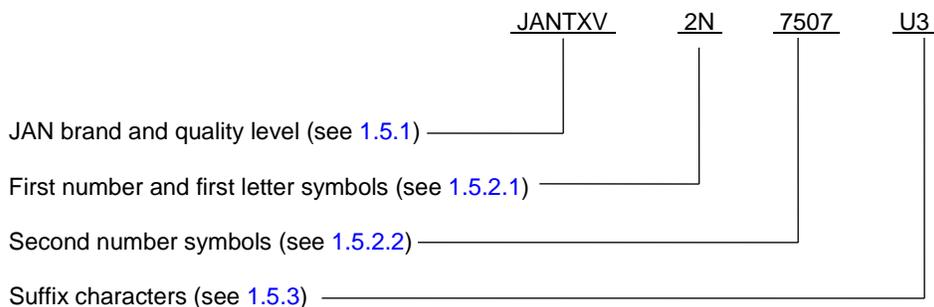
\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <http://assist.dla.mil>.

6.4 Cross-reference complement list. Parts from this specification may be used to supersede the following commercial Part or Identifying Number (PIN) listed below.

Preferred types	Commercial types
2N7507U3	IRF5NJ3315

MIL-PRF-19500/750A

- \* 6.5 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



- \* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices in a TO-276AA package
JAN2N7507U3
JANTX2N7507U3
JANTXV2N7507U3
JANS2N7507U3

- \* 6.7 Changes from previous issue. The margins of this specification are marked with asterisk to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:  
 Army - CR  
 Navy - EC  
 Air Force - 85  
 NASA - NA  
 DLA - CC

Preparing activity:  
 DLA - CC  
 (Project 5961-2014-121)

- \* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.dla.mil/>.