

The documentation and process conversion measures necessary to comply with this revision shall be completed by 19 May 2015.

INCH-POUND

MIL-PRF-19500/749C
 19 February 2015
 SUPERSEDING
 MIL-PRF-19500/749B
 21 May 2010

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED
 P-CHANNEL, SILICON, TYPES 2N7506U8 AND 2N7506U8C,
 JANTXVR, JANTXVF, JANSR AND JANSF

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications. See [6.7](#) for unencapsulated JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: surface mount SMD-0.2, U8 (metal lid) suffix and U8C (ceramic lid) suffix in accordance with [figure 1](#) for all encapsulated device types..

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>
2N7506U8, 2N7506U8C	23	1.0	5.4	-100	-100	±20	-3.1	-2.0	-3.1	-12.4	-55 to +150

- (1) Derate linearly by 0.185 W/°C for $T_C > +25^\circ\text{C}$.
- (2) See [figure 2](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 3](#), maximum drain current graph.
- (5) $I_{DM} = 4 \times I_{D1}$ as calculated in note (3).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



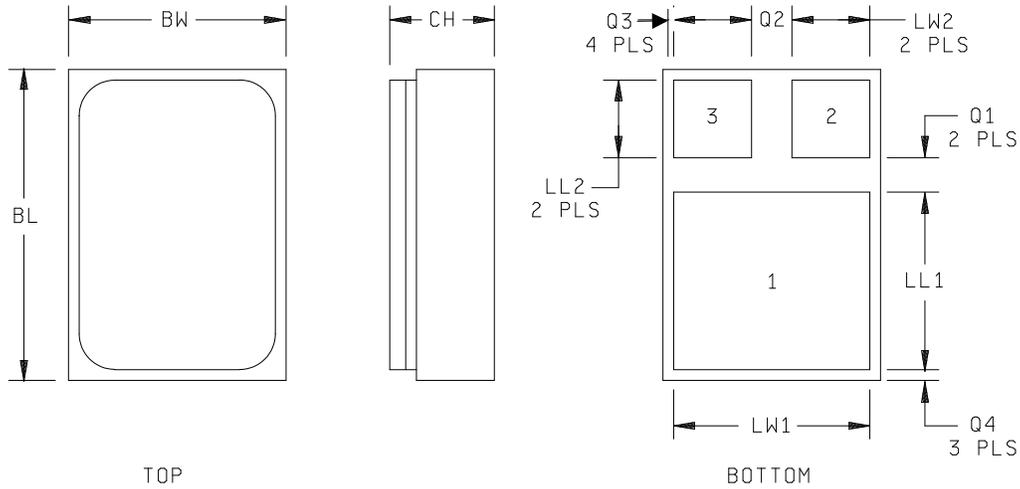
1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 1.0mA dc	V _{GS(TH)1} V _{DS} ≥ V _{GS} I _D = 1.0 mA dc	Max I _{DSS1} V _{GS} = 0 V _{DS} = 80% of rated V _{DS}	Max r _{DS(on)} (1) V _{GS} = 12V, I _D = I _{D2}		E _{AS}	I _{AS}
				T _J = +25°C	T _J = +150°C		
	<u>V dc</u>	<u>V dc</u> Min Max	<u>μA dc</u>	<u>Ω</u>	<u>Ω</u>	<u>mJ</u>	<u>A</u>
2N7506U8, 2N7506U8C	-100	-2.0 -4.0	10	1.20	2.40	28	-3.1

(1) Pulsed (see 4.5.1).

- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.
- * 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".
- * 1.5.2 JAN certification mark and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.
- * 1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "M", "D", "P", "L", "R", "F", "G", and "H".
- * 1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
 - * 1.5.4.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
 - * 1.5.4.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7506".
 - * 1.5.5 Suffix letters. The suffix letter "U8" indicates that the transistor is a surface mount package with a metal lid in accordance with [figure 1](#). The suffix letter "U8C" indicates that the transistor is a surface mount package with a ceramic lid in accordance with [figure 1](#).
 - * 1.5.6 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

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Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.305	.321	7.75	8.15	
BW	.200	.226	5.08	5.74	
CH (for U8)		.097		2.46	U8 only
CH (for U8C)		.106		2.69	U8C only
LW1	.193	.203	4.90	5.16	
LW2	.076	.086	1.93	2.18	
LL1	.174	.184	4.42	4.67	
LL2	.074	.084	1.88	2.13	
Q1	.030	.040	0.76	1.02	
Q2	.030	.040	0.76	1.02	
Q3	.01 REF		0.25 REF		
Q4	.01 REF		0.25 REF		
TERM 1	Drain				
TERM 2	Gate				
TERM 3	Source				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for SMD-0.2, 2N7506U8 and 2N7506U8C.

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

I_{AS} Rated avalanche current, non-repetitive
nC nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (SMD-0.2, U8 and U8C) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

- * 4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

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* 4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein, I _{GSSF1} , I _{GSSR1} , I _{DSS1} as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} Subgroup 2 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value ΔV _{GS(th)1} = ±20 percent of initial value	Subgroup 2 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value ΔV _{GS(th)1} = ±20 percent of initial value

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.

(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and V_{GS(th)1} shall be invoked.

* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 24$ V, minimum for $t = 250$ μ sec., minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D1}$.
- b. Inductance $L = \left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- c. Gate to source resistor R_{GS} : $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage $V_{DD} = 50$ V dc maximum.
- e. Initial case temperature $T_C = +25^\circ$ C, -5° C, $+10^\circ$ C.
- f. Gate voltage $V_{GS} = 12$ V dc (up to rated V_{GS}).
- g. Number of pulses to be applied: 1 pulse minimum.

4.3.3 Thermal impedance ($Z_{\theta JC}$ measurement). The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table III](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#) and as follows.

4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
* B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175^\circ$ C, $t = 24$ hours minimum; or $T_A = +150^\circ$ C, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175^\circ$ C, $t = 120$ hours minimum; or $T_A = +150^\circ$ C, $t = 240$ hours minimum.
B5	2037	Test condition D.

- * 4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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B2	1051	Test condition G, 25 cycles.
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- * B3 1042 Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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C2	2036	Terminal strength is not applicable.
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C5	3161	Thermal resistance, see 4.5.2, $R_{\theta JC(max)} = 5.4$ °C/W.
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- * C6 1042 Intermittent operation life, condition D. No heat sink or forced air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See table E-IX of MIL-PRF-19500, group E, subgroup 4.

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	Bias condition C, $V_{GS} = 0$, $I_D = 1$ mA dc	$V_{(BR)DSS}$	-100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; $I_D = 1$ mA dc	$V_{GS(TH)1}$	-2.0	-4.0	V dc
Gate current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		-100	nA dc
Gate current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		+100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS} ,	I_{DSS1}		10	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		1.20	Ω
* Forward voltage	4011	$V_{GS} = 0$, condition A, $I_D = I_{D1}$	V_{SD}		-5.0	V dc
<u>Subgroup 3</u>						
High temperature operation		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		25	μA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u> - continued						
Static drain to source on-state resistance	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$		2.28	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)2}$	-1.0		V dc
Low temperature operation		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)3}$		-5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = I_{D2}$, $V_{DD} = 15 \text{ V dc}$ (see 4.5.1)	g_{FS}	1.9		S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12 \text{ V dc}$, $R_G = 7.5 \Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$		18	ns
Rise time			t_r		26	ns
Turn-off delay time			$t_{d(off)}$		24	ns
Fall time			t_f		85	ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4 $t_p = 10 \text{ ms min.}$ $V_{DS} = 80$ percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				

See footnotes at end of table.

*

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B. $I_D = I_{D1}$, $V_{GS} = 12$ V dc, $V_{DD} = 50$ percent of rated V_{DS}				
On-state gate charge			$Q_{G(ON)}$	11		nC
Gate to source charge			Q_{GS}	5.0		nC
Gate to drain charge			Q_{GD}	4.0		nC
Reverse recovery time	3473	$di/dt = -100$ A/ μ s, $V_{DD} \leq 50$ V $I_D = I_{D1}$	t_{rr}	100		ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
 Group B, subgroups 2 and 3 (JANTXV).
 Group B, subgroups 3 and 4 (JANS).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F <u>4/</u>		R <u>4/</u>		F <u>4/</u>		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u> Not applicable										
<u>Subgroup 2</u>		$T_C = + 25^\circ\text{C}$								
Steady-state total dose irradiation (V_{GS} bias) <u>5/</u>	1019	$V_{GS} = 12 \text{ V}; V_{DS} = 0$								
Steady-state total dose irradiation (V_{DS} bias) <u>5/</u>	1019	$V_{GS} = 0;$ $V_{DS} = 80$ percent of rated V_{DS} (preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA};$ bias condition C	$V_{(BR)DSS}$	-100		-100		-100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}; I_D = 1 \text{ mA}$	$V_{GS(th)1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-4.0	V dc
Gate current	3411	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$ bias condition C	I_{GSSF1}		-100		-100		-100	nA dc
Gate current	3411	$V_{GS} = -20 \text{ V}; V_{DS} = 0$ bias condition C	I_{GSSR1}		100		100		100	nA dc
Drain current	3413	$V_{GS} = 0, V_{DS} = 80$ percent of rated V_{DS} (preirradiation) bias condition C,	I_{DSS}		-10		-10		-10	μA dc
Static drain to source on-state voltage	3405	$V_{GS} = 12 \text{ V}; I_D = I_{D2}$ condition A pulsed (see 4.5.1)	$V_{DS(on)}$		1.832		1.832		1.872	V dc
* Forward voltage source drain diode	4011	$V_{GS} = 0; I_D = I_{D1}$ bias condition A	V_{SD}		-5.0		-5.0		-5.0	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ The higher level designation F represents devices which pass end-points at all lower level designation.

5/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		Table I, subgroup 2 herein.	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			3 devices
SEE 2/ 3/	1080	See method 1080 of MIL-STD-750	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level linear energy transfer (LET) is sufficient to qualify all lower level LETs.

2N7506U8, 2N7506U8C

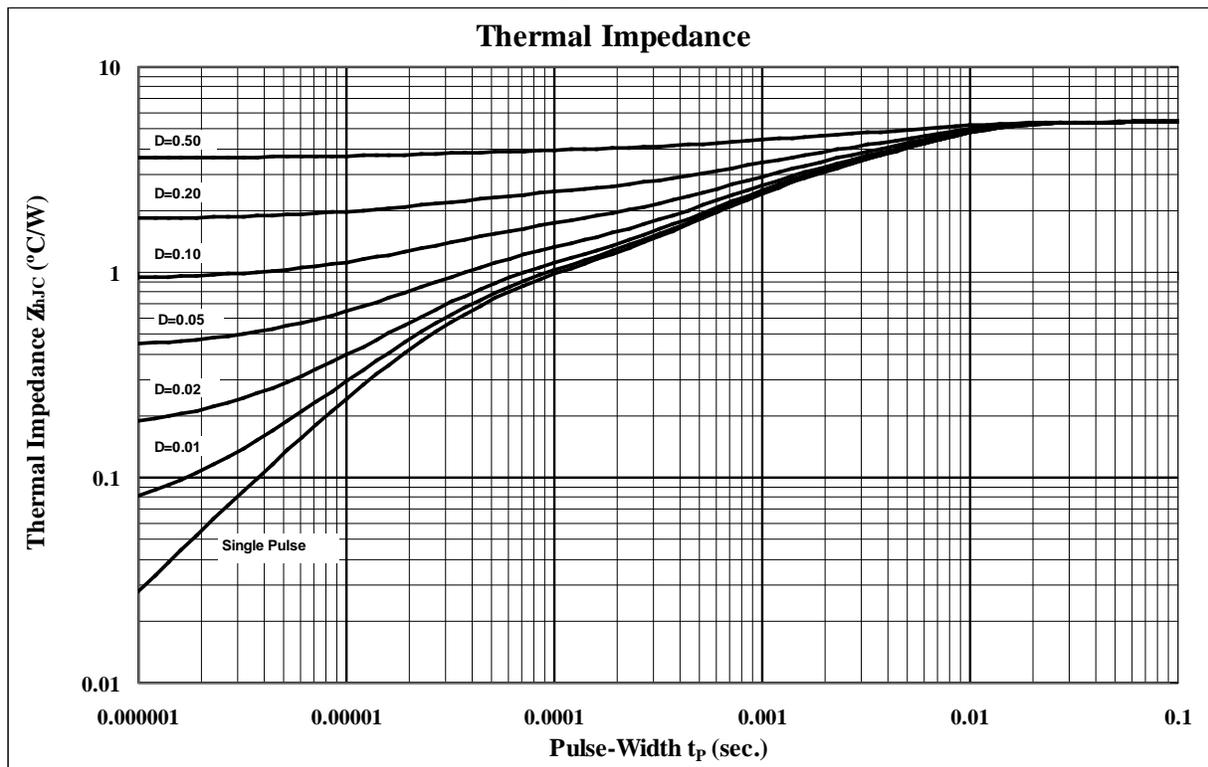


FIGURE 2. Thermal impedance curve.

2N7506U8, 2N7506U8C

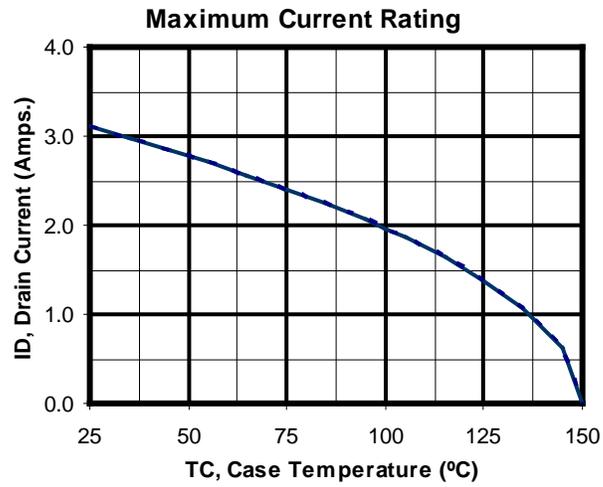


FIGURE 3. Maximum drain current versus case temperature graph.

2N7506U8, 2N7506U8C

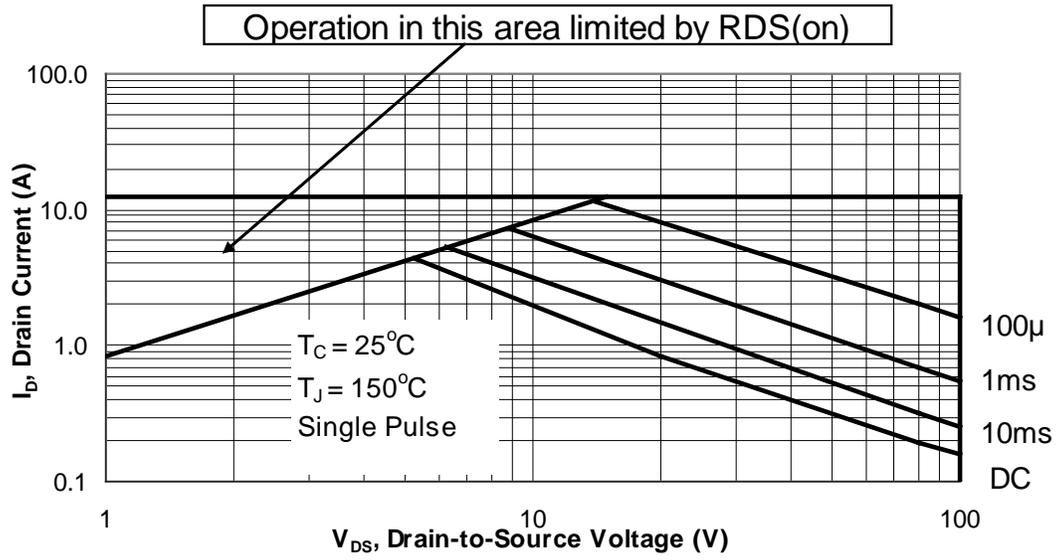


FIGURE 4. Safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

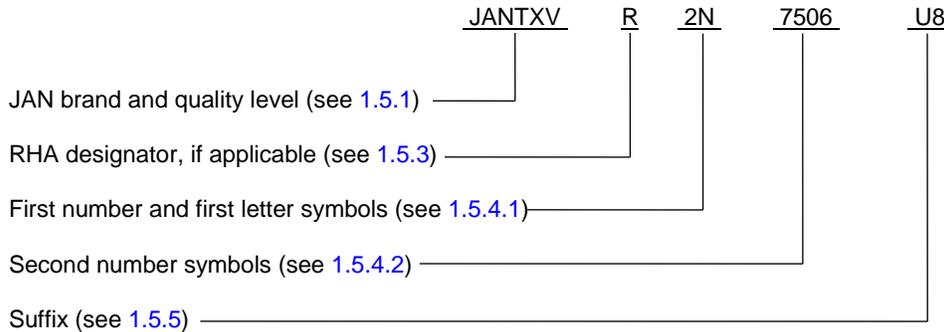
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see [3.4.1](#)).
- * d. The complete Part or Identifying Number (PIN), see [1.5](#) and [6.5](#).
- * e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- * f. If SEE testing data is desired, it should be specified in the contract or order.
- * g. If specific SEE characterization conditions are desired (see section [6.8](#) and [table IV](#)), manufacturer's CAGE code should be specified in the contract or order.
- * 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Military P/N	Generic P/N	Note
2N7506U8	IRHNM597110	
2N7506U8C	IRHNMC597110	Ceramic lid

- * 6.5 PIN construction example. The PINs for encapsulated devices are construction using the following form.



- * 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7506U8	JANTXV#2N7506U8	JANS2N7506U8	JANS#2N7506U8
JANTXV2N7506U8C	JANTXV#2N7506U8C	JANS2N7506U8C	JANS#2N7506U8C

(1) The number sign (#) represent one of five RHA designators available (M, D, P, L, R, F, G, or H).

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

- * 6.8 Application data.

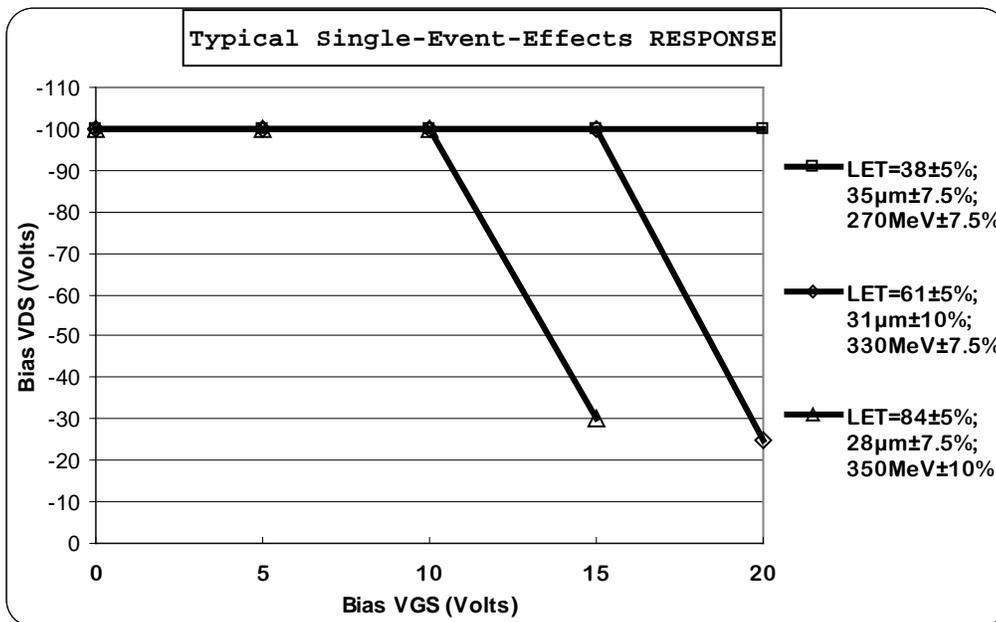
- * 6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 16 June 1998 and older)	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080.0 dated 20 November 2006. See figure 5	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25 \pm 5^\circ C$	
	2N7506U8, 2N7506U8C		Surface LET = $38 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $38 \mu\text{m} \pm 7.5\%$, energy = $270 \text{ MeV} \pm 7.5\%$. In situ bias conditions: $V_{DS} = -100 \text{ V}$ and $V_{GS} = 20 \text{ V}$ (nominal 3.75 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7506U8, 2N7506U8C		Surface LET = $61 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $31 \mu\text{m} \pm 10\%$, energy = $330 \text{ MeV} \pm 7.5\%$. In situ bias conditions: $V_{DS} = -100 \text{ V}$ and $V_{GS} = 10 \text{ V}$, $V_{DS} = -25 \text{ V}$ and $V_{GS} = 20 \text{ V}$, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7506U8, 2N7506U8C	Surface LET = $84 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $28 \mu\text{m} \pm 7.5\%$, energy = $350 \text{ MeV} \pm 7.5\%$. In situ bias conditions: $V_{DS} = -100 \text{ V}$ and $V_{GS} = 10 \text{ V}$, $V_{DS} = -30 \text{ V}$ and $V_{GS} = 15 \text{ V}$, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)			
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I , subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> Upon qualification, all manufacturers should provide the verification test conditions to be added to this table. </div>				

1/ I_{GSSF1} , I_{GSSR1} , and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option.

2N7506U8, 2N7506U8C



*

FIGURE 5. Typical SEE safe operating area graph.

6.9 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2015-012)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.