

INCH-POUND

The documentation and process conversion measures necessary to comply with this revision shall be completed by 14 August 2012.

MIL-PRF-19500/740
w/AMENDMENT 1
15 June 2012
SUPERSEDING
MIL-PRF-19500/740
13 December 2005

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE AND SINGLE EVENT EFFECTS)
QUAD TRANSISTOR, N-CHANNEL AND P-CHANNEL, SILICON TYPES
2N7521U, 2N7522U, 2N7525, AND 2N7526, JANTXVR AND F AND JANSR AND F

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for quad N-channel and quad P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, MS-004CC (28-pad ceramic leadless chip carrier) and 2, MO-036AB.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type (1)	P _T (free air) T _A = +25°C (2)	P _T (3) T _C = +25°C	R _{θJC} (4)	R _{θJA} (4)	V _{DS} = V _{DG}	V _{GS}	I _{D1} T _C = +25°C	I _{D2} T _C = +100°C	I _S	I _{DM} (5)	T _J and T _{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>°C</u>
2N7521U	2.08 (ref.)	10.6	11.8	60	100	±20	4.6	2.9	4.6	18.4	-55
2N7522U	2.08 (ref.)	10.6	11.8	60	-100	±20	-2.4	-1.5	-2.4	-9.6	to
2N7525	1.39	n/a	n/a	90	100	±20	1.6	1.0	1.6	6.4	+150
2N7526	1.39	n/a	n/a	90	-100	±20	-0.85	-0.55	-0.85	-3.4	

- (1) The 2N7521U and 2N7525 are N-channel devices, the 2N7522U and the 2N7526 are P-channel devices.
- (2) Derate linearly 0.017 W/°C (2N7521U and 2N7522U, ref.) or 0.011 W/°C (2N7525 and 2N7526) for T_A > +25°C.
- (3) Derate linearly 0.96 W/°C (2N7525 and 2N7526 only) for T_C > +25°C.
- (4) See figure 3, thermal impedance curves.
- (5) I_{DM} = 4 X I_{D1}; I_{D1} as calculated by:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(for 2N7521U and 2N7522U)

$$I_D = \sqrt{\frac{T_{JM} - T_A}{(R_{\theta JA}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(for 2N7525 and 2N7526)

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil>.

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1.4 Primary electrical characteristics.

Type (1)	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0 \text{ mA}$ dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0 \text{ mA}$ dc	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80\%$ rated V_{DS}	Max $r_{DS(on)1}$ (2) $V_{GS} = 12V,$ $I_D = I_{D2}$ $T_J = +25^\circ C$	Max $r_{DS(on)2}$ (2) $V_{GS} = 12 V,$ $I_D = I_{D2}$ $T_J = +150^\circ C$	E_{AS}	I_{AS}
	<u>V dc</u>	<u>V dc</u> Min Max		<u>μA dc</u>	<u>Ω</u>	<u>mJ</u>	<u>A</u>
2N7521U	100	2.0	4.0	10	0.27	47	4.6
2N7522U	-100	-2.0	-4.0	-10	0.96	60	-2.4
2N7525	100	2.0	4.0	10	0.29	130	1.6
2N7526	-100	-2.0	-4.0	-10	0.96	175	-0.85

- (1) The 2N7521U and 2N7525 are N-channel devices, the 2N7522U and the 2N7526 are P-channel devices.
(2) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

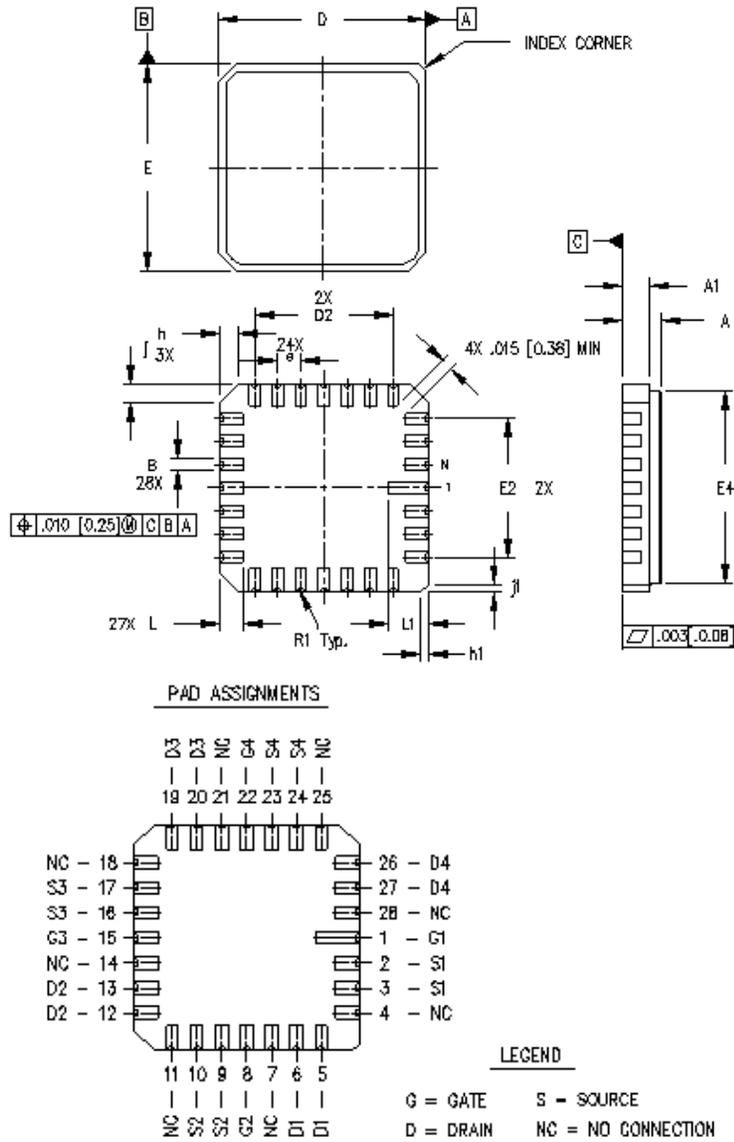
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch> or <https://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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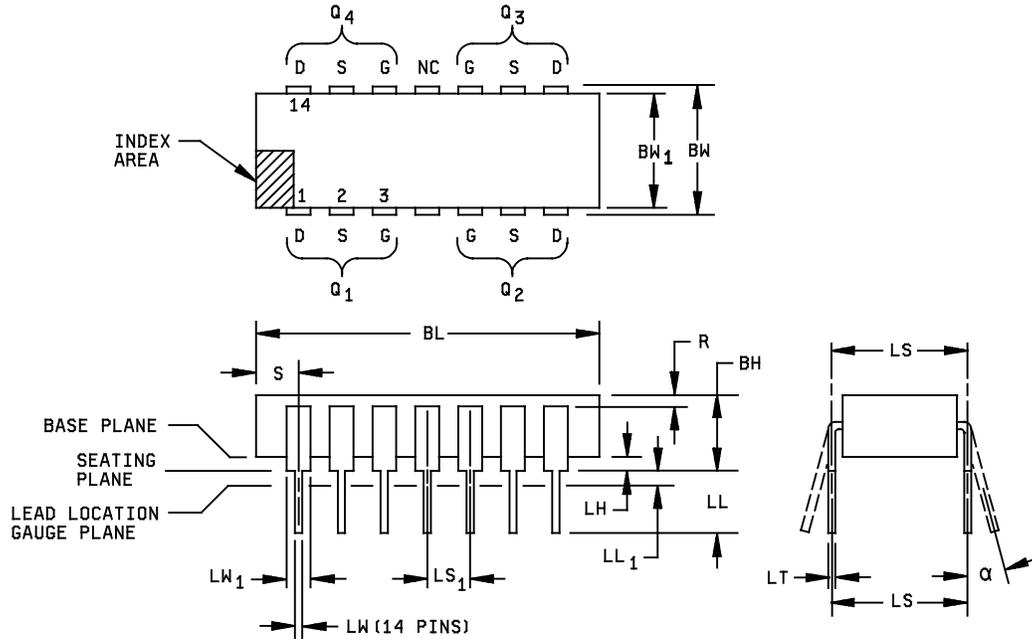
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.075	.095	1.91	2.41
A1	.054	.066	1.37	1.68
B	.020	.030	0.51	0.76
D	.440	.460	11.18	11.68
D2	.300		7.62	
E	.440	.460	11.18	11.68
E2	.300		7.62	
E4	.413	.419	10.49	10.64
e	.050 BSC		1.27 BSC	
h	.040 BSC		1.02 BSC	
h1	.010	.020	0.26	0.50
j	.040 BSC		1.02 BSC	
j1	.010	.020	0.26	0.50
L	.044	.056	1.12	1.42
L1	.079	.091	2.01	2.31
N	28		28	
R1	.007	.011	.178	.279

NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- All terminals are isolated from the case.
- N is the quantity of terminal positions.
- The package meet dimension A without solder. Maximum allowable solder thickness is .006 inch (0.15 mm).
- Applied solder to the terminals will increase flatness tolerance by additional .004 inch (0.10 mm).
- All four Q1 through Q4 are un-committed, either all N-channel (2N7521U) or all P-channel (2N7522U).

FIGURE 1. Dimensions and configuration of leadless chip carrier (MS-004CC).

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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.105	.175	2.67	4.45	
LH	.025	.055	0.64	1.40	
LW	.015	.021	0.381	0.533	
LW ₁	.038	.060	0.97	1.52	
LT	.008	.012	0.203	0.305	
BL	.690	.770	17.53	19.56	
BW	.290	.325	7.37	8.26	
BW ₁	.280	.310	7.11	7.87	

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS	.300 TP		7.62 TP		
LS ₁	.100 TP		2.54 TP		
LL	.125	.175	3.18	4.45	
LL ₁	.000	.030	0.00	0.76	
α	0°	15°	0°	15°	
R	.010		0.25		
S	.030	.095	0.76	2.41	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. All four Q1 through Q4 are un-committed, either all N-channel (2N7525) or all P-channel (2N7526).

FIGURE 2. Dimensions and configuration dual in line (MO-036AB).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 and 2.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

* 3.6 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 Single event effects SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area graph shown herein. End-point measurements shall be in accordance with table III.

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* 4.3 Screening (JANTXV and JANS levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E- IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} test (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} test (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
7	Optional.	Optional.
9	Subgroup 2 of table I herein I _{DSS1} , I _{GSSF1} , I _{GSSR1} , as a minimum	Subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} , subgroup 2 of table I herein. ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} , subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein, ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein, ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.
14	Required.	Required.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D1}$.
- b. Peak gate voltage (V_{GS})..... 12 V dc.
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature +25°C, +10°C, -5°C.
- e. Inductance: $L = \left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage $V_{DD} = 25$ V dc.

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μ s max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) and table E-VIb (JANTXV) of MIL-PRF-19500, and herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM qualification may be performed anytime prior to lot formation.
B4	1042	The heating cycle shall be 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum;
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 240$ hours minimum.
B5	2037	Bond strength; test condition A.

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4.4.2.2 Group B inspection, table E-VIb (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum;
B3	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 170 hours minimum; or T_A = +150°C, t = 340 hours minimum.
B3	2037	Test condition A, all internal bond wires for each device shall be pulled separately.
B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, 3 ounce weight; three bends of 15 degrees, not applicable to 2N7521U and 2N7522U.
C5	3161	See 4.3.3, $R_{\theta JA}$ = 60°C/W maximum for 2N7521U, 2N7522U; $R_{\theta JA}$ = 90°C/W maximum for 2N7525, 2N7526.
C6	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 48 hours minimum; or T_A = +150°C, t = 96 hours minimum.
C6	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 500 hours minimum; or T_A = +150°C, t = 1,000 hours minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u> 2N7521U and 2N7522U 2N7525 and 2N7526	3161	See 4.3.3	$Z_{\theta JC}$			$^{\circ}C/W$
Breakdown voltage drain to source 2N7521U and 2N7525 2N7522U and 2N7526	3407	$V_{GS} = 0$ V, bias condition C $I_D = 1$ mA dc $I_D = -1$ mA dc	$V_{(BR)DSS}$	100 -100		V dc V dc
Gate to source voltage (threshold) 2N7521U and 2N7525 2N7522U and 2N7526	3403	$V_{DS} \geq V_{GS}$ $I_D = 1$ mA dc $I_D = -1$ mA dc	$V_{GS(TH)1}$	2.0 -2.0	4.0 -4.0	V dc V dc
Gate current 2N7521U, 2N7525 2N7522U, 2N7526	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSSF1}		100 -100	nA dc nA dc
Gate current 2N7521U, 2N7525 2N7522U, 2N7526	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSSR1}		-100 100	nA dc nA dc
Drain current 2N7521U and 2N7525 2N7522U and 2N7526	3413	$V_{GS} = 0$ V, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		10 -10	μ A dc μ A dc
Static drain to source on-state resistance 2N7521U 2N7522U 2N7525 2N7526	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$ $V_{GS} = 12$ V dc $V_{GS} = -12$ V dc $V_{GS} = 12$ V dc $V_{GS} = -12$ V dc	$r_{DS(ON)1}$		0.27 0.96 0.29 0.96	Ω Ω Ω Ω
Forward voltage 2N7521U and 2N7525 2N7522U and 2N7526	4011	$V_{GS} = 0$ V, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2 -5.0	V dc V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$ V, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		25 -25	μA dc μA dc
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7521U		$V_{GS} = 12$ V dc			0.54	Ω
2N7522U		$V_{GS} = -12$ V dc			1.92	Ω
2N7525		$V_{GS} = 12$ V dc			0.55	Ω
2N7526		$V_{GS} = -12$ V dc			1.82	Ω
High temperature operation		$T_C = T_J = +125^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(TH)2}$			
2N7521U and 2N7525		$I_D = 1$ mA dc		1.0		V dc
2N7522U and 2N7526		$I_D = -1$ mA dc		-1.0		V dc
Low temperature operation		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$	$V_{GS(TH)3}$			
2N7521U and 2N7525		$I_D = 1$ mA dc			5.0	V dc
2N7522U and 2N7526		$I_D = -1$ mA dc			-5.0	V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u>						
Forward transconductance 2N7521U 2N7522U 2N7525 2N7526	3475	$I_D = I_{D2}$, (see 4.5.1) $V_{DD} = 15$ V dc $V_{DD} = -15$ V dc $V_{DD} = 15$ V dc $V_{DD} = -15$ V dc	g_{FS}	3.3 1.9 1.0 1.1		S S S S
Switching time test	3472	$I_D = I_{D1}$, $R_G = 7.5 \Omega$, $V_{DD} = 50$ percent of rated V_{DS} $V_{GS} = 12$ V dc (N-channel); $V_{GS} = -12$ V dc (P-channel)				
Turn-on delay time 2N7521U and 2N7525 2N7522U and 2N7526			$t_{D(on)}$		20 21	ns ns
Rise time 2N7521U and 2N7525 2N7522U and 2N7526			t_r		24 17	ns ns
Turn-off delay time 2N7521U and 2N7525 2N7522U and 2N7526			$t_{D(off)}$		32 40	ns ns
Fall time 2N7521U and 2N7525 2N7522U and 2N7526			t_f		90 90	ns ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4, $t_p = 10$ ms min. $V_{DS} = 80$ percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{DD} = 50$ percent of rated V_{DS} $V_{GS} = 12$ V dc (N-channel); $V_{GS} = -12$ V dc (P-channel)	$Q_{G(ON)}$			
On-state gate charge						
2N7521U					13.0	nC
2N7522U					17.0	nC
2N7525				11.0	nC	
2N7526				13.4	nC	
Gate to source charge			Q_{GS}			
2N7521U					4.0	nC
2N7522U					4.4	nC
2N7525					3.0	nC
2N7526				3.7	nC	
Gate to drain charge			Q_{GD}			
2N7521U					3.9	nC
2N7522U					3.9	nC
2N7525					4.2	nC
2N7526				3.0	nC	
Reverse recovery time	3473	$di/dt = -100$ A/ μ s, $I_D = I_{D1}$	t_{rr}			
2N7521U		$V_{DD} \leq 50$ V			173	ns
2N7522U		$V_{DD} \leq -50$ V			110	ns
2N7525		$V_{DD} \leq 50$ V			138	ns
2N7526		$V_{DD} \leq -50$ V		86	ns	

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroups 2 and 6.
- Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F		R and F		
				Min	Max	Min	Max	
<u>Subgroup 1</u> Not applicable								
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$						
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	$V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V (N-channel)}$ $V_{GS} = -12\text{ V (P-channel)}$						
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	$V_{GS} = 0\text{ V};$ $V_{DS} = 80\text{ percent of rated } V_{DS}$ (pre-irradiation)						
End-point electricals								
Breakdown voltage, drain to source 2N7521U, 2N7525 2N7522U, 2N7526	3407	$V_{GS} = 0\text{ V}; I_D = 1\text{ mA};$ bias condition C	$V_{(BR)DSS}$	100 -100		100 -100		V dc V dc
Gate to source voltage (threshold) 2N7521U, 2N7525 2N7522U, 2N7526	3403	$V_{DS} \geq V_{GS}$ $I_D = 1\text{ mA}$	$V_{GS(th)1}$	2.0 -2.0	4.0 -4.0	2.0 -2.0	4.0 -4.0	V dc V dc
Gate current 2N7521U, 2N7525 2N7522U, 2N7526	3411	$V_{GS} = +20\text{ V}; V_{DS} = 0\text{ V}$ bias condition C	I_{GSSF1}		100 -100		100 -100	nA dc nA dc
Gate current 2N7521U, 2N7525 2N7522U, 2N7526	3411	$V_{GS} = -20\text{ V}; V_{DS} = 0\text{ V}$ bias condition C	I_{GSSR1}		-100 100		-100 100	nA dc nA dc
Drain current 2N7521U, 2N7525 2N7522U, 2N7526	3413	$V_{GS} = 0\text{ V}$, bias condition C, $V_{DS} = 80\text{ percent of rated } V_{DS}$	I_{DSS}		10 -10		10 -10	$\mu\text{A dc}$ $\mu\text{A dc}$
Static drain-source on-state voltage 2N7521U 2N7522U 2N7525 2N7526	3405	$I_D = I_{D2}$, condition A pulsed (see 4.5.1) $V_{GS} = 12\text{ V}$ $V_{GS} = -12\text{ V}$ $V_{GS} = 12\text{ V}$ $V_{GS} = -12\text{ V}$	$V_{DS(on)}$		0.783 -1.442 0.290 -0.529		0.783 -1.442 0.290 -0.529	V dc V dc V dc V dc
Forward voltage source drain diode 2N7521U, 2N7525 2N7522U, 2N7526	4011	$V_{GS} = 0\text{ V}; I_D = I_{D1}$ bias condition C	V_{SD}		1.2 -5.0		1.2 -5.0	V dc V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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* TABLE III. Group E inspection (all quality levels) - for qualification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
<u>Subgroup 1</u>			12 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071	Test conditions G or H	
Fine leak		Test conditions C or D	
Gross leak			
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			12 devices c = 0
Steady state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 5</u>			
Not applicable			

See footnotes at end of table.

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* TABLE III. Group E inspection (all quality levels) - for qualification only - Continued.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
<u>Subgroup 10</u> Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors	3476	Test conditions shall be derived by the manufacturer	22 devices c = 0
<u>Subgroup 11</u> SEE <u>2/ 3/ 4/</u> Electrical measurements <u>5/</u> SEE irradiation	1080	See figure 5 I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2 Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = 25 ± 5 °C LET = 36.7 – 37.3 MeV-cm ² /mg, range = 36.8 – 39.5 microns, energy = 285 – 309 MeV Insitu bias conditions: $V_{DS} = 100$ V and $V_{GS} = -20$ V Insitu bias conditions: $V_{DS} = -100$ V and $V_{GS} = 20$ V LET = 59.8 – 59.9 MeV-cm ² /mg, range = 32.5 – 32.7 microns, energy = 341 – 344 MeV Insitu bias conditions: $V_{DS} = 100$ V and $V_{GS} = -10$ V $V_{DS} = 35$ V and $V_{GS} = -15$ V $V_{DS} = 25$ V and $V_{GS} = -20$ V Insitu bias conditions: $V_{DS} = -100$ V and $V_{GS} = 15$ V $V_{DS} = -75$ V and $V_{GS} = 17.5$ V $V_{DS} = -25$ V and $V_{GS} = 20$ V LET = 82.3 MeV-cm ² /mg, range = 28.4 – 28.5 microns, energy = 350 – 351 MeV Insitu bias conditions: $V_{DS} = 100$ V and $V_{GS} = -8$ V $V_{DS} = 80$ V and $V_{GS} = -10$ V $V_{DS} = 25$ V and $V_{GS} = -15$ V Insitu bias conditions: $V_{DS} = -100$ V and $V_{GS} = 10$ V $V_{DS} = -30$ V and $V_{GS} = 15$ V	3 devices
2N7521U and 2N7525 2N7522U and 2N7526 2N7521U and 2N7525 2N7522U and 2N7526 2N7521U and 2N7525 2N7522U and 2N7526 Electrical measurements <u>5/</u>		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	

1/ A separate sample for each test shall be pulled.

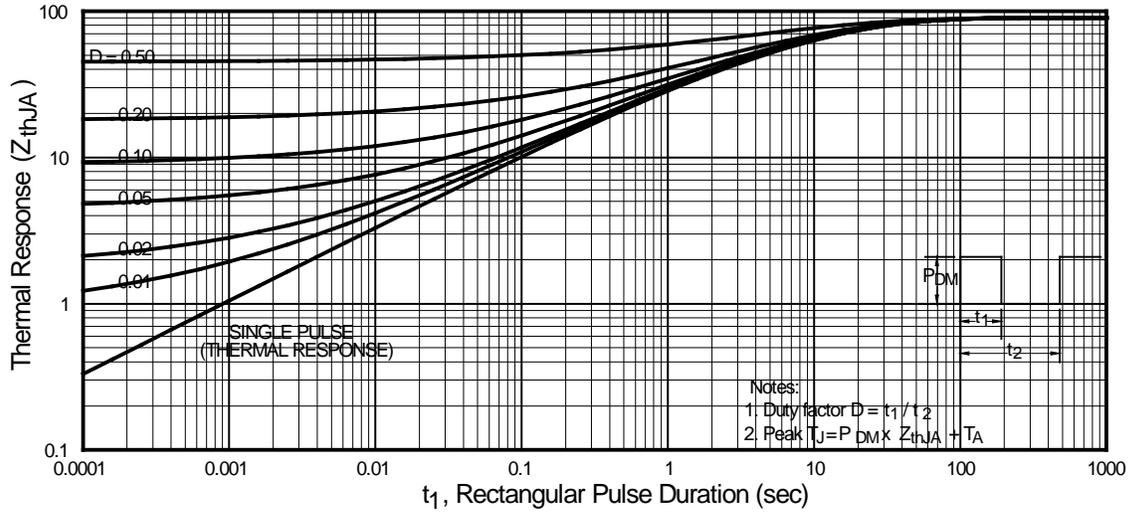
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other performance specifications utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

4/ The sampling plan applies to each bias condition.

5/ Examine I_{GSSF1} , I_{GSSR1} , and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

2N7525 (N-Channel) and 2N7526 (P-Channel)



2N7521U (N-Channel) and 2N7522U (P-Channel)

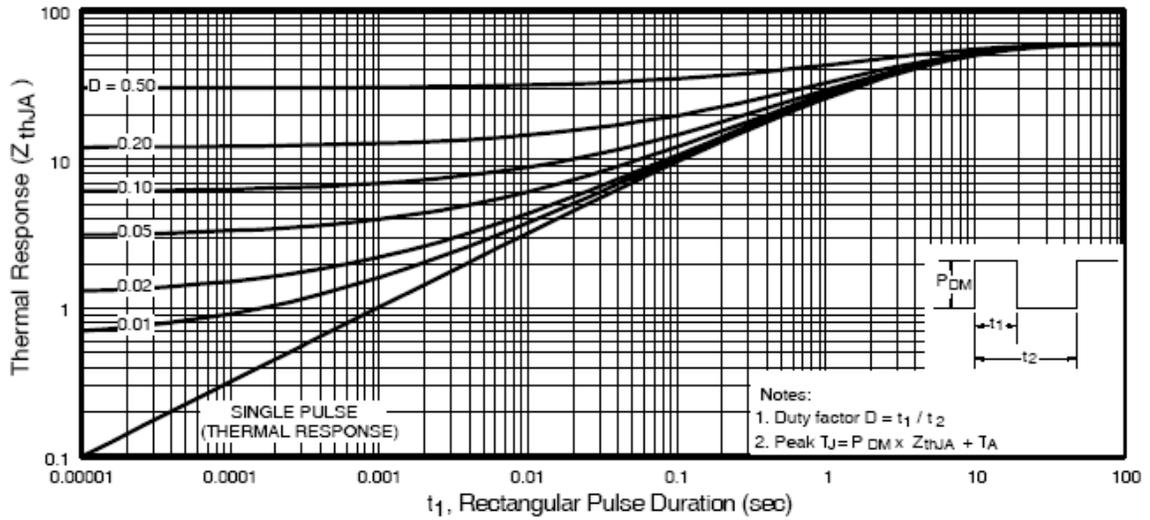
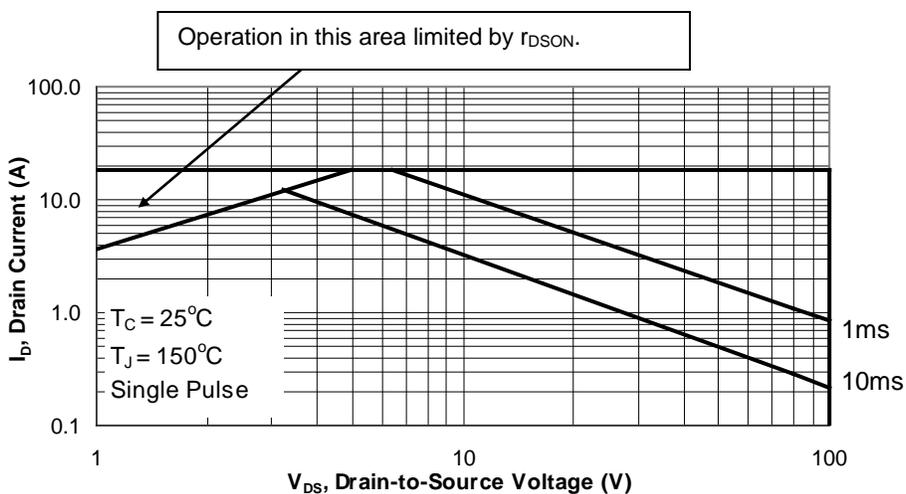


FIGURE 3. Thermal impedance curves.

2N7521U (N-Channel)



2N7522U (P-Channel)

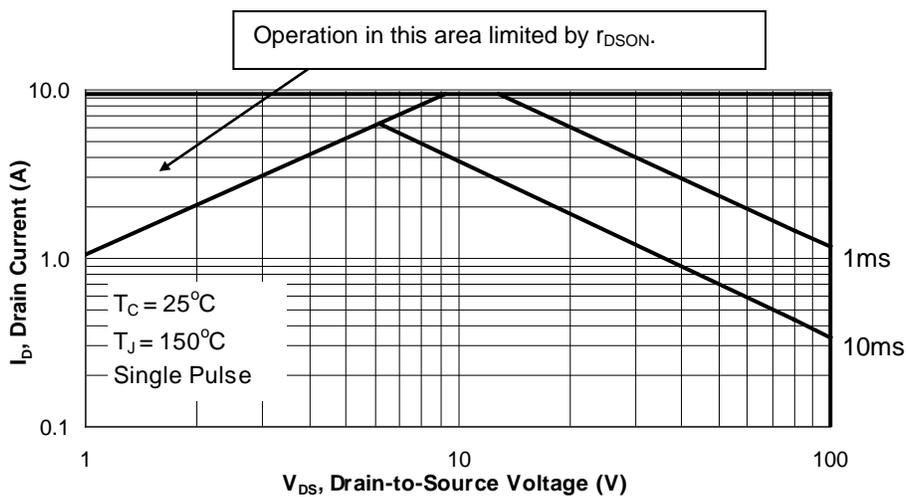
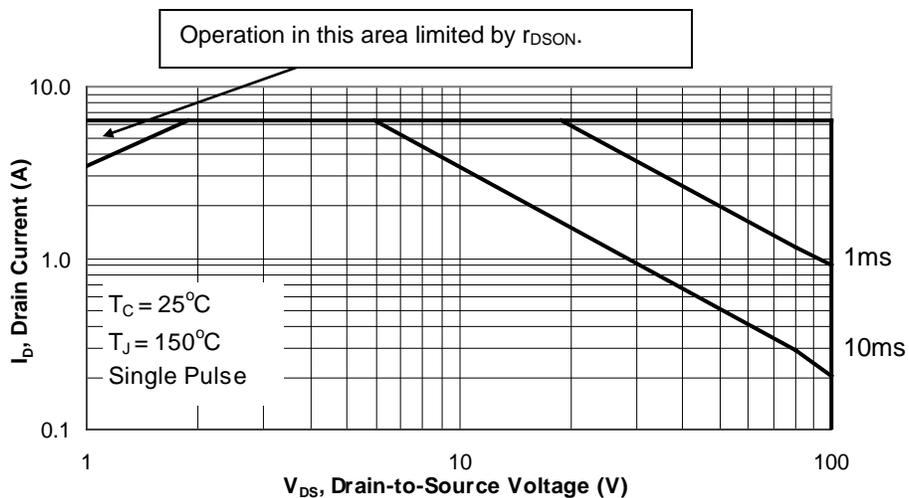


FIGURE 4. Safe operating area graphs.

2N7525 (N-Channel)



2N7526 (P-Channel)

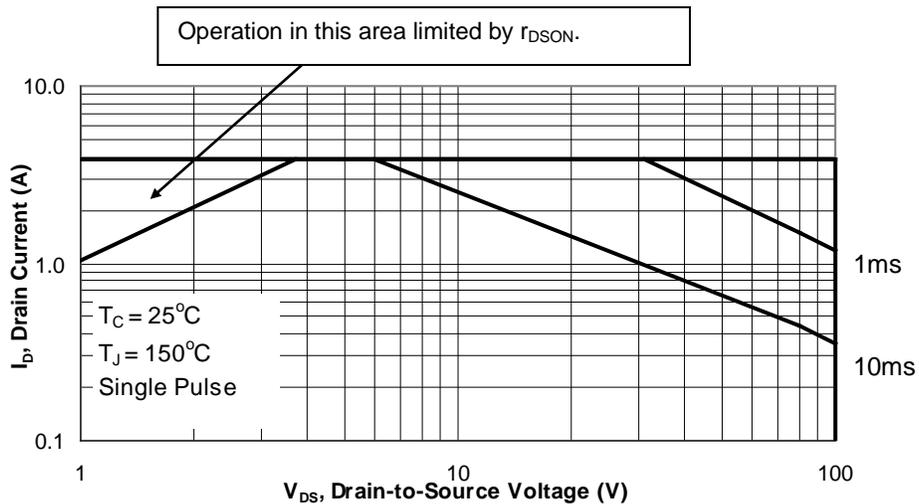
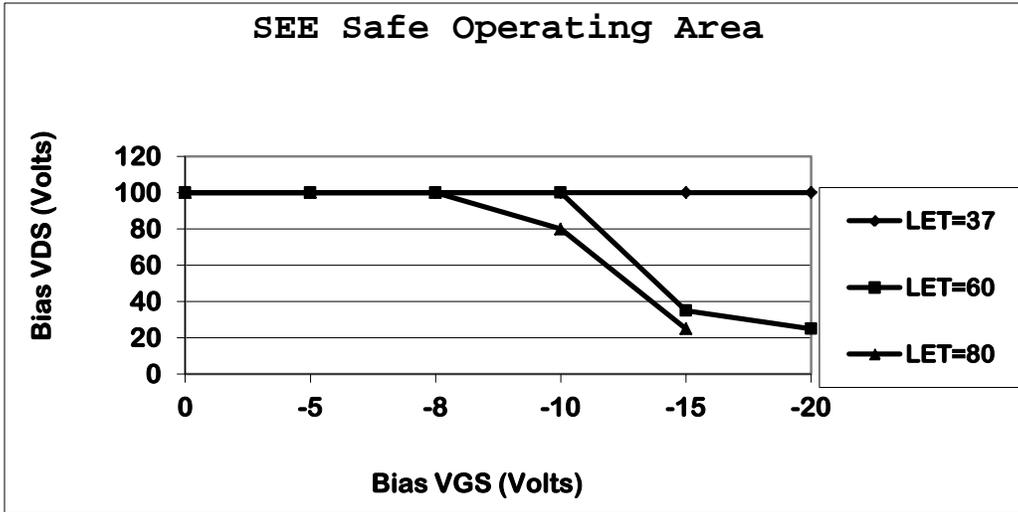


FIGURE 4. Safe operating area graph - Continued.

2N7525 and 2N7521U (N-Channel)



2N7526 and 2N7522U (P-Channel)

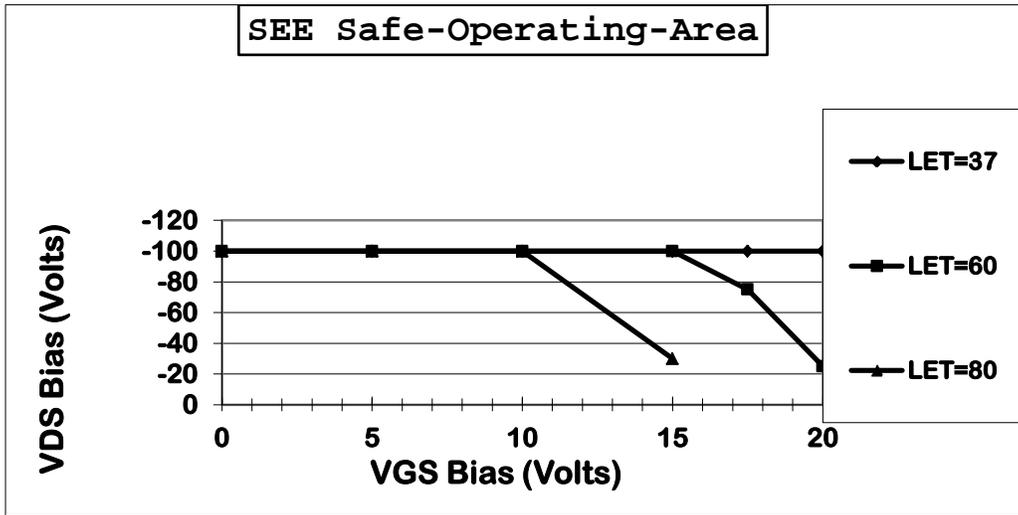


FIGURE 5. SEE safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

* 6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.) The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistics support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Channel	Commercial PIN
2N7521U	N-channel	IRHQ57110
2N7522U	P-channel	IRHQ597110
2N7525	N-channel	IRHG57110
2N7526	P-channel	IRHG597110

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

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* 6.6 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA

Preparing activity:
DLA - CC

(Project 5961-2011-086)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil/> .