The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 October 2013.

INCH-POUND

MIL-PRF-19500/739A
1 July 2013
SUPERSEDING
MIL-PRF-19500/739
24 January 2006

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
* QUAD TRANSISTOR, N-CHANNEL AND P-CHANNEL, SILICON, TYPES 2N7518 AND 2N7518U, JANTXVR, F, AND JANSR, F

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for quad N-channel and P-channel, enhancement-mode, MOSFET, radiation hardened, power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}).

1.2 Physical dimensions. See figure 1, MS-004CC (28-pad ceramic leadless chip carrier) and 2, MO-036AB.

* 1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (free air) (1) T_A = +25°C	P_T (2) T_C = +25°C	$R_{\theta JC}$	$R_{\theta JA}$	V_{DS} = V_{DG}		V_{GS}	
					N-channel	P-channel	N-channel	P-channel
	W	W	°C/W	°C/W	V dc	V dc	V dc	V dc
2N7518	1.39	N/A	N/A	90	100	-100	±20	±20
2N7518U	2.08 (ref.)	10.6	11.8	60 (ref.)	100	-100	±20	±20

Type	I_{D1} (3) T_C = +25°C		I_{D2} T_C = +100°C		I_S		I_{DM} (3)		T_J and T_{STG}
	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	
	A dc	A dc	A dc	A dc	A dc	A dc	A (pk)	A (pk)	°C
2N7518	1.6	-0.85	1.0	-0.55	1.6	-0.85	6.4	-3.4	-55 to
2N7518U	4.6	-2.4	2.9	-1.5	4.6	-2.4	18.4	-9.6	+150

(1) Derate linearly 0.017 W/°C (2N7518U, ref.) or 0.011 W/°C (2N7518) for T_A > +25°C, $P_T = (T_{JMAX} - T_A)/R_{\theta JA}$.
* (2) Derate linearly 0.084 W/°C for T_C > +25°C; $P_T = (T_{JMAX} - T_C) / R_{\theta JC}$.
(3) See figure 3, thermal impedance curves.
(4) I_{DM} = 4 X I_{D1}; I_{D1} as calculated by:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$ (for 2N7518U)

$$I_D = \sqrt{\frac{T_{JM} - T_A}{(R_{\theta JA}) x (R_{DS}(on) \text{ at } T_{JM})}}$$ (for 2N7518)

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mAdc		$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent rated V_{DS}		Max $r_{DS(on)}$ (1) V_{GS} = 12V, I_D = I_{D2}			
							T_J = +25°C		T_J = +150°C	
	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel
	V dc	V dc	V dc Min Max	V dc Min Max	µA dc	µA dc	Ω	Ω	Ω	Ω
2N7518	100	-100	2.0 4.0	-2.0 -4.0	10	10	0.29	0.96	0.58	1.92
2N7518U	100	-100	2.0 4.0	-2.0 -4.0	10	10	0.27	0.96	0.57	2.10

Type	E_{AS} N-channel	E_{AS} P-channel
	mJ	mJ
2N7518	130	175
2N7518U	47	60

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

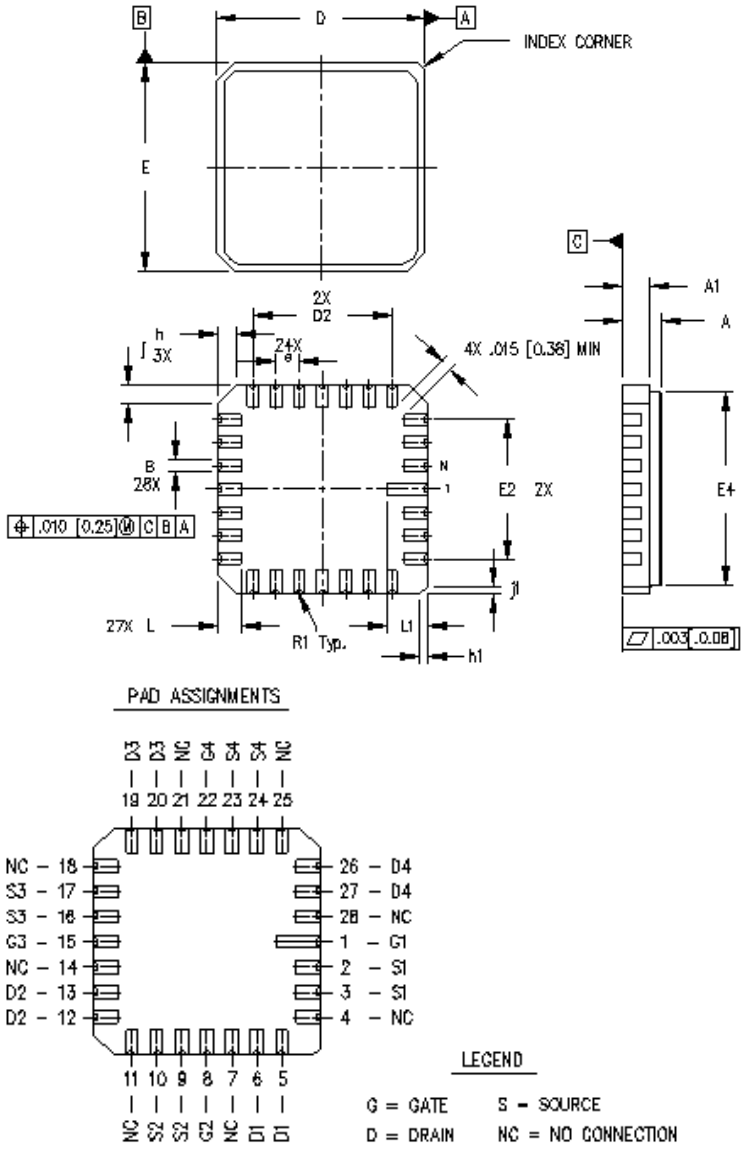
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/ or https://assist.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

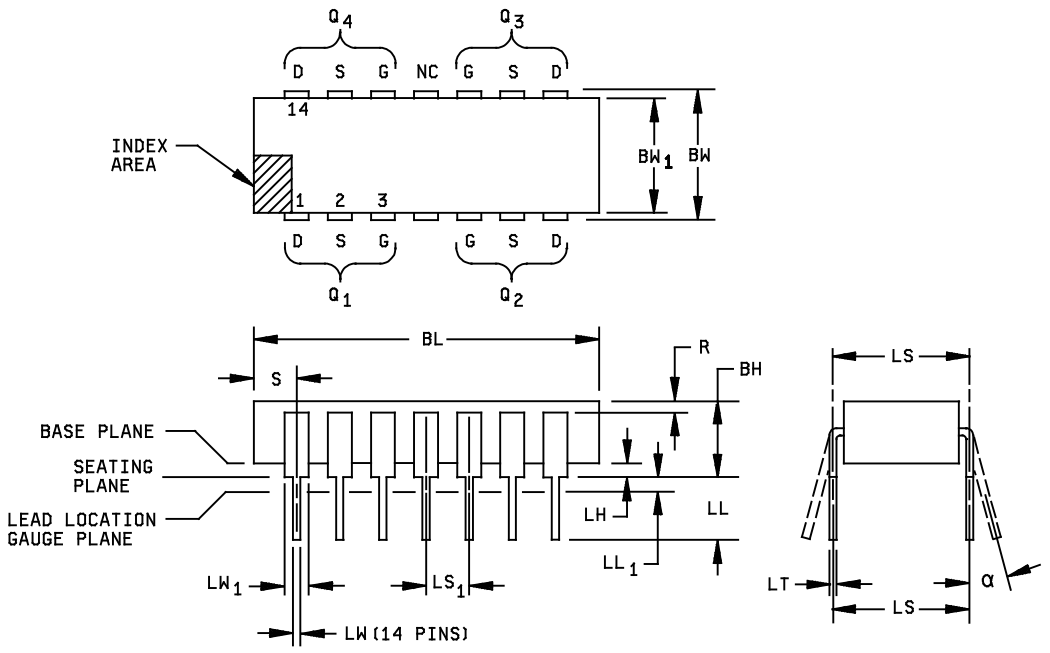
* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.075	.095	1.91	2.41
A1	.054	.066	1.37	1.68
B	.020	.030	0.51	0.76
D	.440	.460	11.18	11.68
D2	.300		7.62	
E	.440	.460	11.18	11.68
E2	.300		7.62	
E4	.413	.419	10.49	10.64
e	.050 BSC		1.27 BSC	
h	.040 BSC		1.02 BSC	
h1	.010	.020	0.26	0.50
j	.040 BSC		1.02 BSC	
j1	.010	.020	0.26	0.50
L	.044	.056	1.12	1.42
L1	.079	.091	2.01	2.31
N	28		28	
R1	.007	.011	.178	.279

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4 N is the quantity of terminal positions.
5. The package shall meet dimension A without solder. Maximum allowable solder thickness is .006 inch (0.15 mm).
6 Applied solder to the terminals will increase flatness tolerance by additional .004 inch (0.10 mm).
7. Q1 and Q4 are N-channel. Q2 and Q3 are P-channel. All are un-committed.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Dimensions and configuration of leadless chip carrier (MS-004CC).



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.105	.175	2.67	4.45	
LH	.025	.055	0.64	1.40	
LW	.015	.021	0.381	0.533	
LW_1	.038	.060	0.97	1.52	
LT	.008	.012	0.203	0.305	
BL	.690	.770	17.53	19.56	
BW	.290	.325	7.37	8.26	
BW_1	.280	.310	7.11	7.87	

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS	.300 TP		7.62 TP		
LS_1	.100 TP		2.54 TP		
LL	.125	.175	3.18	4.45	
LL_1	.000	.030	0.00	0.76	
α	0°	15°	0°	15°	
R	.010		0.25		
S	.030	.095	0.76	2.41	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. Q1 and Q3 are N-channel. Q2 and Q4 are P-channel. All are un-committed.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Dimensions and configuration dual in line (MO-036AB).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS} ..... Rated avalanche current, nonrepetitive.
nC .....nano coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 and figure 2.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq$ or 100 kΩ, whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the performance specification sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, I_{GSSR1}, as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
* (3) Shall be performed anytime after temperature cycling, screen 3a. JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Peak gate voltage (V_{GS})..... 12 V dc.

c. Gate to source resistor (R_{GS}) ..... $25 \leq R_{GS} \leq 200\ \Omega$.

d. Initial case temperature ..... +25°C, +10°C, -5°C.

e. Inductance: ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage ..... V_{DD} = 25 V dc.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μs max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIA (JANS) and table VIB (JANTXV) of MIL-PRF-19500, and herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table VIA (JANS) of MIL-PRF-19500.

	Subgroup	Method	Condition
	B3	1051	Test condition G, 100 cycles.
	B3	2077	SEM qualification may be performed anytime prior to lot formation.
*	B4	1042	Test condition D ; The heating cycle shall be 30 seconds minimum.
	B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum; and accelerated steady-state reverse bias, condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
*	B5	2037	Bond strength; test condition D.

* 4.4.2.2 Group B inspection, table VIB (JANTXV) of MIL-PRF-19500.

	Subgroup	Method	Condition
	B2	1051	Test condition G, 25 cycles.
	B3	1042	Test condition D, the heating cycle shall be 30 seconds minimum.
*	B3	2037	Test condition D, all internal bond wires for each device shall be pulled separately.
	B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

Subgroup	Method	Condition
C2	2036	Test condition E, 3 ounce weight; three bends of 15 degrees for 2N7518, not applicable to 2N7518U.
C5	3161	See 4.3.3, $R_{\theta JA}$ = 90°C/W maximum (2N7518), $R_{\theta JC}$ = 11.8°C/W maximum (2N7518U).
C6	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated, T_A = +175°C, t = 48 hours minimum; or T_A = +150°C, t = 96 hours minimum; and accelerated steady-state reverse bias, condition A, V_{DS} = rated, T_A = +175°C, t = 500 hours minimum; or T_A = +150°C, t = 1,000 hours minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			
2N7518U N & P-channel						°C/W
2N7518 N & P-channel						°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0 V, bias condition C	$V_{(BR)DSS}$			
N-channel		I_D = 1 mA dc		100		V dc
P-channel		I_D = -1 mA dc		-100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(TH)1}$			
N-channel		I_D = 1 mA dc		2.0	4.0	V dc
P-channel		I_D = -1 mA dc		-2.0	-4.0	V dc
Gate current N-channel	3411	V_{GS} = +20V dc, bias condition C, V_{DS} = 0 V	I_{GSSF1}		+100	nA dc
Gate current P-channel	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0 V	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}			
N-channel					10	µA dc
P-channel					-10	µA dc
Static drain to source on state resistance	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7518U N-channel		V_{GS} = 12V dc			0.27	Ω
2N7518U P-channel		V_{GS} = -12V dc			0.96	Ω
2N7518 N-channel		V_{GS} = 12V dc			0.29	Ω
2N7518 P-channel		V_{GS} = -12V dc			0.96	Ω
Forward voltage	4011	V_{GS} = 0 V, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}			
N-channel					1.2	V dc
P-channel					-5.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}			
N-channel					25	µA dc
P-channel					-25	µA dc
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7518U N-channel		V_{GS} = 12 V dc			0.54	Ω
2N7518U P-channel		V_{GS} = -12 V dc			1.92	Ω
2N7518 N-channel		V_{GS} = 12 V dc			0.55	Ω
2N7518 P-channel		V_{GS} = -12 V dc			1.82	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(TH)2}$			
N-channel		I_D = 1 mA dc		1.0		V dc
P-channel		I_D = -1 mA dc		-1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$	$V_{GS(TH)3}$			
N-channel		I_D = 1 mA dc			5.0	V dc
P-channel		I_D = -1 mA dc			-5.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, (see 4.5.1),	g_{FS}			
2N7518U N-channel		V_{DD} = 15 V dc		3.3		S
2N7518U P-channel		V_{DD} = -15 V dc		1.9		S
2N7518 N-channel		V_{DD} = 15 V dc		1.0		S
2N7518 P-channel		V_{DD} = -15 V dc		1.1		S
Switching time test	3472	$I_D = I_{D1}$, R_G = 7.5 Ω, V_{DD} = 50 percent of rated V_{DS} V_{GS} = 12 V dc (N-channel); V_{GS} = -12 V dc (P-channel)				
Turn-on delay time			$t_{D(on)}$			
N-channel					20	ns
P-channel					21	ns
Rise Time			t_r			
N-channel					24	ns
P-channel					17	ns
Turn-off delay time			$t_{D(off)}$			
N-channel					32	ns
P-channel					40	ns
Fall time			t_f			
N-channel					90	ns
P-channel					90	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4 t_p = 10 ms min. V_{DS} = 80 percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B. $I_D = I_{D1}$, V_{DD} = 50 percent of rated V_{DS}, V_{GS} = 12 V dc (N-channel); V_{GS} = -12 V dc (P-channel)				
On-state gate charge			$Q_{G(ON)}$			
2N7518U N-channel					13.0	nC
2N7518U P-channel					17.0	nC
2N7518 N-channel					11.0	nC
2N7518 P-channel					13.4	nC
Gate to source charge			Q_{GS}			
2N7518U N-channel					4.0	nC
2N7518U P-channel					4.4	nC
2N7518 N-channel					3.0	nC
2N7518 P-channel					3.7	nC
Gate to drain charge			Q_{GD}			
2N7518U N-channel					3.9	nC
2N7518U P-channel					3.9	nC
2N7518 N-channel					4.2	nC
2N7518 P-channel					3.0	nC
Reverse recovery time	3473	di/dt = -100 A/µs, $I_D = I_{D1}$	t_{rr}			
2N7518U N-channel		$V_{DD} \leq 50$ V			173	ns
2N7518U P-channel		$V_{DD} \leq -50$ V			110	ns
2N7518 N-channel		$V_{DD} \leq 50$ V			138	ns
2N7518 P-channel		$V_{DD} \leq -50$ V			86	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B Subgroups 3 and 4 (JANS).
Group B Subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
				R and F		R and F		
	Method	Conditions		Min	Max	Min	Max	
Subgroup 1								
Not applicable								
Subgroup 2		T_C = + 25°C						
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{DS} = 0 V V_{GS} = 12 V (N-channel) V_{GS} = -12 V (P-channel)						
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0 V; V_{DS} = 80 % of rated V_{DS} (preirradiation)						
End-point electricals								
Breakdown voltage, drain to source	3407	V_{GS} = 0 V; I_D = 1 mA; bias condition C	$V_{(BR)DSS}$					
N-channel				100		100		V dc
P-channel				-100		-100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = 1 mA	$V_{GS(th)1}$					
N-channel				2.0	4.0	2.0	4.0	V dc
P-channel				-2.0	-4.0	-2.0	-4.0	V dc
Gate current	3411	V_{GS} = +20 V; V_{DS} = 0 V; bias condition C	I_{GSSF1}					
N-channel					100		100	nA dc
P-channel					-100		-100	nA dc
Gate current	3411	V_{GS} = -20 V; V_{DS} = 0 V; bias condition C	I_{GSSR1}					
N-channel					-100		-100	nA dc
P-channel					100		100	nA dc
Drain current	3413	V_{GS} = 0 V; bias condition C V_{DS} = 80% of rated V_{DS} ;	I_{DSS}					
N-channel					10		10	µA dc
P-channel					-10		-10	µA dc
Static drain-source on-state voltage	3405	I_D = I_{D2}, condition A; pulsed (see 4.5.1)	$V_{DS(on)}$					
2N7518U N-channel		V_{GS} = 12 V			0.783		0.783	V dc
2N7518U P-channel		V_{GS} = -12 V			-1.442		-1.442	V dc
2N7518 N-channel		V_{GS} = 12 V			0.290		0.290	V dc
2N7518 P-channel		V_{GS} = -12 V			-0.529		-0.529	V dc
Forward voltage source drain diode	4011	V_{GS} = 0 V; I_D = I_{D1}; bias condition C	V_{SD}					
N-channel					1.2		1.2	V dc
P-channel					-5.0		-5.0	V dc

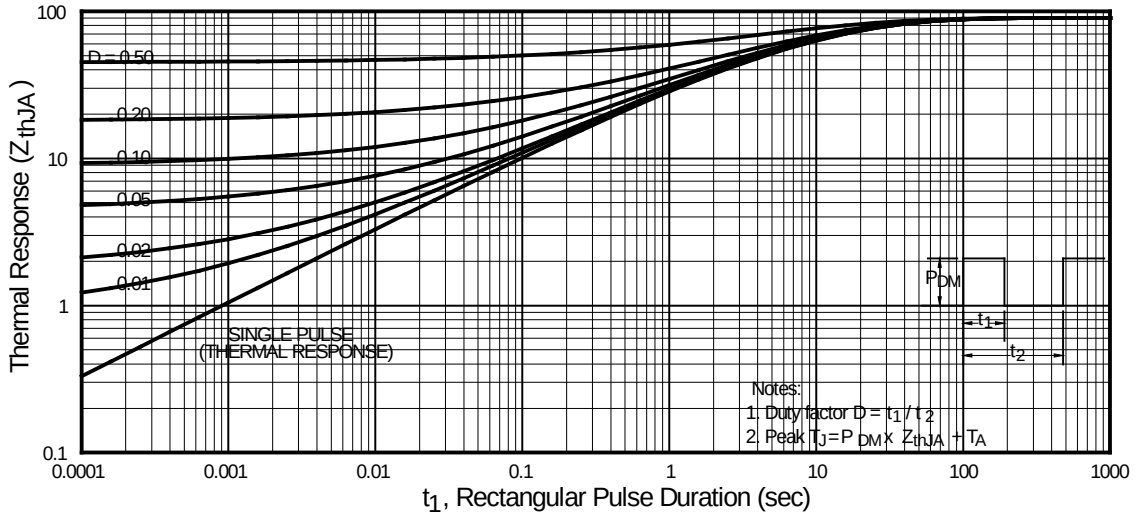
1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package, or in any qualified package, that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
Subgroup 1			12 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			12 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Not applicable			
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
Subgroup 11			
SEE 2/ 3/	1080	See MIL-STD-750 method 1080.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LET's.

2N7518 (N-channel and P-channel)



2N7518U (N-channel and P-channel)

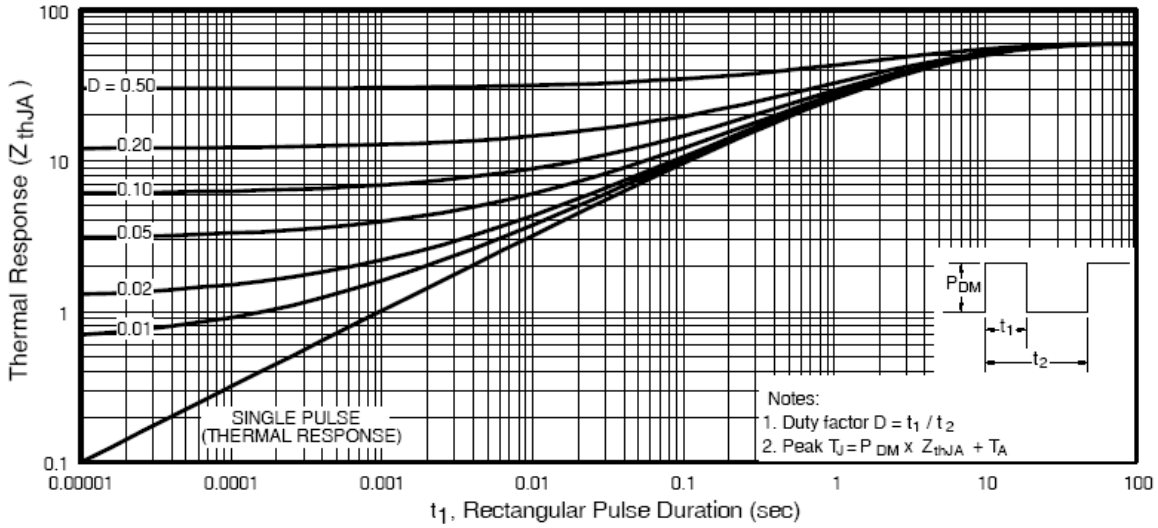
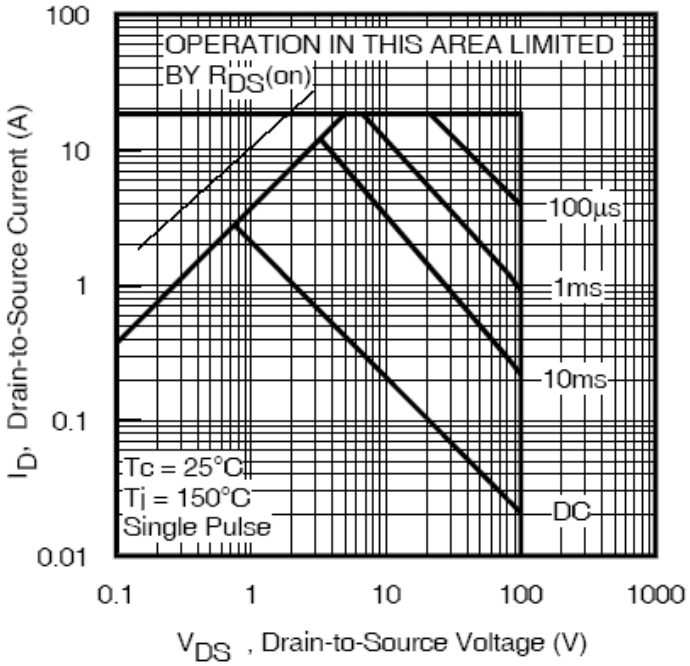
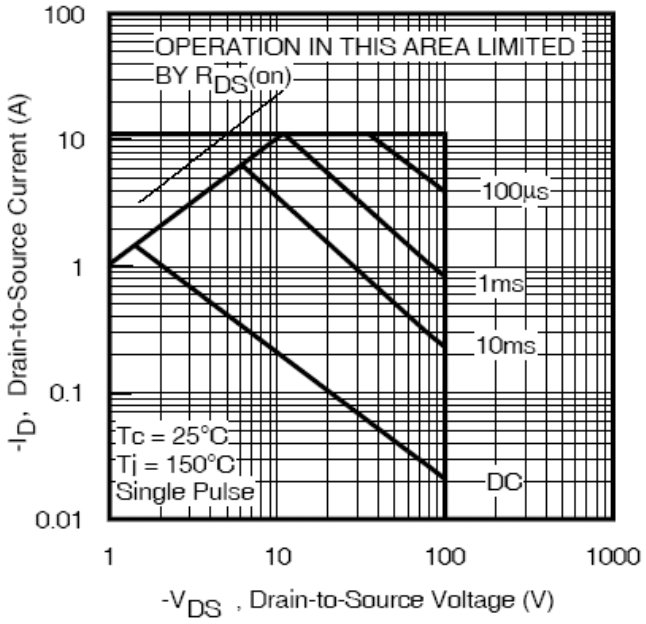


FIGURE 3. Thermal impedance curves

2N7518 N-channel



2N7518 P-channel



* FIGURE 4. Safe operating area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.1).

d. Product assurance level and type designator.

* e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

* f. If SEE testing data is desired, it should be specified in the contract or order.

* g. If specific SEE characterization conditions are desired (see section 6.6 and table IV), manufacturer's cage code should be specified in the contract or order.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Commercial PIN
2N7518U 2N7518	IRHQ567110 IRHG567110

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

* 6.6 Application data.

* 6.6.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements method 1080 of MIL-STD-750 and as specified herein. Since each manufacturer's characterization conditions can be different, the MIL-STD-750 method 1080 conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

* TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
No current qualified sources	SEE 1/	1080	See MIL-STD-750, method 1080 and SEE graphs.	3 devices
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

* 6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activity:
Air Force - 99

Preparing activity:
DLA - CC

(Project 5961-2013-041)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.