The documentation and process conversion measures necessary to comply with this revision shall be completed by 27 November 2023.

INCH-POUND

MIL-PRF-19500/730C
w/AMENDMENT 3
25 August 2023
SUPERSEDING
MIL-PRF-19500/730C
w/AMENDMENT 2
15 December 2022

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, DUAL, CENTER TAP,
TYPES 1N7037CCU1, 1N7043CAT1, 1N7043CCT1, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, Schottky power rectifier diodes. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (U1) and figure 2 (TO-254AA).

1.3 Maximum ratings. Unless otherwise specified, maximum ratings (T_A = +25°C).

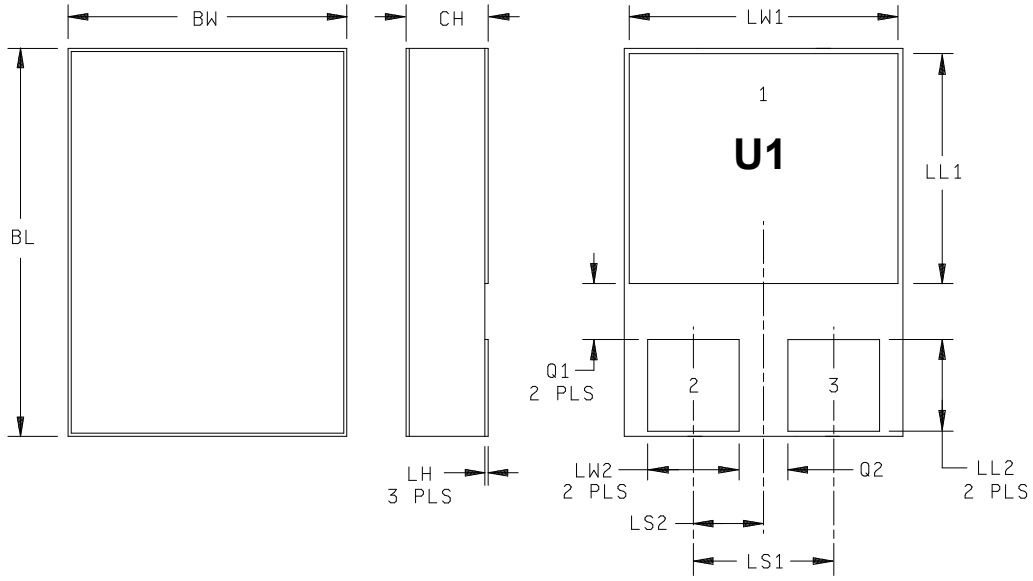
Column 1	Column 2	Column 3	Column 4	Column 5		Column 6
Types (1)	V_{RWM}	I_O (1) (2) T_C = +100°C	I_{FSM} (3) t_p = 8.3 ms, T_C = +25°C	$R_{\theta JC}$ (2)	$R_{\theta JC}$ (3)	T_{STG} and T_J
	V dc	A dc	A (pk)	°C/W	°C/W	°C
1N7037CCU1	100	35	250	0.8	1.6	-65 to +150
1N7043CCT1 1N7043CAT1	100	35	175	1.15	2.3	

(1) See temperature-current derating curves on figures 3 and 4.
(2) For each package.
(3) For each leg, see figures 5 and 6.

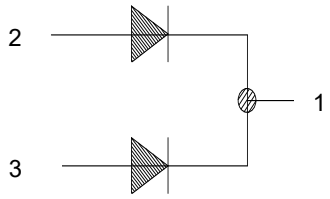
1.4 Primary electrical characteristics. $R_{\theta JC}$ = 0.8°C/W maximum entire package for 1N7037CCU1, $R_{\theta JC}$ = 1.15°C/W maximum entire package for 1N7043CCT1 and 1N7043CAT1.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A
FSC 5961

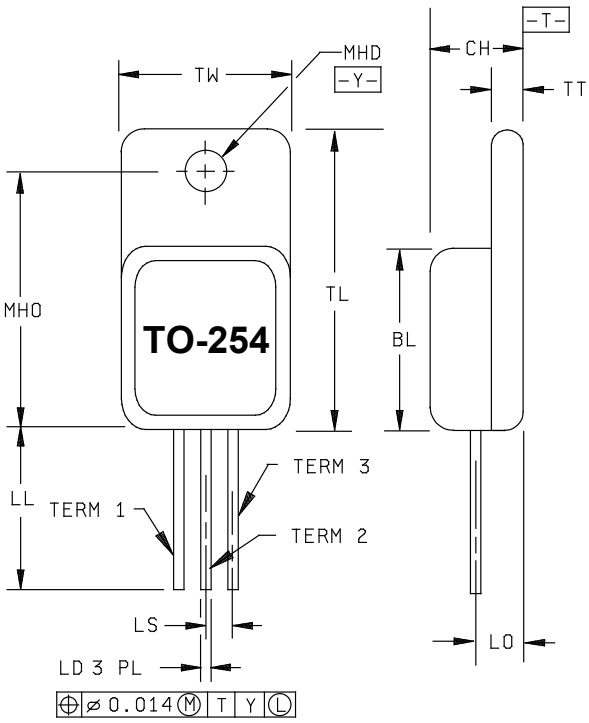


Symbol	Dimensions			
	Inches	Inches	mm	mm
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
* CH	.129	.141	3.28	3.58
LH	.010	.020	0.26	0.51
LL1	.410	.420	10.41	10.67
LL2	.152	.162	3.86	4.12
LS1	.200	.220	5.08	5.59
LS2	.100	.110	2.54	2.79
LW1	.370	.380	9.40	9.65
LW2	.135	.145	3.43	3.68
Q1	.030		0.76	
Q2	.035		0.89	

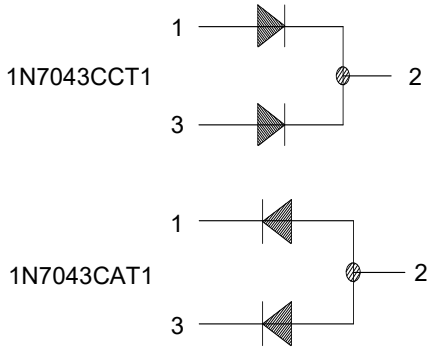


NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.

FIGURE 1. Dimensions and configuration 1N7037CCU1.



Ltr	Dimensions			
	Inches	Inches	mm	mm
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84



1N7043CCT1	1N7043CAT1
TERM 1 = ANODE	TERM 1 = CATHODE
TERM 2 = CATHODE	TERM 2 = ANODE
TERM 3 = ANODE	TERM 3 = CATHODE

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.

FIGURE 2. Dimensions and configuration 1N7043CAT1 and 1N7043CCT1 (TO-254AA).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level designators. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: level "JAN", "JANTX", "JANTXV", and "JANS".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows: "7037" and "7043".

1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN for this specification sheet.

CC	Indicates a dual, common cathode, die configuration.
CA	Indicates a dual, common anode, die configuration.
U1	Indicates a 3 pad surface mount package (see figure 1).
T1	Indicates a 3 pin, through hole mount, TO-254AA package (see figure 2).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* MIL-STD-883 - Test Method Standard for Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (U1) and figure 2 herein. Methods used for electrical isolation of the terminal feedthroughs for the TO-254 shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Polarity. Polarity and terminal configuration shall be in accordance with figures 1 and 2 herein.

3.4.2 Lead material, finish, and formation. Lead material shall be Kovar or Alloy 52; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation, material, or finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

* 3.4.4 Silicone die coating. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883, on each lot of silicon die coating for its intended applications.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3 and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.3 Silicone die coating. When silicon die coating is used, method 5011 of MIL-STD-883 shall be performed on that coating in the full MIL-PRF-19500 qualification process.

4.3 Screening (JANS, JANTXV and JANTX levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTX and JANTXV levels
3b	Condition A, one pulse, tp = 8.3 ms, I_O = 0, V_{RWM} = 0, I_{FSM} = see 1.3 herein.	Condition A, one pulse, tp = 8.3 ms, I_O = 0, V_{RWM} = 0, I_{FSM} = see 1.3 herein.
(1) 3c	Thermal impedance (see 4.3.2).	Thermal impedance (see 4.3.2).
3d	Avalanche energy test (see 4.3.3).	Avalanche energy test (see 4.3.3).
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.5)	Not applicable
9, 10	Not applicable.	Not applicable.
11	V_{F1} and I_{R1}	V_{F1} and I_{R1}
12	See 4.3.1, 240 hours, minimum.	See 4.3.1, 48 hours minimum.
13	Subgroup 2 and 3, of table I herein, V_{F1} and I_{R1}, excluding thermal impedance; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ± 100 percent from the initial value or ±500 uA, whichever is greater.	Subgroup 2, of table I herein excluding thermal impedance; V_{F1} and I_{R1}; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ± 100 percent from the initial value or ±500 uA, whichever is greater.
14	Required.	Required.
15	Required.	Not applicable.
16	Required.	Not applicable.
(2) 17	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.

(1) Thermal impedance shall be performed any time after screen 3.
(2) Not applicable for U1 package.

4.3.1 Power burn-in conditions. Burn-in conditions are as follows: Method 1038 of MIL-STD-750, test condition A. T_J = +125°C; V_R = 80 V dc.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, and t_{MD}. See table III, subgroup 4, and figures 5 and 6.

4.3.3 Avalanche energy test. The avalanche energy test is to be performed in accordance with method 4064 of MIL-STD-750 using the circuit as shown on figure 7 or equivalent. The Schottky rectifier under test shall be capable of absorbing the reverse energy, as follows: I_{AS} = 1A, Vbr = 100 V minimum, L = 100 µH.

4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage ..... 900 V dc.

b. Duration of application of test voltage ..... 15 seconds (min).

c. Points of application of test voltage ..... All leads to case (bunch connection).

d. Method of connection ..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200V /1.0 mA (min).

f. Maximum leakage current ..... 1.0 mA.

g. Voltage ramp up time ..... 500V /second.

* 4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table E-V of MIL-PRF-19500, and table I herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (JANS) and E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with table II herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

	Subgroup	Method	Condition
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	B4	1037	ΔT_C = +85°C, I_F = 2 A minimum.
	B5	1038	Condition A, V_R = 80 V dc, T_J = +125°C, t = 1,000 hours minimum; heat sinking allowed. As an alternative method a five (5) dice sample from each individual wafer from the wafer lot shall be qualified for 1,000 hours minimum then each conformance inspection lot requires 340 hours minimum when selected from qualified wafers. This option must be approved by the qualifying activity based on data from at least 3 wafer lots. Any change to the die design, or a conformance inspection failure of the alternate method, requires the 3 wafer lot qualification prior to using this alternative method.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1037	ΔT_C = +85°C, I_F = 2 A minimum for 2,000 cycles.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with table II herein.

	Subgroup	Method	Condition
	C2	2036	Condition A, weight = 10 lbs, t = 15 seconds. Not applicable to U1 package.
*	C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	C5	4081	Limit for thermal resistance for 1N7037 is 1.6°C/W for each diode. Limit for thermal resistance for 1N7043 is 2.3°C/W for each diode.
	C6	1037	ΔT_C = +85°C, I_F = 2 A minimum for 6,000 cycles.
	C6	1038	Condition A, V_R = 80 V dc, T_J = +125°C, t = 1,000 hours minimum; heat sinking allowed. As an alternative method a five (5) dice sample from each individual wafer from the wafer lot shall be qualified for 1,000 hours minimum then each conformance inspection lot requires 340 hours minimum when selected from qualified wafers. This option must be approved by the qualifying activity based on data from at least 3 wafer lots. Any change to the die design, or a conformance inspection failure of the alternate method, requires the 3 wafer lot qualification prior to using this alternative method.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 3/	3101	See 4.3.2	$Z_{\theta JX}$			°C/W
Forward voltage	4011	Condition B, Pulsed test (see 4.5.1)	V_{F1}			
1N7037		I_F = 15A (pk)			.90	V
1N7043		I_F = 15A (pk)			.95	V
Forward voltage	4011	Condition B, Pulsed test (see 4.5.1)	V_{F2}			
1N7037		I_F = 35 A(pk)			1.22	V
1N7043		I_F = 35 A(pk)			1.30	V
Reverse current	4016	Condition A or B, DC method	I_{R1}			
1N7037		V_R = 100 V			.5	mA
1N7043		V_R = 100 V			.5	mA
Subgroup 3						
High temperature operation:		T_C = +125 °C				
Forward voltage	4011	Condition B, Pulsed test (see 4.5.1)	V_{F3}			
1N7037		I_F = 35 A(pk)			1.00	V
1N7043		I_F = 35 A(pk)			1.20	V
Reverse current	4016	Condition A or B, DC method;	I_{R2}			
1N7037		V_R = 100 V			15	mA
1N7043		V_R = 100 V			15	mA
Low temperature operation:		T_C = -55°C				
Forward voltage	4011	Condition B, Pulsed test (see 4.5.1)	V_{F4}			
1N7037		I_F = 35 A dc			1.35	V
1N7043		I_F = 35 A dc			1.84	V

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Junction capacitance	4001	V_R = 5 V dc, f = 1 MHz, V_{SIG} = 50 mV (p-p)	C_J		600	pF
Subgroup 5						
Not applicable						
Subgroup 6						
Surge	4066	Condition A, see column 4 of 1.3. Ten surges per diode. 60 seconds between surges. (See 4.5.1)				
Electrical measurements		See table I, subgroup 2 herein				
Subgroup 7						
Insulation resistance	1016	V_R = 500 V dc; all leads shorted; TO-254AA package: V_R applied across leads to case; U1 package: V_R applied across lid to case bottom.	I_R		10	µA
* Scope display evaluation	4023	Condition A, Stable only				
Electrical measurements		See table I, subgroup 2 herein				

1/ For sampling plan, see MIL-PRF-19500.
2/ Each individual diode.
3/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II. Groups B, C, and E delta requirements. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits	Limits	Unit
		Method	Conditions		Min	Max	
1.	Forward voltage	4011	I_F = 15 A (pk), Condition B pulsed (see 4.5.1)	ΔV_{F1}	± 50 mV dc from initial reading.		
2.	Reverse current	4016	Condition A or B, DC method, V_R = 100V	ΔI_{R1}	±100% from initial reading or ±500uA whichever is greater.		

1/ Each individual diode.
2/ The delta measurements for appendix E, table E-VIA (JANS) of MIL-PRF-19500 are as follows:
   a. Subgroup 3, see table II herein, steps 1, and 2.
   b. Subgroup 4, see table II herein, steps 1, and 2.
   c. Subgroup 5, see table II herein, steps 1 and 2.
3/ The delta measurements for appendix E, table E-VIB (JANTX and JANTXV) of MIL-PRF-19500 are as follows:
   a. Subgroup 2, see table II herein, steps 1, and 2.
   b. Subgroup 3, see table II herein, steps 1, and 2.
   c. Subgroup 6, see table II herein, steps 1 and 2.
4/ The delta measurements for appendix E, table E-VII of MIL-PRF-19500 are as follows:
   a. Subgroup 2, see table II herein, steps 1, and 2 for all levels.
   b. Subgroup 3, see table II herein, steps 1 and 2 for all levels.
   c. Subgroup 6, see table II herein, steps 1, and 2 for all levels.
5/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows:
   a. Subgroup 1, see table II herein, steps 1, and 2.
   b. Subgroup 2, see table II herein, steps 1 and 2.
6/ Devices which exceed the table I, limits for this test shall not be accepted.

TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			n = 45, c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55°C to +150°C.	
Electrical measurements		See table I subgroup 2 and delta requirements of table II herein.	
Subgroup 2			n = 45, c = 0
Life test	1048	t = 1,000 hours, T_J = +125°C, V_R = 80 percent rated voltage (see 1.3, column 2 herein).	
Electrical measurements		See table I subgroup 2 and delta requirements of table II herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 10 1/			n = 5, c = 0
Surge	4066		
1N7037		Condition A, T_A = +25°C I_{FSM} = 250 A, 10 surge of 8.3 ms, superimposed on I_O, V_R = 0; I_O = 10 A pk half sine wave, continuous.	
1N7043		Condition A, T_A = +25°C I_{FSM} = 175 A, 10 surge of 8.3 ms, superimposed on I_O, V_R = 0; I_O = 10 A pk half sine wave, continuous.	
Electrical measurements		See table I subgroup 2 (V_F and I_R only).	

1/ Each individual diode.

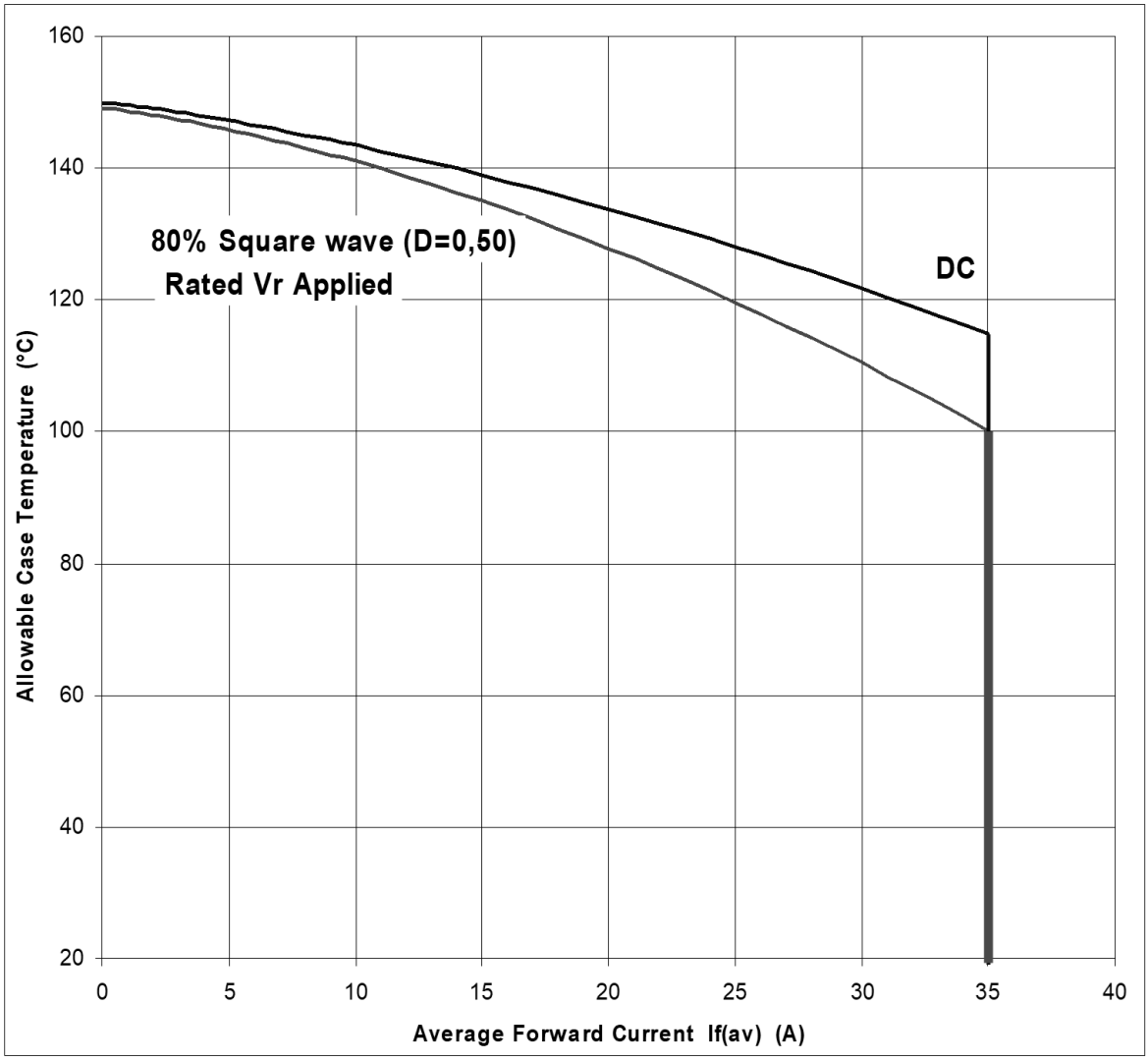


FIGURE 3. Temperature-current derating curve - 1N7037 (entire package).

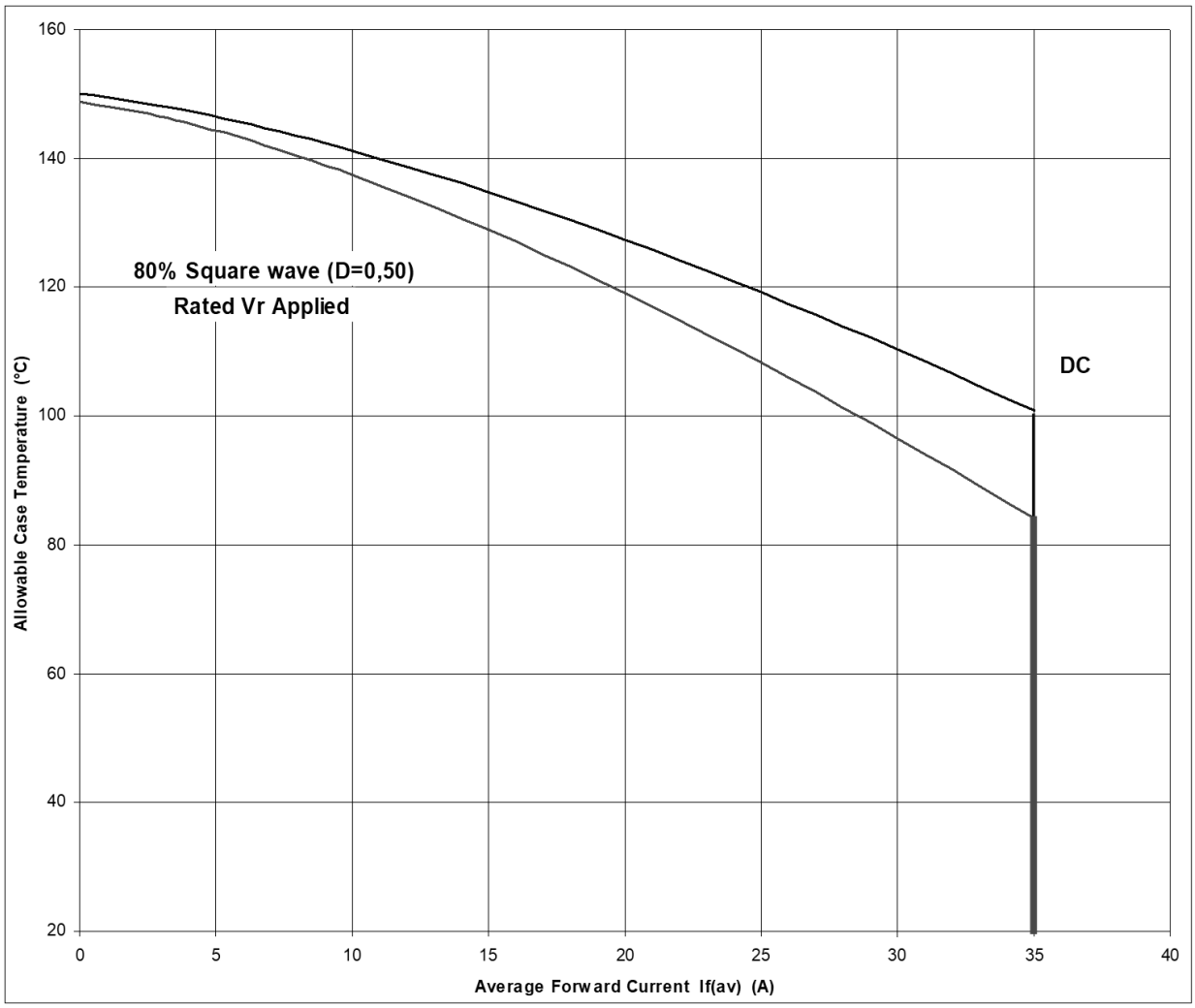


FIGURE 4. Temperature-current derating curve - 1N7043 (entire package).

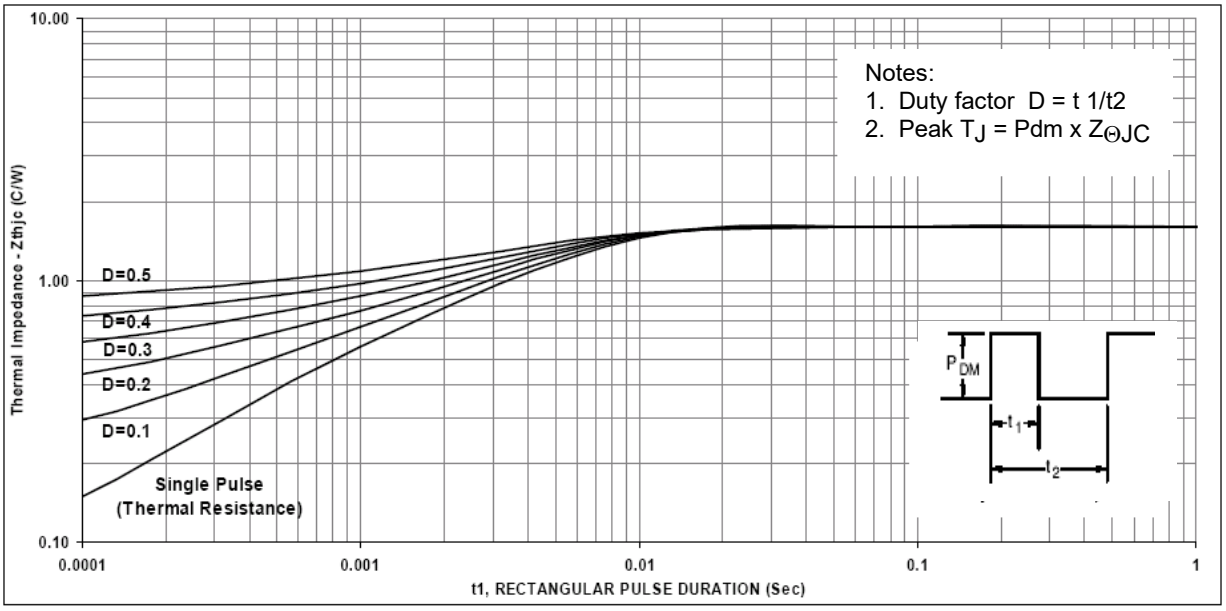


FIGURE 5. Thermal impedance - 1N7037 (for each leg).

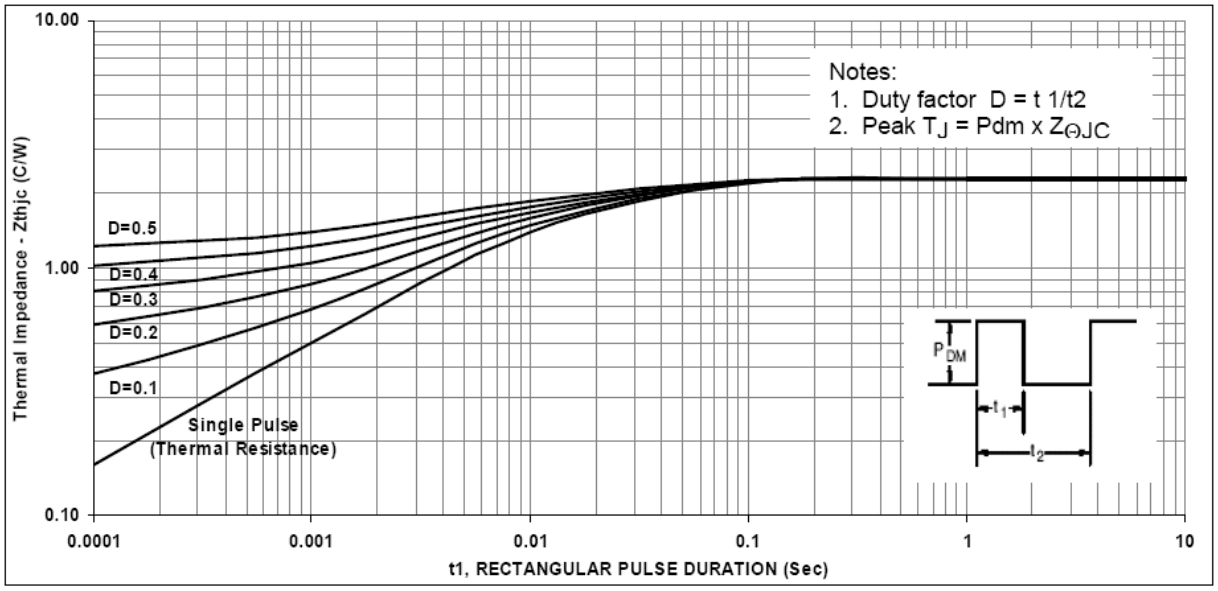
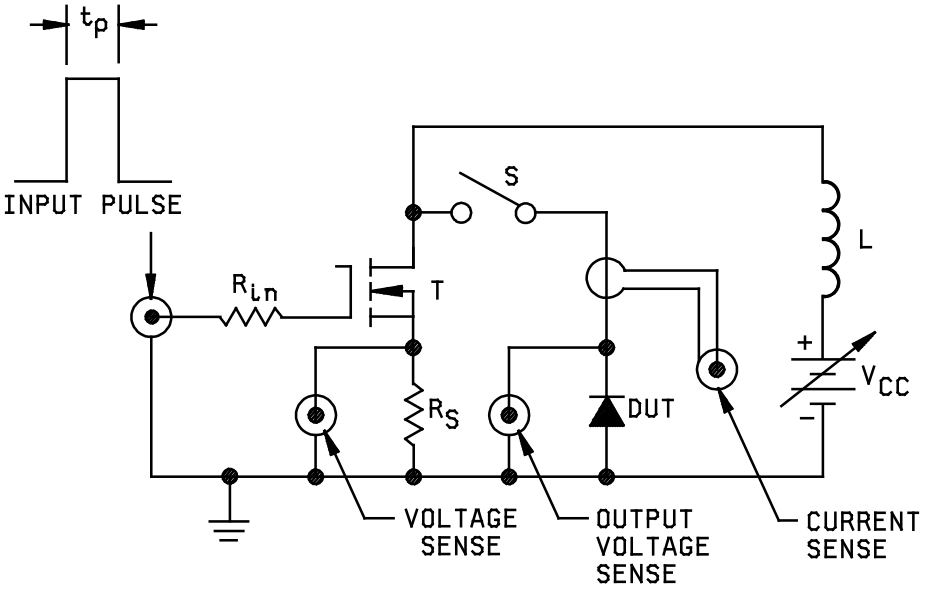


FIGURE 6. Thermal impedance - 1N7043 (for each leg).



Input pulse R_{in} = 50 ohms, 1 watt
V_G = 10 Volts, R_S = 0.1 ohms, 1 watt
Z_G = 50 ohms
L = 100μH
P.W. ≈ 30 μs
Duty cycle ≤ 1 percent, T = IRF250/2N6766 or equivalent

PROCEDURES:
1. With S open, adjust pulse width to test current of 1 amps through R_S.
2. Close S, verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

FIGURE 7. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.2).

d. The complete PIN, see 1.5.

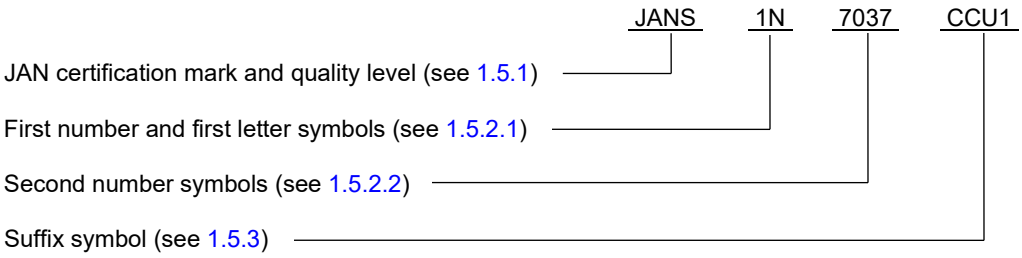
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Cross reference substitution list. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
15CGQ100	JANS, JANTXV, JANTX1N7043CCT1
15JGQ100	JANS, JANTXV, JANTX1N7043CAT1
15CLQ100	JANS, JANTXV, JANTX1N7037CCU1

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

6.6.1 List of Encapsulated device types.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N7037CCU1	JANTX1N7037CCU1	JANTXV1N7037CCU1	JANS1N7037CCU1
JAN1N7043CCT1	JANTX1N7043CCT1	JANTXV1N7043CCT1	JANS1N7043CCT1
JAN1N7043CAT1	JANTX1N7043CAT1	JANTXV1N7043CAT1	JANS1N7043CAT1

6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Air Force - 19

Preparing activity:
DLA - CC

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.