

The documentation and process conversion measures necessary to comply with this document shall be completed by 28 February 2015.

INCH-POUND

MIL-PRF-19500/727C
28 November 2014
SUPERSEDING
MIL-PRF-19500/727B
21 January 2010

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, SWITCHING,
DEVICE TYPES 2N5010 THROUGH 2N5015, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, transistors. Four levels of product assurance are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

* 1.2. Package outlines. The device package for this specification sheet is (TO-5 and TO-39) in accordance with [figure 1](#) and (U4) in accordance with [figure 2](#) for all packaged device types.

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^{\circ}\text{C}$.

Types	I_C	I_B	V_{CBO}	V_{CER}	V_{EBO}	T_J and T_{STG} (1)
	<u>mA dc</u>	<u>mA dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	
2N5010, 2N5010S, U4	200	20	500	500	5	-65 to +200
2N5011, 2N5011S, U4	200	20	600	600	5	-65 to +200
2N5012, 2N5012S, U4	200	20	700	700	5	-65 to +200
2N5013, 2N5013S, U4	200	20	800	800	5	-65 to +200
2N5014, 2N5014S, U4	200	20	900	900	5	-65 to +200
2N5015, 2N5015S, U4	200	20	1000	1000	5	-65 to +200

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

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1.3 Maximum ratings - Continued. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Types	P_T $T_A = +25^\circ\text{C}$ (2) (3)	P_T $T_C = +25^\circ\text{C}$ (2) (3)	$R_{\theta JA}$ (3) (4)	$R_{\theta JC}$ (3) (4)
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>
2N5010 through 2N5015 and 2N5010S through 2N5015S	1	7	175	20
2N5010U4 through 2N5015U4	1	7	175	7

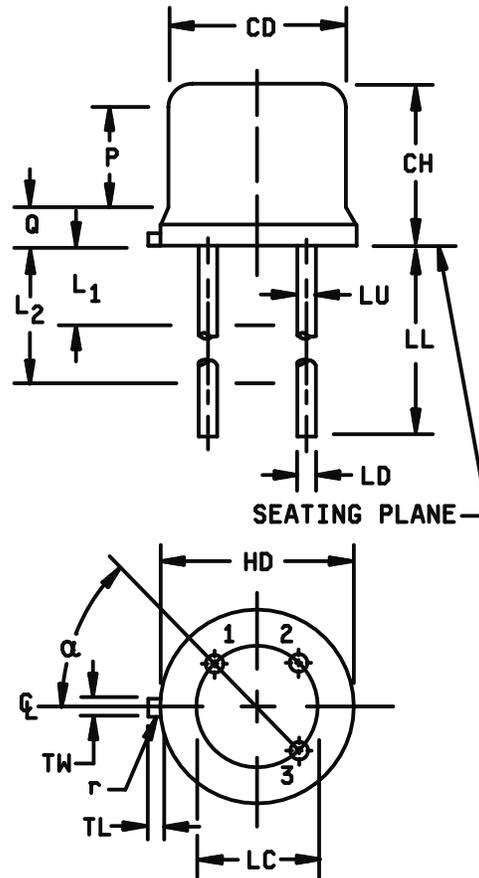
- (1) For derating, see figures 3, 4, and 5.
- (2) See [figure 5](#) for special bias considerations under ambient operation.
- (3) For thermal impedance curves, see figures 6, 7, 8, and 9.
- (4) $T_A = 25^\circ\text{C}$ for (U4) on printed circuit board (PCB), PCB = FR4 .0625 inch (1.59 mm) 1-layer 1-Oz Cu, horizontal, still air, pads (U4) = .067 x .065 inch (1.7 x 1.65 mm) for the two smaller pads and .165 x .135 inch (4.19 x 3.43 mm) for the larger collector pad; $R_{\theta JA}$ with a defined PCB thermal resistance condition included.

1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Types	h_{FE} at $V_{CE} = 10\text{ V dc}$				$V_{CE(sat)1}$ (1) $I_C = 25\text{ mA dc}$ $I_B = 5\text{ mA dc}$	$V_{BE(sat)1}$ (1) $I_C = 25\text{ mA dc}$ $I_B = 5\text{ mA dc}$	$ h_{fe} $ $f = 10\text{ MHz}$	C_{obo} $100\text{ kHz} \leq f \leq 2\text{ MHz}$		
	h_{FE1} $I_C = 25\text{ mA dc}$		h_{FE2} $I_C = 5\text{ mA dc}$						$V_{CE} = 10\text{ V dc}$ $I_C = 25\text{ mA dc}$	$V_{CB} = 10\text{ V dc}$ $I_E = 0$
	min	max	min	max						
2N5010, 2N5010S U4	30	180	10		1.4	1	1	30		
2N5011, 2N5011S, U4	30	180	10		1.5	1	1	30		
2N5012, 2N5012S, U4	30	180	10		1.6	1	1	30		
Types	h_{FE} at $V_{CE} = 10\text{ V dc}$				$V_{CE(sat)1}$ (1) $I_C = 20\text{ mA dc}$ $I_B = 5\text{ mA dc}$	$V_{BE(sat)1}$ (1) $I_C = 20\text{ mA dc}$ $I_B = 5\text{ mA dc}$	$ h_{fe} $ $f = 10\text{ MHz}$	C_{obo} $100\text{ kHz} \leq f \leq 2\text{ MHz}$		
	h_{FE1} $I_C = 20\text{ mA dc}$		h_{FE2} $I_C = 5\text{ mA dc}$						$V_{CE} = 10\text{ V dc}$ $I_C = 20\text{ mA dc}$	$V_{CB} = 10\text{ V dc}$ $I_E = 0$
	min	max	min	max						
2N5013, 2N5013S U4	30	180	10		1.6	1	1	30		
2N5014, 2N5014S, U4	30	180	10		1.6	1	1	30		
2N5015, 2N5015S, U4	30	180	10		1.8	1	1	30		

- (1) Pulsed see [4.5.1](#).

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L ₁		.050		1.27	8,9
L ₂	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		7
	1, 2, 10, 12, 13, 14				

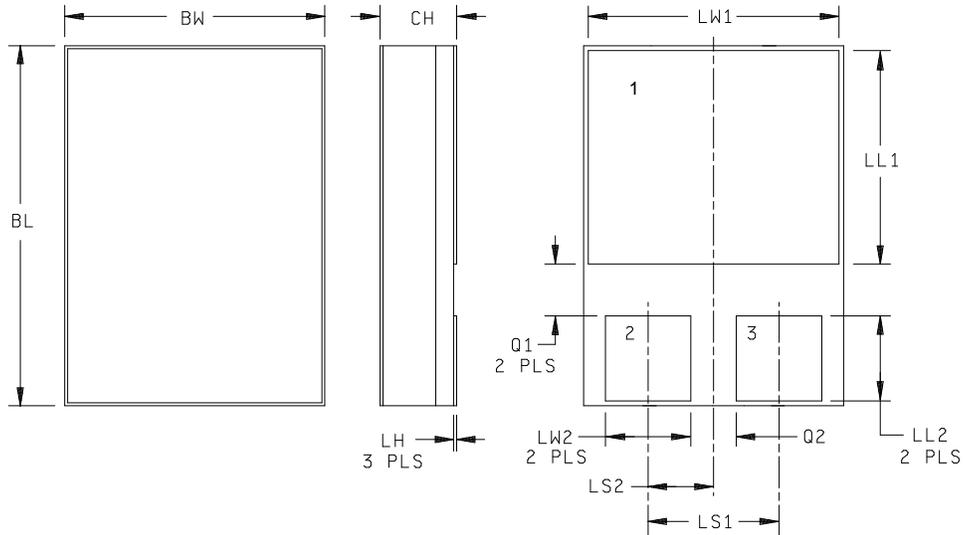


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
8. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For non-S-suffix devices (TO-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For S-suffix types (TO-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions (TO-5 and TO-39).

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.02		0.51
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.085	.125	2.16	3.17
LL2	.045	.075	1.14	1.9
LS1	.070	.095	1.78	2.41
LS2	.035	.048	0.89	1.21
Q1	.03	.070	0.76	1.78
Q2	.02	.035	0.51	0.89
TERM 1	Collector			
TERM 2	Base			
TERM 3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeter equivalents are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to \varnothing x symbology.

FIGURE 2. Physical dimensions, surface mount (U4 version).

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* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

* 1.5.1 JAN brand and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: The base quality level "JAN" that uses no modifiers, "TX", "TXV" and "S".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "5010" through "5015".

* 1.5.2.3 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

S	Indicates a package similar to a TO-39 (see figure 1).
U4	Indicates a 3 pad surface mount package (see figure 2).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

* 3.4 Interface and physical dimensions. The interface requirements and physical dimensions shall be as specified in [MIL-PRF-19500](#) and herein. The device package style is either a TO-5, TO-39 or U4 in accordance with [figure 1](#) and [figure 2](#) for all device types.

* 3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

* 3.4.2 Pin-out. The pin-out of the device shall be as shown on [figure 1](#) and [figure 2](#).

* 3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.2.2, 1.2.3, and [table I](#).

3.6 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

* 3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

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4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see E-table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
2	Optional	Optional
3a	Required	Required
3b	Not applicable	Not applicable
3c	Thermal impedance (transient), method 3131 of MIL-STD-750 (1)	Thermal impedance (transient), method 3131 of MIL-STD-750 (1)
4	Required	Optional
5	Required	Not applicable
8	Required	Not required
9	I_{CBO1} , h_{FE1}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO1} ; h_{FE1} ; ΔI_{CBO1} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE1} = ± 15 percent	I_{CBO1} ; h_{FE1}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent	Subgroup 2 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent
15	Required	Not required
16	Required	Not required

(1) Shall be performed any time after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc. Power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum, rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J , mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Use method 3100 of MIL-STD-750 to measure T_J .

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table II](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein. If alternate screening is being performed in accordance with [MIL-PRF-19500](#), a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with [4.4.2](#)).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#), and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of [MIL-PRF-19500](#) and [4.4.2.1](#). See [4.4.2.2](#) for JAN, JANTX, and JANTXV group B testing.

4.4.2.1 Group B inspection (JANS), table E-VIa of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} \geq 10$ V dc.
B5	1027	$V_{CB} = 10$ V dc; $P_D \geq 100$ percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with table E-VIa of MIL-PRF-19500 , adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a $T_J = +225^\circ\text{C}$ minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of [MIL-PRF-19500](#) shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3 . n = 45 devices, c = 0.
2	1048	Blocking life: $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, $T_A = +200^\circ\text{C}$. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See [MIL-PRF-19500](#).
- b. Shall be chosen from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and in [4.4.3.1](#) (JANS) and [4.4.3.2](#) (JAN, JANTX, and JANTXV) herein for group C testing.

* 4.4.3.1 Group C inspection (JANS), table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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C2	2036	Test condition E; not applicable for U4 devices.
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* C5 3131 $R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see [1.3](#)).

* C6 1026 1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated P_T as defined in [1.3](#), $n = 45$, $c = 0$.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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C2	2036	Test condition E; not applicable for U4 devices.
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C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).
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C6		Not applicable.
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4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes [table I](#) tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
* Visual and mechanical examination <u>3/</u>	2071					
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>4/ 6/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		Table I , subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T _A = +250°C at t = 24 hrs or T _A = +300°C at t = 2 hrs n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.2	Z _{θJX}			°C/W
* Collector to base cutoff current 2N5010, 2N5010S, U4 2N5011, 2N5011S, U4 2N5012, 2N5012S, U4 2N5013, 2N5013S, U4 2N5014, 2N5014S, U4 2N5015, 2N5015S, U4	3036	Condition D V _{CB} = 400 V dc V _{CB} = 500 V dc V _{CB} = 580 V dc V _{CB} = 650 V dc V _{CB} = 700 V dc V _{CB} = 760 V dc	I _{CBO1}		10 10 10 10 10 10	nA dc
* Emitter to base cutoff current	3061	Condition D, V _{EB} = 4 V dc	I _{EBO1}		20	μA dc
Breakdown voltage, collector to base 2N5010, 2N5010S, U4 2N5011, 2N5011S, U4 2N5012, 2N5012S, U4 2N5013, 2N5013S, U4 2N5014, 2N5014S, U4 2N5015, 2N5015S, U4		I _E = 0 mA dc I _C = 0.1 mA dc I _C = 0.1 mA dc I _C = 0.1 mA dc I _C = 0.2 mA dc I _C = 0.2 mA dc I _C = 0.2 mA dc	V _{(BR)CBO}		500 600 700 800 900 1,000	V dc
Breakdown voltage, emitter to base		I _C = 0 mA dc, I _E = 0.05 mA dc	V _{(BR)EBO}		5	V dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
* Breakdown voltage, collector to emitter 2N5010, 2N5010S, U4 2N5011, 2N5011S, U4 2N5012, 2N5012S, U4 2N5013, 2N5013S, U4 2N5014, 2N5014S, U4 2N5015, 2N5015S, U4	3011	Bias condition B; $R_{BE} = 1K\Omega$ $I_C = 0.2$ mA dc pulsed (see 4.5.1)	$V_{(BR)CER}$	500 600 700 800 900 1,000		V dc
Forward-current transfer ratio 2N5010, 2N5011, 2N5012 2N5010S, 2N5010U4, 2N5011S, 2N5011U4, 2N5012S, 2N5012U4 2N5013, 2N5014, 2N5015 2N5013S, 2N5014U4, 2N5015S, 2N5013U4, 2N5014S, 2N5015U4	3076	$V_{CE} = 10$ V dc; $I_C = 25$ mA dc $V_{CE} = 10$ V dc; $I_C = 20$ mA dc	h_{FE1}	30 30	180 180	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 5$ mA dc	h_{FE2}	10		
Base-emitter saturation voltage 2N5010, 2N5010S, U4 2N5011, 2N5011S, U4 2N5012, 2N5012S, U4 2N5013, 2N5013S, U4 2N5014, 2N5014S, U4 2N5015, 2N5015S, U4	3066	Test condition A; $I_B = 5$ mA dc; pulsed (see 4.5.1) $I_C = 25$ mA dc $I_C = 25$ mA dc $I_C = 25$ mA dc $I_C = 20$ mA dc $I_C = 20$ mA dc $I_C = 20$ mA dc	$V_{BE(sat)1}$		1 1 1 1 1 1	V dc V dc V dc V dc V dc V dc
Collector-emitter saturation voltage 2N5010, 2N5010S, U4 2N5011, 2N5011S, U4 2N5012, 2N5012S, U4 2N5013, 2N5013S, U4 2N5014, 2N5014S, U4 2N5015, 2N5015S, U4	3071	$I_B = 5$ mA dc; pulsed (see 4.5.1) $I_C = 25$ mA dc $I_C = 25$ mA dc $I_C = 25$ mA dc $I_C = 20$ mA dc $I_C = 20$ mA dc $I_C = 20$ mA dc	$V_{CE(sat)1}$		1.4 1.5 1.6 1.6 1.6 1.8	V dc V dc V dc V dc V dc V dc

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
High temperature operation		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D;	I_{CBO2}			$\mu\text{A dc}$
2N5010, 2N5010S, U4		$V_{CB} = 400 \text{ V dc}$			10	
2N5011, 2N5011S, U4		$V_{CB} = 500 \text{ V dc}$			10	
2N5012, 2N5012S, U4		$V_{CB} = 588 \text{ V dc}$			10	
2N5013, 2N5013S, U4		$V_{CB} = 650 \text{ V dc}$			10	
2N5014, 2N5014S, U4		$V_{CB} = 700 \text{ V dc}$			10	
2N5015, 2N5015S, U4		$V_{CB} = 760 \text{ V dc}$			10	
Low temperature operation		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 20 \text{ mA dc}$	h_{FE3}	10		
<u>Subgroup 4</u>						
Magnitude of small-signal short-circuit forward current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 25 \text{ mA dc}; f = 10 \text{ MHz}$	$/h_{fe}/$	1		
2N5010, 2N5011, 2N5012 2N5010S, 2N5010U4, 2N5011S, 2N5011U4, 2N5012S, 2N5012U4						
Magnitude of small-signal short-circuit forward current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 20 \text{ mA dc}; f = 10 \text{ MHz}$	$/h_{fe}/$	1		
2N5013, 2N5014, 2N5015 2N5013S, 2N5014S, 2N5015S, 2N5013U4, 2N5014U4, 2N5015U4						
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0; f = 2 \text{ MHz}$	C_{obo}		30	pF
<u>Subgroups 5 and 6</u>						
Not required						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed table I, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

6/ This hermetic seal test is an end-point to temp cycling in addition to electrical measurements.

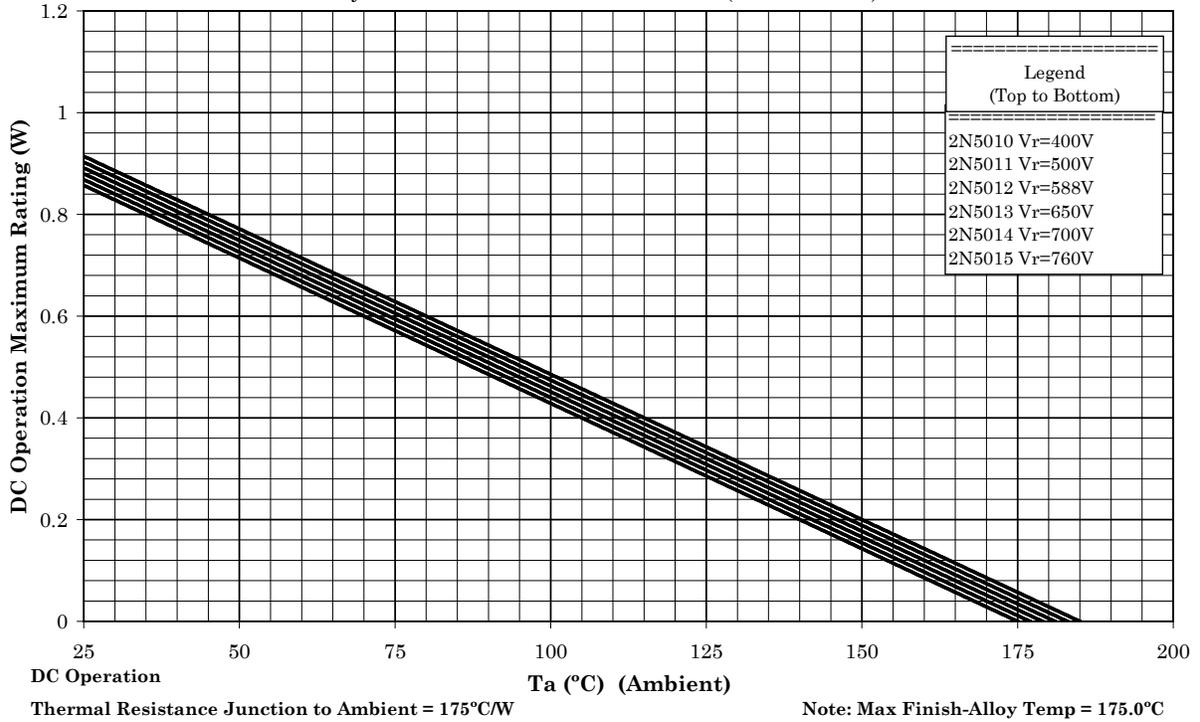
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* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			
* Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			15 devices c = 0
* Barometric pressure	1001	$I_C = 0.1$ mA, condition D, pressure = 8 mm HG, normal mounting, t = 60 seconds minimum.	
<u>Subgroup 6</u>			
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A.	

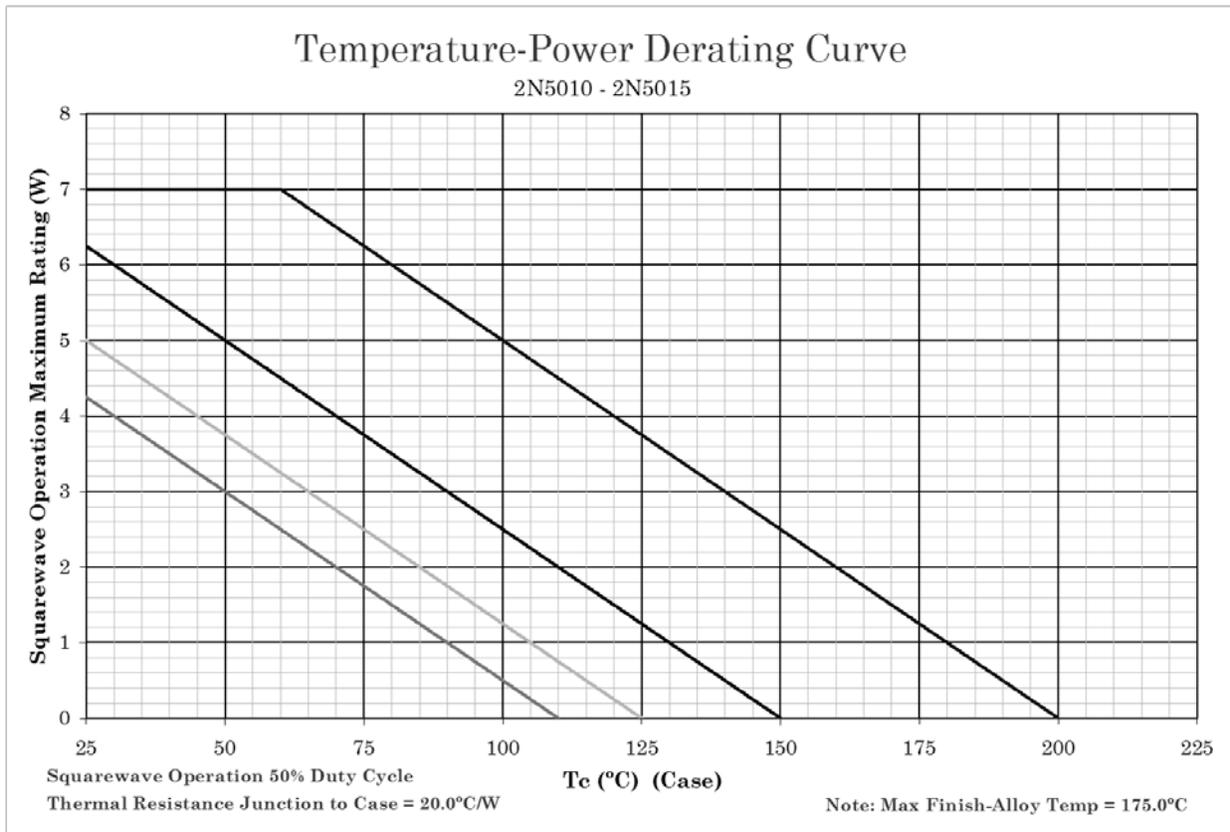
Ambient Derating Curves

Family Curves $T_a=25^\circ\text{C}$ 2N5010 - 2N5015 (TO-39 & PCB)



NOTE: Applies only to ambient (free air) operation either as TO-5, TO-39, or as U4 on a PCB (dc operation).

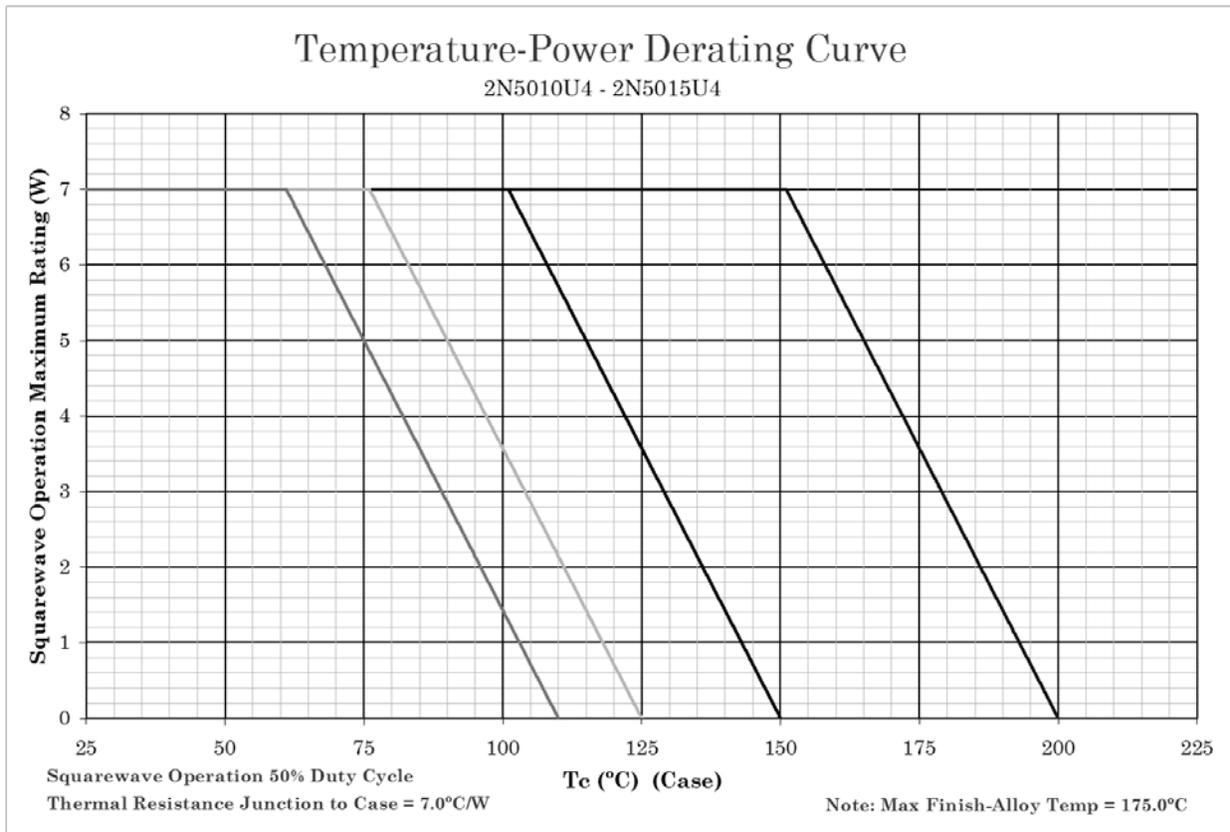
FIGURE 3. Ambient temperature-power derating curve.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 4. Temperature-power derating for steel (TO-5 and TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating for (U4).

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Maximum Thermal Impedance

Free Air $T_A=25^\circ\text{C}$

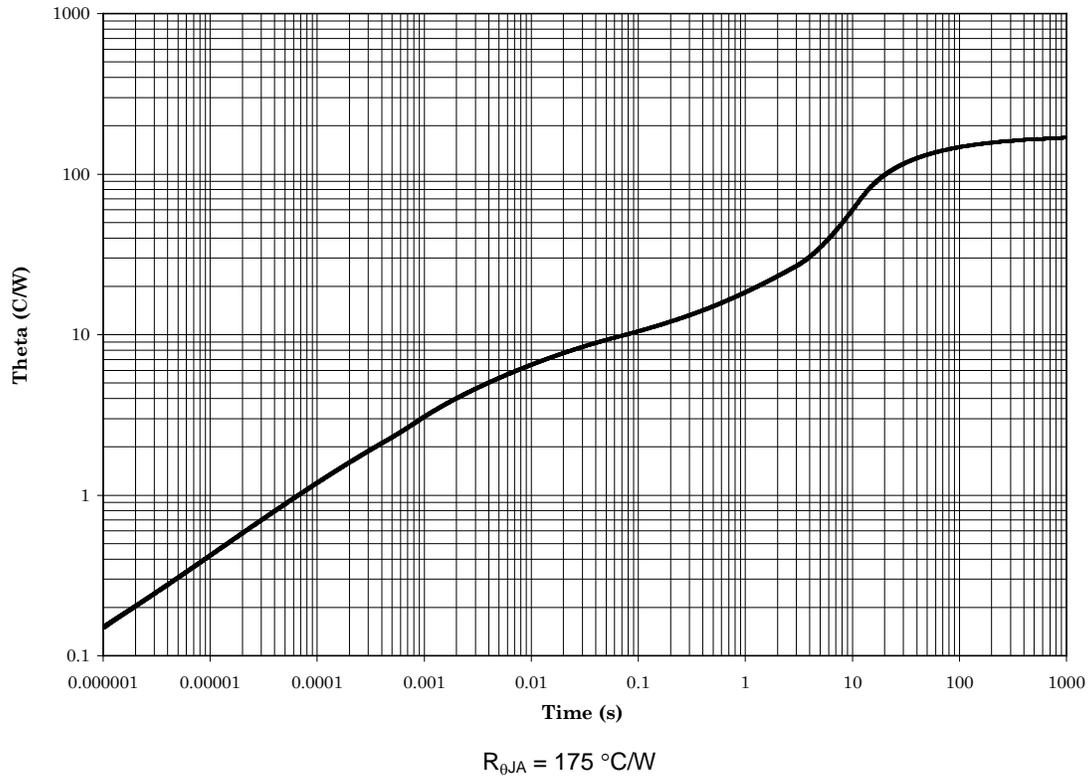


FIGURE 6. Thermal impedance graph for 2N5010 through 2N5015 steel (TO-5 and TO-39).

Maximum Thermal Impedance

Free Air $T_A=25^\circ\text{C}$

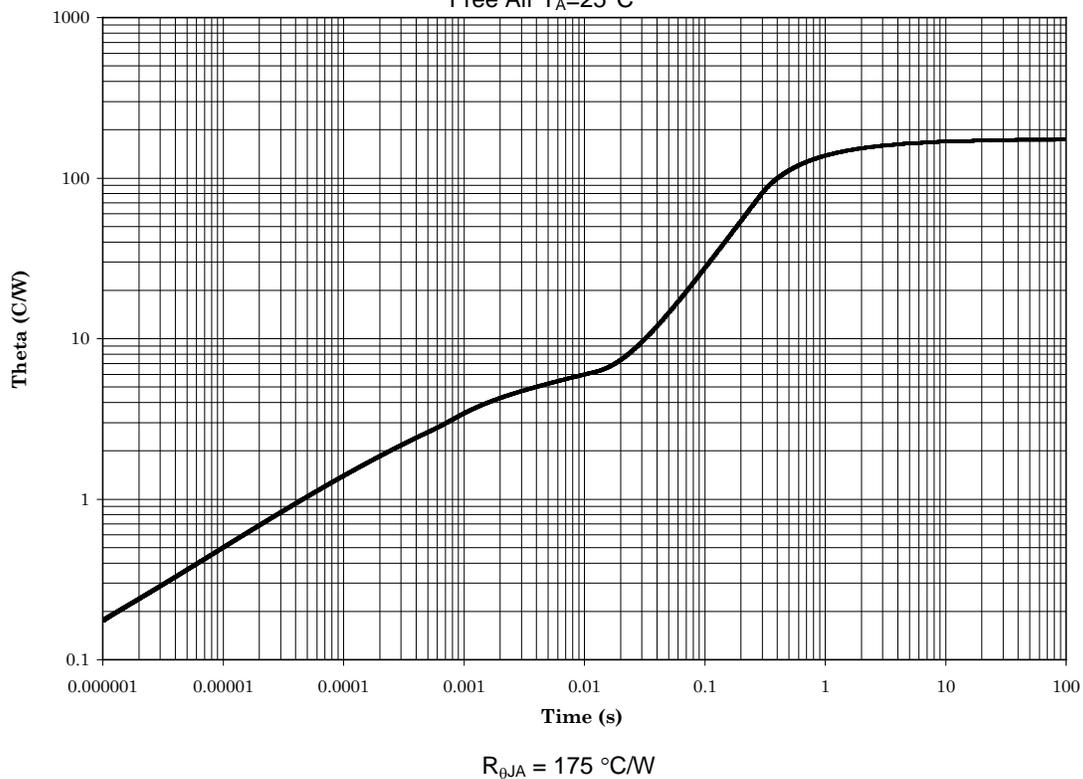


FIGURE 7. Thermal impedance graph for 2N5010U4 through 2N5015U4.

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Maximum Thermal Impedance
Case Mount $T_C=25^\circ\text{C}$

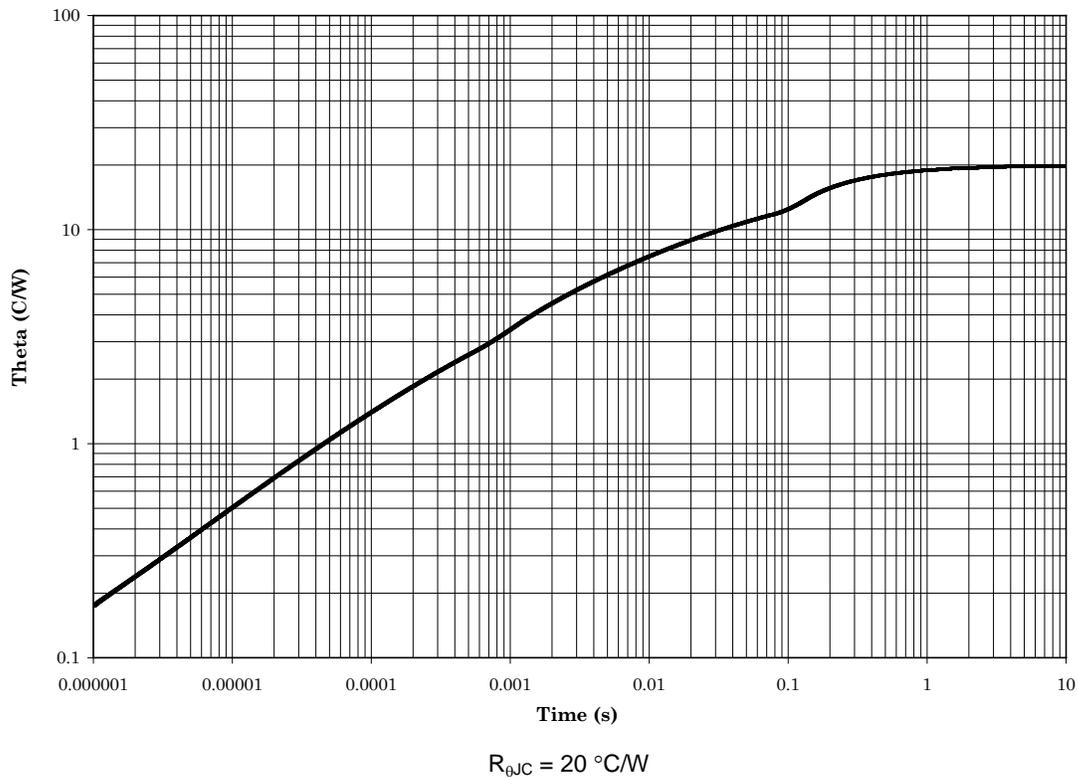


FIGURE 8. Thermal impedance graph for 2N5010 through 2N5015, steel (TO-5 and TO-39).

Maximum Thermal Impedance

Case Mount $T_C=25^\circ\text{C}$

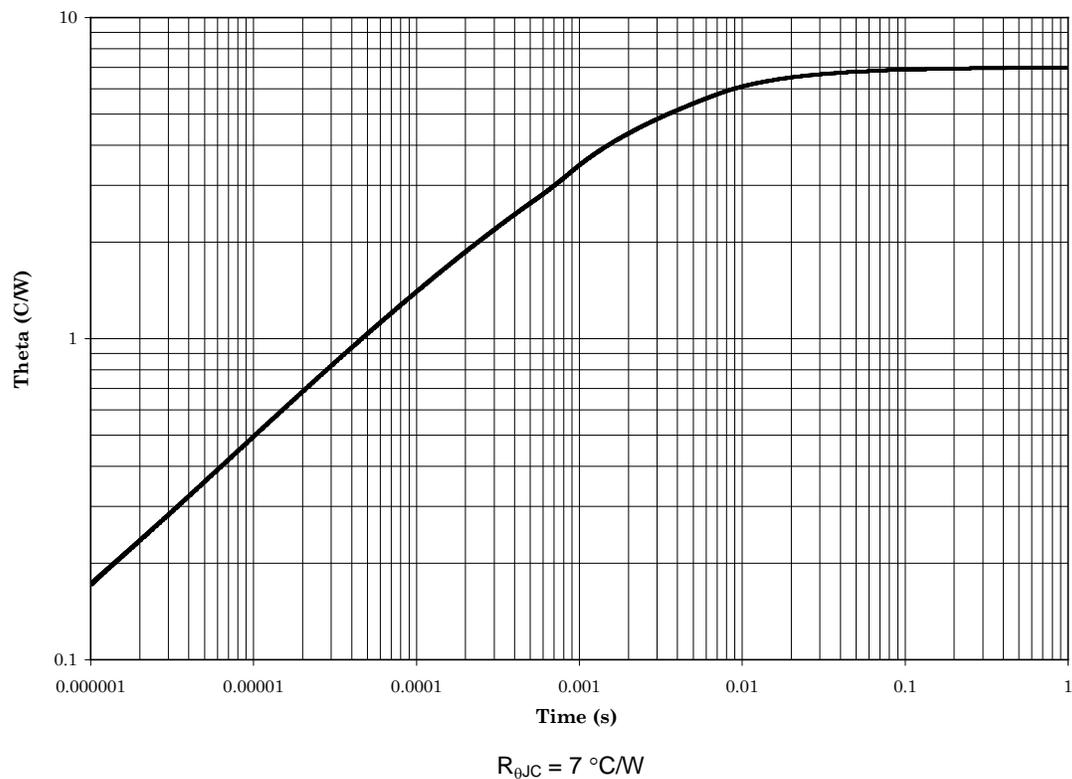


FIGURE 9. Thermal impedance graph for 2N5010U4 through 2N5015U4.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
 - b. Packaging requirements (see 5.1).
 - c. Lead finish (see 3.4.1).
 - * d. The complete Part or Identifying Number (PIN), see title and section 1.
 - e. Surface mount designation if applicable.
- * 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil/>.
- * 6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2014-137)

Review activities:

Army - AR, MI, SM
Navy - AS, MC
Air Force - 19, 71, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.