

The documentation and process conversion measures necessary to comply with this revision shall be completed by 16 March 2017.

INCH-POUND

MIL-PRF-19500/713D  
 AMENDMENT 1  
 16 December 2016  
 SUPERSEDING  
 MIL-PRF-19500/713D  
 3 April 2015

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, RADIATION HARDENED  
 P-CHANNEL, SILICON, DEVICE TYPES 2N7549T1, 2N7549U2, 2N7550T1, AND 2N7550U2,  
 JANTXVR, F AND JANSR, F

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating ( $E_{AS}$ ) and maximum avalanche current ( $I_{AS}$ ) for use in particular power-switching applications. See 6.7 for JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with [figure 1](#) and SMD2 TO-276AC (U2) in accordance with [figure 2](#) for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet [MIL-PRF-19500/741](#).

1.3 Maximum ratings. Unless otherwise specified,  $T_A = +25^\circ\text{C}$ .

Type	$P_T$ (1) $T_C = +25^\circ\text{C}$	$P_T$ $T_A = +25^\circ\text{C}$ (free air)	$R_{\theta JC}$ (2)	$V_{DS}$	$V_{DG}$	$V_{GS}$	$I_{D1}$ (3) (4) $T_C = +25^\circ\text{C}$	$I_{D2}$ (3) (4) $T_C = +100^\circ\text{C}$	$I_S$	$I_{DM}$ (5)	$T_J$ and $T_{STG}$	$V_{ISO}$ 70,000 foot altitude
	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u><math>^\circ\text{C}</math></u>	<u>V dc</u>
2N7550T1	208	2.6	0.60	-100	-100	$\pm 20$	-45	-28.5	-45	-180	-55	100
2N7550U2	250	1.6	0.50	-100	-100	$\pm 20$	-47	-30	-47	-188	to	100
2N7549T1	208	2.6	0.60	-200	-200	$\pm 20$	-30	-19	-30	-120	+150	200
2N7549U2	250	1.6	0.50	-200	-200	$\pm 20$	-33.5	-21	-33.5	-134		200

- (1) Derate linearly by 2.0 W/ $^\circ\text{C}$  (U2) or 1.67 W/ $^\circ\text{C}$  (T1) for  $T_C > +25^\circ\text{C}$ .
- (2) See [figure 3](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical  $I_D$  limit.  $I_D$  is limited by package design and device construction, to 45 A for T1 or limited to 56 A for U2:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 4](#), maximum drain current graph.
- (5)  $I_{DM} = 4 \times I_{D1}$ , as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.



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1.4 Primary electrical characteristics. Unless otherwise specified,  $T_C = +25^\circ\text{C}$ .

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0$ mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0$ mA dc		Max $I_{DSS1}$ $V_{GS} = 0$ $V_{DS} = 80$ percent of rated $V_{DS}$	Max $r_{DS(ON)}$ (1) $V_{GS} = 12\text{ V dc}$		$E_{AS}$ at $I_{D1}$	$I_{AS}$
					$T_J = +25^\circ\text{C}$ at $I_{D2}$	$T_J = +150^\circ\text{C}$ at $I_{D2}$		
	<u>V dc</u>	<u>V dc</u>		<u><math>\mu\text{A dc}</math></u>	<u>ohm</u>	<u>ohm</u>	<u>mJ</u>	<u>A</u>
		Min	Max					
2N7550T1	-100	-2.0	-4.0	-10	0.050	0.103	480	-45
2N7550U2	-100	-2.0	-4.0	-10	0.049	0.113	400	-47
2N7549T1	-200	-2.0	-4.0	-10	0.103	0.232	332	-30
2N7549U2	-200	-2.0	-4.0	-10	0.102	0.224	303	-33.5

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.

1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "M", "D", "P", "L", "R", and "F".

1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

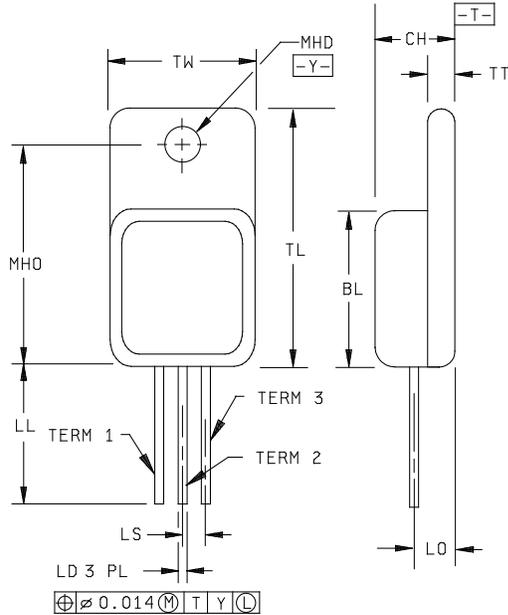
1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7549" and "7550".

1.5.4.3 Suffix letters. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of [figure 1](#). The suffix letters "U2" are used on devices packaged in the SMD2 TO-276AC (U2) package of [figure 2](#)

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

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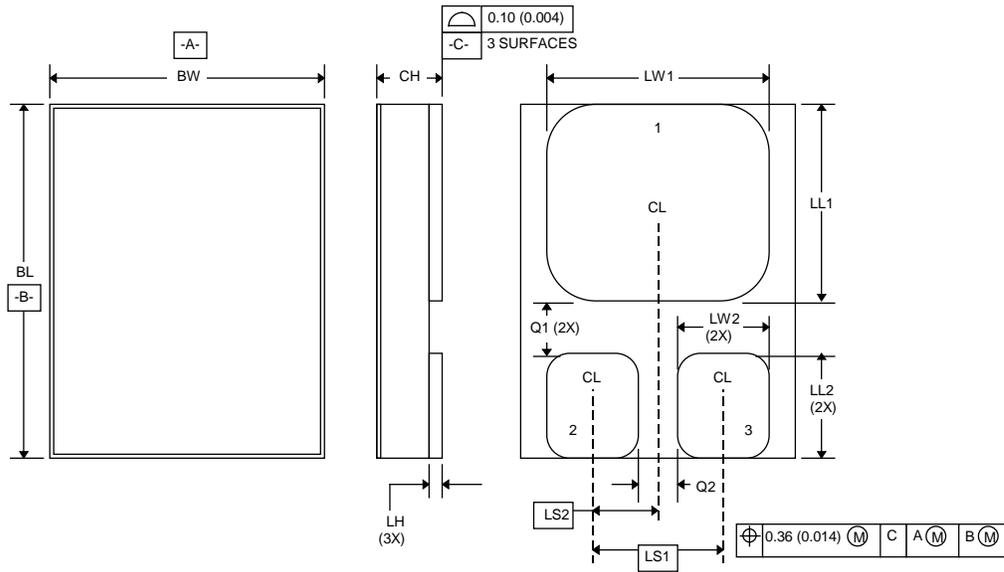
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.33	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.79	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7549T1 and 2N7550T1).

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
CH		.142		3.61
LH	.010	.020	0.25	0.51
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.12
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.
4. Terminal 1 – Drain, Terminal 2 – Gate, Terminal 3 – Source.

FIGURE 2. Physical dimensions for SMD2 TO-276AC (2N7550U2 and 2N7549U2).

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## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figures 1](#) (T1, TO-254AA) and [2](#) (U2, surface mount TO-276AC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

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3.5.1 Handling. MOS devices shall be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate shall be terminated to source,  $R \leq 100 \text{ k}\Omega$ , whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

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\* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E <sub>AS</sub> (see 4.3.2)	Method 3470 of MIL-STD-750, E <sub>AS</sub> (see 4.3.2)
(4) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein; I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub>	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(on)1</sub> , V <sub>GS(TH)1</sub> ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(on)1</sub> , V <sub>GS(TH)1</sub>
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr <sub>DS(on)1</sub> = ±20 percent of initial value. ΔV <sub>GS(TH)1</sub> = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr <sub>DS(on)1</sub> = ±20 percent of initial value. ΔV <sub>GS(TH)1</sub> = ±20 percent of initial value.
17	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

- (1) At the end of the test program, I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, and I<sub>DSS1</sub> are measured.
- \* (2) An out-of-family program to characterize I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, I<sub>DSS1</sub>, V<sub>GS(th)1</sub>, and r<sub>DS(on)1</sub> shall be invoked.
- (3) Shall be performed anytime before screen 9.
- (4) Shall be performed anytime after temperature cycling, screen 3a. JANTXV level does not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply  $V_{GS} = 30$  V minimum for  $t = 250$   $\mu$ s, minimum.

4.3.2 Single pulse avalanche energy ( $E_{AS}$ ).

- a. Peak current .....  $I_{AS} = I_{D1}$ .
- b. Inductance .....  $L = \left[ \frac{2E_{AS}}{(I_{D1})^2} \right] \left[ \frac{V_{BR} - V_{DD}}{V_{BR}} \right]$  mH minimum.
- c. Gate to source resistor  $R_{GS}$  .....  $25 \Omega \leq R_{GS} \leq 200 \Omega$ .
- d. Supply voltage .....  $V_{DD} = 50$  V dc
- e. Initial case temperature .....  $T_c = +25^\circ$  C,  $-5^\circ$  C,  $+10^\circ$  C.
- f. Gate voltage .....  $V_{GS} = 12$  V dc.
- g. Number of pulses to be applied ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$ , (and  $V_H$  where appropriate) (see [figure 4](#) herein). Measurement delay time ( $t_{MD}$ ) = 70  $\mu$ s max. See [table III](#), group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage ..... 900 V dc.
- b. Duration of application of test voltage ..... 15 seconds (min).
- c. Points of application of test voltage ..... All leads to case (bunch connection).
- d. Method of connection ..... Mechanical.
- e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).
- f. Maximum leakage current ..... 1.0 mA.
- g. Voltage ramp up time ..... 500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and as follows.

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\* 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM (scanning electron microscope).
B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$ ; $T_A = +175^\circ\text{C}$ , $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$ , $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$ ; $T_A = +175^\circ\text{C}$ , $t = 120$ hours minimum; or $T_A = +150^\circ\text{C}$ , $t = 240$ hours minimum.
B5	2037	Bond strength, test condition D.

\* 4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5 and B6		Not applicable.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
* C2	2036	Test condition A; weight = 10 pounds; $t = 15$ s, not applicable to 2N7550U2 and 2N7549U2.
C5	3161	See 4.3.3, $R_{\theta JC(max)} = 0.60$ °C/W (T1) or $0.50$ °C/W (U2).
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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 TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source 2N7550T1 and U2 2N7549T1 and U2	3407	$V_{GS} = 0$ V dc, $I_D = -1$ mA dc, bias condition C	$V_{(BR)DSS}$	-100 -200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = -1$ mA dc	$V_{GS(th)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	$I_{GSSF1}$		+100	nA dc
Gate reverse current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	$I_{GSSR1}$		-100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS1}$		-10	μA dc
Static drain to source on-state resistance 2N7550T1 2N7550U2 2N7549T1 2N7549U2	3421	$V_{GS} = -12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$		0.050 0.049 0.103 0.102	Ω Ω Ω Ω
Forward voltage	4011	Condition A, $I_D = I_{D1}$ , $V_{GS} = 0$ V dc	$V_{SD}$		-5.0	V
<u>Subgroup 3</u>						
High-temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate reverse current	3411	$V_{GS} = -20$ V dc and +20 V dc, bias condition C, $V_{DS} = 0$	$I_{GSS2}$		± 200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS2}$		-25	μA dc

See footnotes at end of table.

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 TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 3</u> - continued	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
High-temperature operation: Static drain to source on-state resistance 2N7550T1 2N7550U2 2N7549T1 2N7549U2	3421	$T_C = T_J = +125^\circ\text{C}$ $V_{GS} = -12\text{ V dc}$ , pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$		0.100 0.098 0.206 0.204	$\Omega$ $\Omega$ $\Omega$ $\Omega$
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = -1\text{ mA dc}$	$V_{GS(th)2}$	-1.0		V dc
Low-temperature operation: Gate to source voltage (threshold)	3403	$T_C = T_J = -55^\circ\text{C}$ $V_{DS} \geq V_{GS}$ , $I_D = -1\text{ mA dc}$	$V_{GS(th)3}$		-5.0	V dc
<u>Subgroup 4</u> Forward transconductance 2N7550T1 and U2 2N7549T1 and U2	3475	$I_D = \text{rated } I_{D2}$ , $V_{DD} = -15\text{ V}$ (see 4.5.1)	gFS	24 23		S S
Switching time test Turn-on delay time	3472	$I_D = \text{rated } I_{D1}$ , $V_{GS} = -12\text{ V dc}$ , $R_G = 1.2\ \Omega$ (T1) or $2.35\ \Omega$ (U2), $V_{DD} = 50\text{ percent of rated } V_{DS}$	$t_{d(on)}$		35	ns
Rise time 2N7550T1 and U2 2N7549T1 and U2			$t_r$		100 100	ns ns
Turn-off delay time			$t_{d(off)}$		100	ns
Fall time			$t_f$		100	ns

See footnotes at end of table.

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 TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See <a href="#">figure 5</a> ; $t_p = 10$ ms, $V_{DS} = 80$ percent of rated $V_{DS}$				
Electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B	QG(on)		170 180	nC nC
2N7550T1 and U2 2N7549T1 and U2						
On-state gate charge			QGS		65 75	nC nC
2N7550T1 and U2 2N7549T1 and U2						
Gate to drain charge			QGD		30 50	nC nC
2N7550T1 and U2 2N7549T1 and U2						
Reverse recovery time		$di/dt \leq 100A/\mu s$ , $V_{DD} \leq 50$ V, $I_D = I_{D1}$	$t_{rr}$		200 230 300 450	ns ns ns ns
2N7550T1 2N7550U2 2N7549T1 2N7549U2						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:  
 Group B, subgroups 2 and 3 (JANTXV).  
 Group B, subgroups 3 and 4 (JANS).  
 Group C, subgroup 2 and 6.  
 Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>										
Not applicable										
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$								
Steady-state total dose irradiation ( $V_{GS}$ bias) <u>4/</u>	1019	$V_{GS} = -12\text{V}$ $V_{DS} = 0$								
Steady-state total dose irradiation ( $V_{DS}$ bias) <u>4/</u>	1019	$V_{GS} = 0$ $V_{DS} = 80$ percent of rated $V_{DS}$ (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ $I_D = -1$ mA bias cond. C	$V_{(BR)DSS}$							
2N7550T1, U2 2N7549T1, U2				-100 -200		-100 -200		-100 -200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GSth1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	$V_{GS} = -20$ V $V_{DS} = 0$ bias cond. C	$I_{GSSR1}$		-100		-100		-100	nA dc
Gate forward current	3411	$V_{GS} = 20$ V $V_{DS} = 0$ bias cond. C	$I_{GSSF1}$		100		100		100	nA dc
Drain current	3413	$V_{GS} = 0$ bias cond. C $V_{DS} = 80$ percent of rated $V_{DS}$ (pre-irradiation)	$I_{DSS1}$		-10		-10		-10	$\mu\text{A}$ dc

See footnotes at end of table.

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TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 2</u> - Continued:  Static drain to source on-state voltage  2N7550T1 2N7550U2 2N7549T1 2N7549U2	3405	$V_{GS} = -12$ V cond. A pulsed (see <a href="#">4.5.1</a> ) $I_D = I_{D2}$	$V_{DSon1}$							
					1.425		1.425		1.425	V dc
					1.500		1.500		1.500	V dc
					1.957		1.957		1.957	V dc
					2.163		2.163		2.163	V dc
Forward voltage source to drain diode	4011	$V_{GS} = 0$ , Condition A, $I_D = I_{D1}$	$V_{SD}$		-5.0		-5.0		-5.0	V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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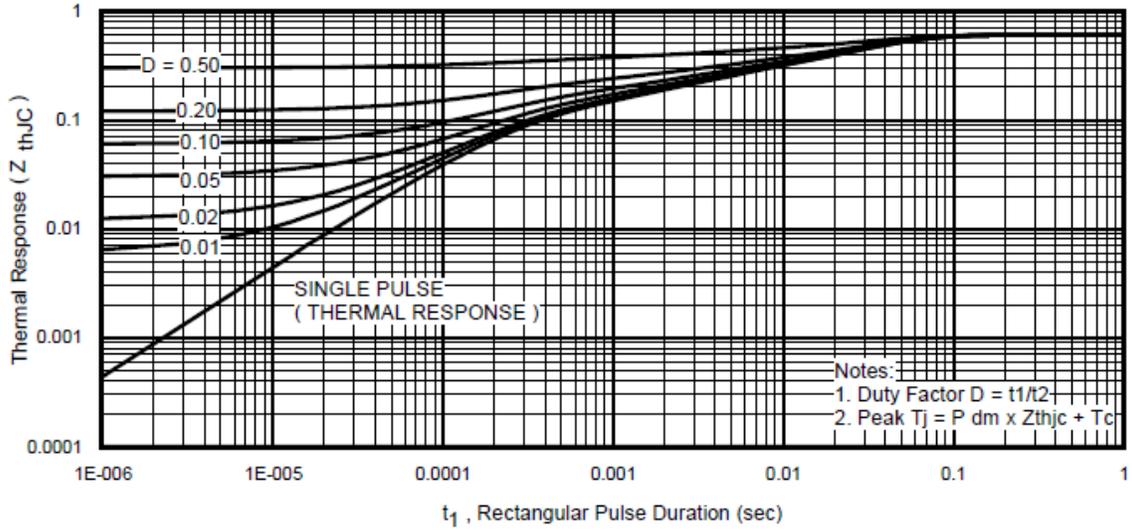
TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
Steady-state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See <a href="#">MIL-PRF-19500</a> .	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

- 1/ A separate sample for each test shall be pulled.  
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.  
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

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2N7550T1 & 2N7549T1



2N7550U2 & 2N7549U2

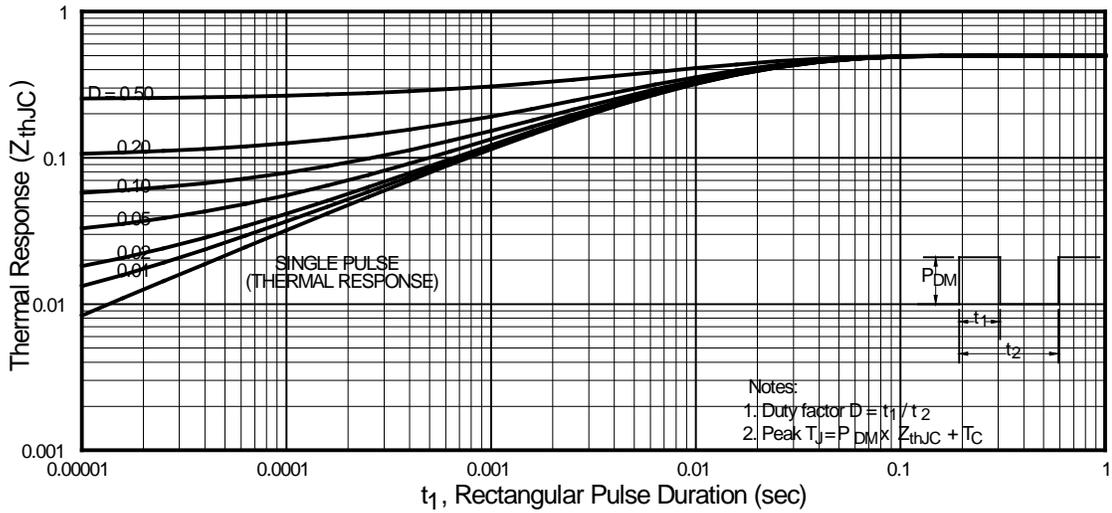


FIGURE 3. Thermal impedance curves.

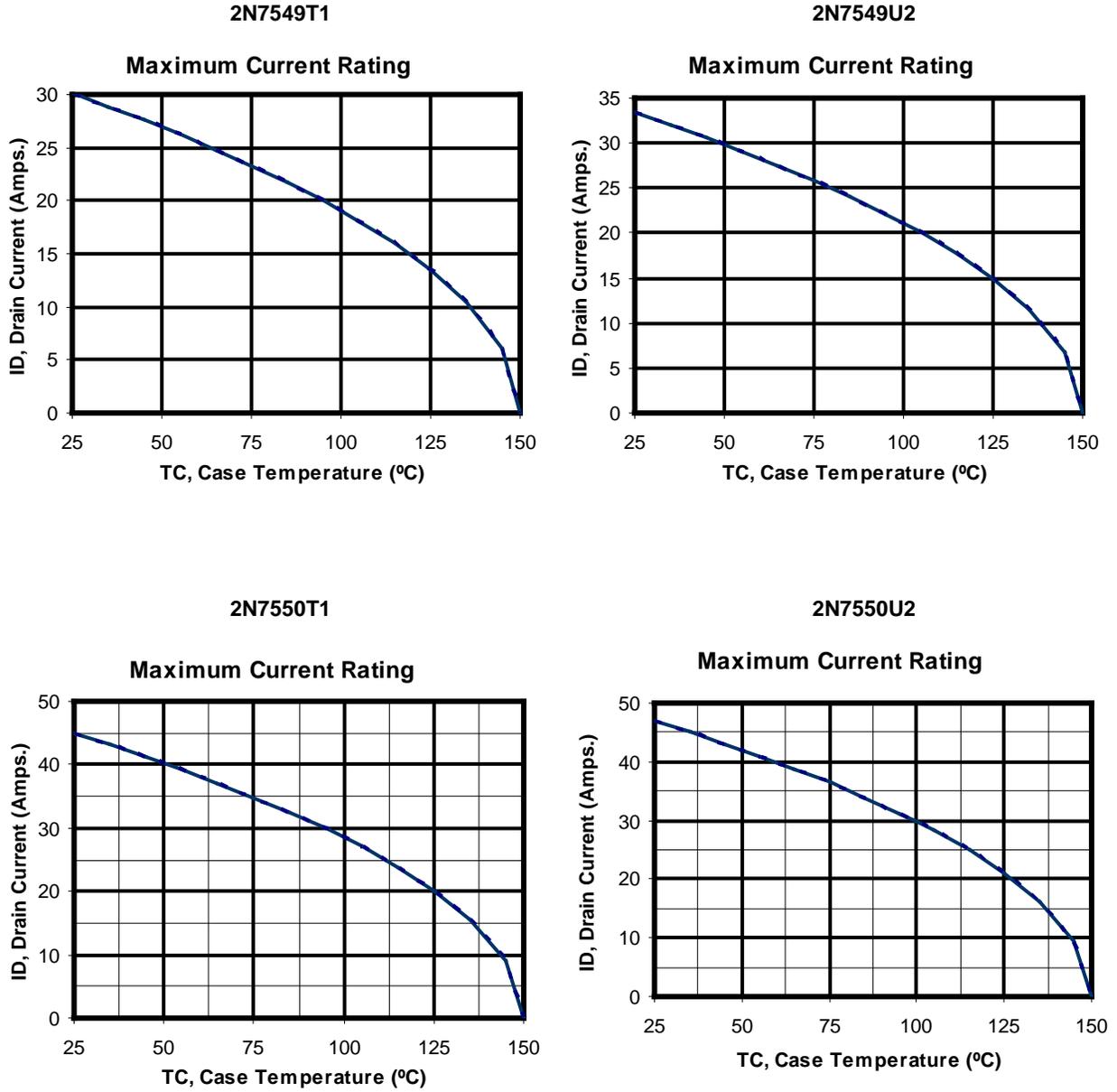
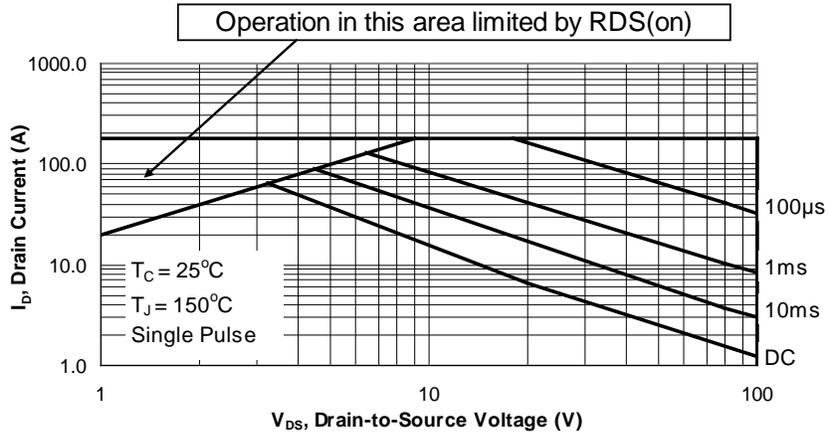
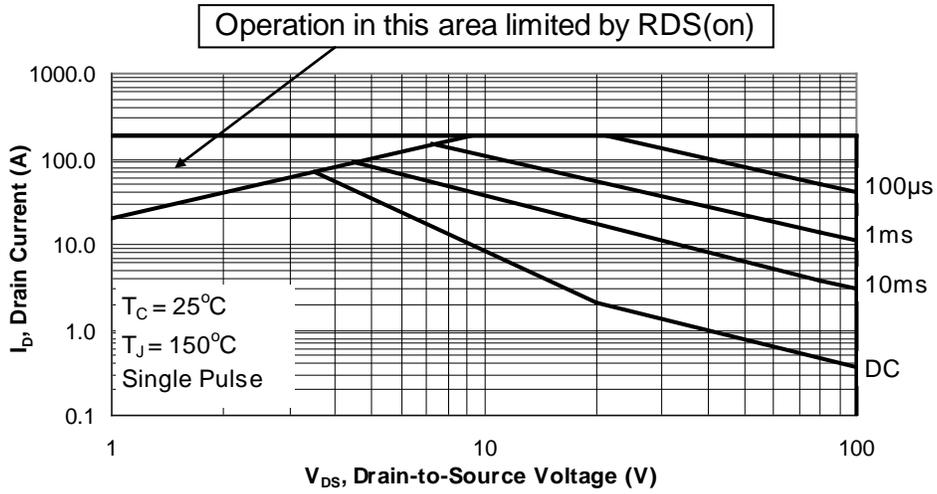


FIGURE 4. Maximum drain current versus case temperature graphs.

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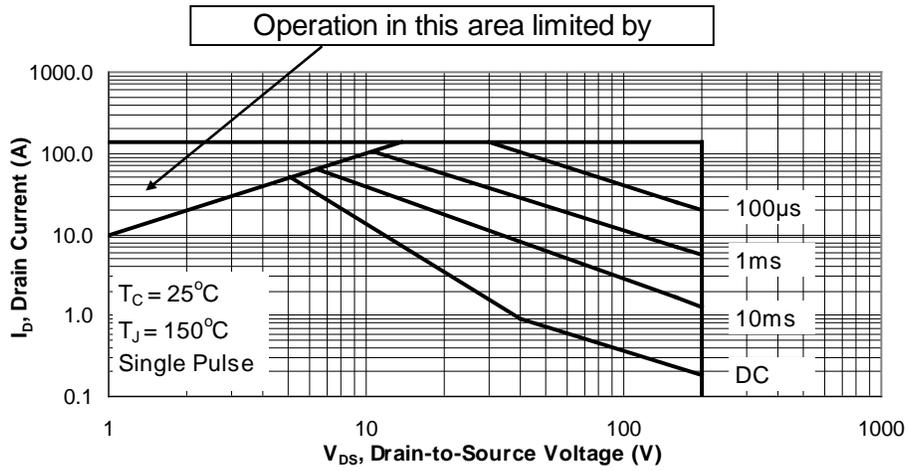
2N7550T1



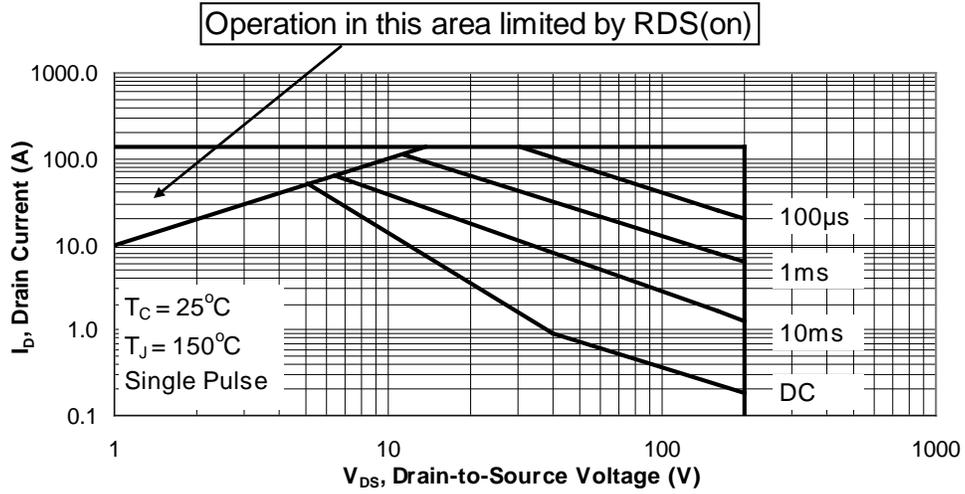
2N7550U2

FIGURE 5. Safe operating area graphs.

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2N7549T1



2N7549U2

FIGURE 5. Safe operating area graphs – Continued.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

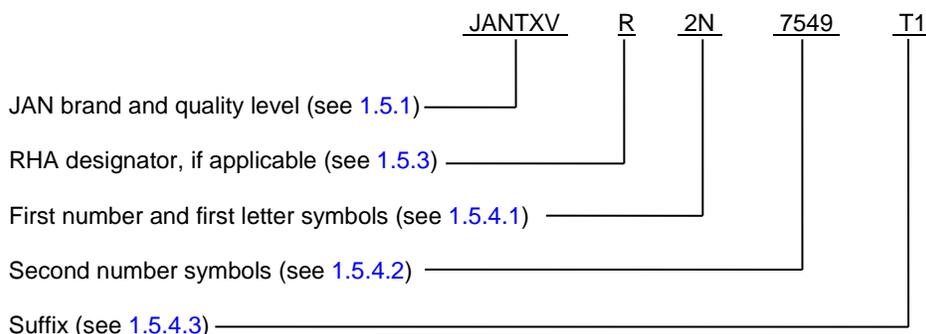
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see section 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

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6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7549T1	JANTXV#2N7549T1	JANS2N7549T1	JANS#2N7549T1
JANTXV2N7549U2	JANTXV#2N7549U2	JANS2N7549U2	JANS#2N7549U2
JANTXV2N7550T1	JANTXV#2N7550T1	JANS2N7550T1	JANS#2N7550T1
JANTXV2N7550U2	JANTXV#2N7550U2	JANS2N7550U2	JANS#2N7550U2

(1) The number sign (#) represent one of five RHA designators available (M, D, P, L, or R).

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix). Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Generic PIN	
	TO-254AA	TO-276AC (SMD2)
2N7550T1	IRHMS59_160	
2N7550U2		IRHNA59_160
2N7549T1	IRHMS59_260	
2N7549U2		IRHNA59_260

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

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6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
No manufacturers are currently qualified to the SEE requirements	SEE 1/	1080	See <a href="#">MIL-STD-750</a> method 1080	3 devices
	Electrical Measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with <a href="#">table I</a> , subgroup 2	
	Electrical Measurement		IGSSF1, IGSSR1, and IDSS1 in accordance with <a href="#">table I</a> , subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">                     Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.                 </div>				

1/ IGSSF1, IGSSR1, IDSS1 are examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option.

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\* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil) or by facsimile (614) 693-1642 or DSN 850-6939.

\* 6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:  
Army - CR  
Navy - EC  
Air Force - 85  
NASA - NA  
DLA - CC

Preparing activity:  
DLA - CC  
  
(Project 5961-2017-007)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.